ECE606: Solid State Devices
Lecture 24
MOSFET non-idealities

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Outline

1) Flat band voltage - What is it and how to measure it?

2) Threshold voltage shift due to trapped charges

3) Physics of interface traps

4) Conclusion

Ref: Sec. 16.4 of SDF Chapter 18, SDF

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1) Flat band voltage - What is it and how to measure it?

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$$I_D(V_D = V_{DD}) \sim (V_G - V_{th})^{\alpha}$$
$$1 < \alpha < 2$$

Ref: Sec. 16.4 of SDF Chapter 18, SDF

$$V_{th} = V_{th,ideal} + \phi_{MS} - \frac{\gamma_M Q_M}{C_O} - \frac{Q_F}{C_O} - \frac{Q_{IT}(\phi_s)}{C_O}$$

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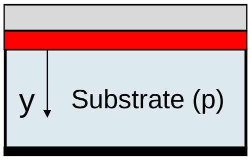
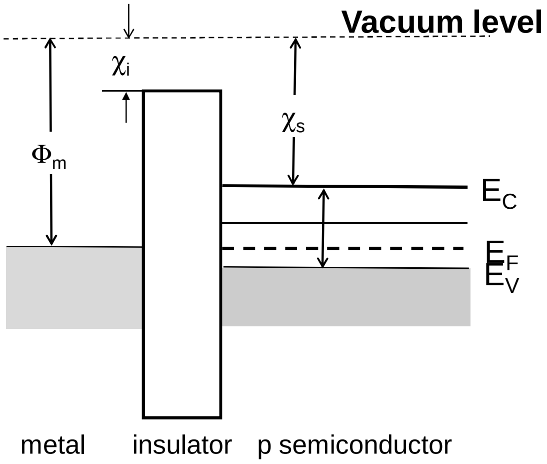
(1) Idealized MOS Capacitor

In the idealized MOS capacitor, the Fermi Levels in metal and semiconductor align perfectly so that at zero applied bias, the energy bands are flat

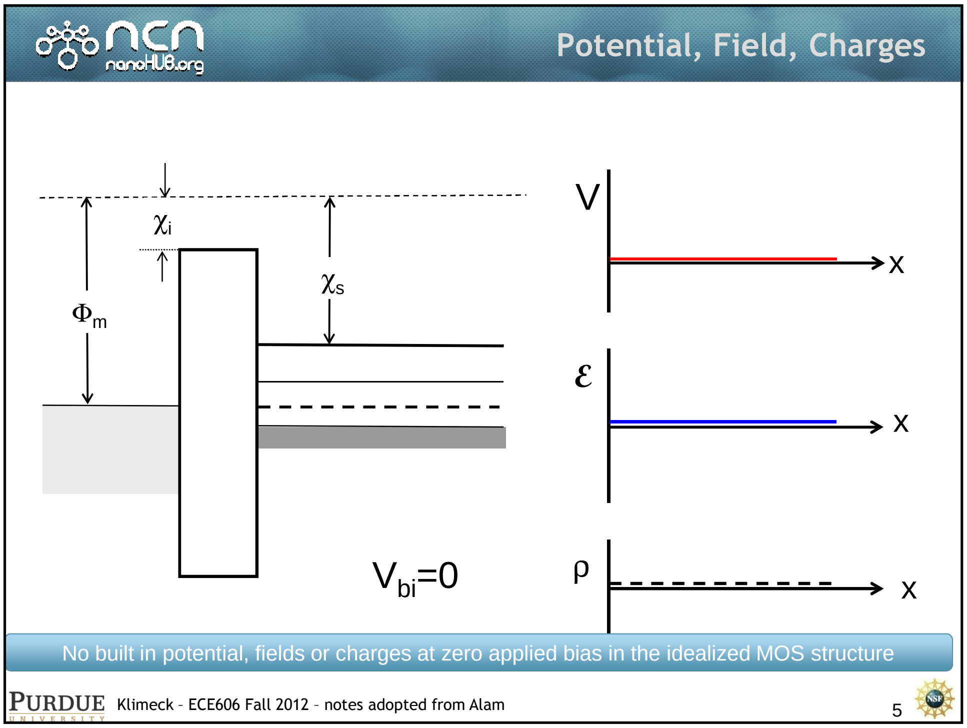




Recall that

$$Q_i = C_{ox}(V_G - V_{th,ideal})$$

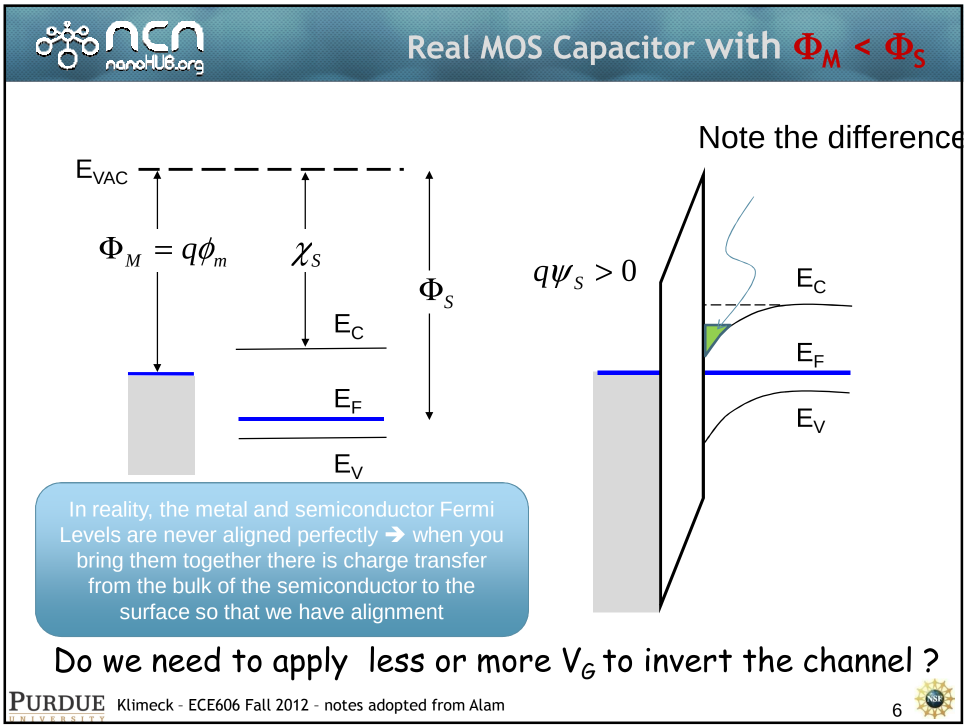
$$V_{th,ideal} = \psi_s - \left.\frac{Q_B}{C_{ox}}\right|_{\psi_s = 2\phi_F}$$



Potential, Field, Charges

$V_{bi}=0$

No built in potential, fields or charges at zero applied bias in the idealized MOS structure



Real MOS Capacitor with $\Phi_M < \Phi_S$

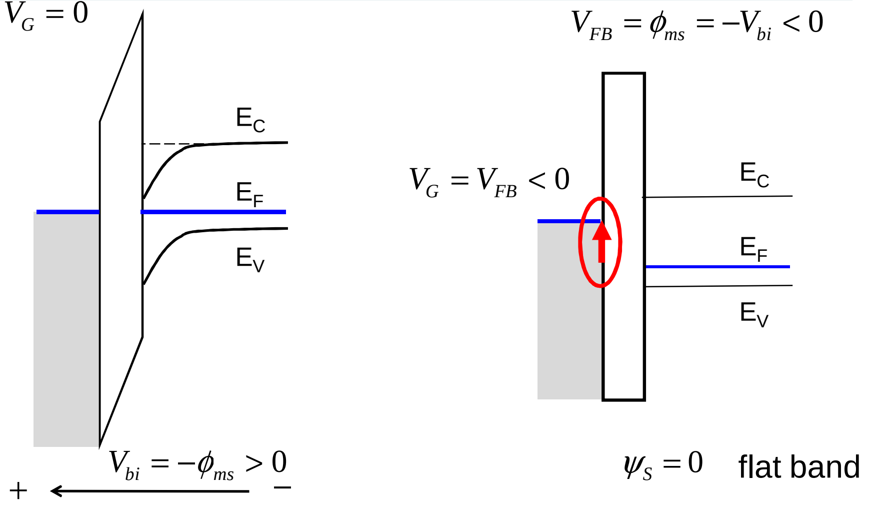
Note the difference

In reality, the metal and semiconductor Fermi Levels are never aligned perfectly ➔ when you bring them together there is charge transfer from the bulk of the semiconductor to the surface so that we have alignment

Do we need to apply less or more V_G to invert the channel ?

Physical Interpretation of Flatband Voltage

The Flatband Voltage is the voltage applied to the gate that gives zero-band bending in the MOS structure. Applying this voltage nullifies the effect of the built-in potential. This voltage needs to be incorporated into the idealized MOS analysis while calculating threshold voltage



$V_G = 0$

$V_{bi} = -\phi_{ms} > 0$

$V_{FB} = \phi_{ms} = -V_{bi} < 0$

$V_G = V_{FB} < 0$

$\psi_S = 0$ flat band

How to Calculate Built-in or Flat-band Voltage

The presence of a flatband voltage lowers or raises the threshold voltage of a MOS structure. Engineering question ➔ Is it desirable to have a metal having a work function greater or less than the electron affinity+(Ec-Ef) in the semiconductor?

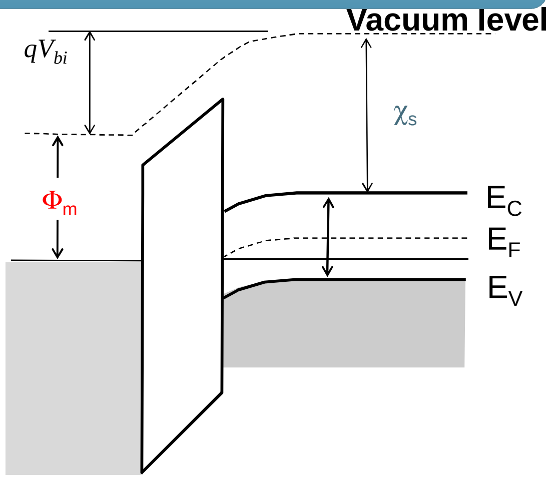
$$qV_{bi} = \left(\chi_s + E_g - \Delta_p\right) - \Phi_M$$

$$= qV_{FB} \equiv \phi_{MS}$$

Therefore,

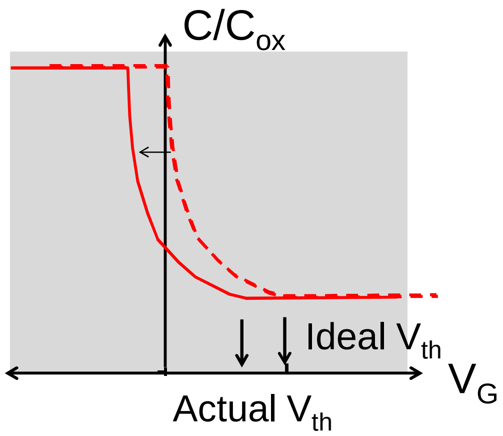
$$Q_i = C_{ox}(V_G - V_{th})$$

$$V_{th} = \left(2\phi_F - \frac{Q_B}{C_{ox}}\right) - V_{FB}$$



Measure of Flat-band shift from C-V Characteristics

The transition point between accumulation and depletion in a non-ideal MOS structure is shifted to the left when the metal work function is smaller that the electron affinity +(Ec-Ef). At **zero applied bias the semiconductor is already depleted** so that a very small positive bias inverts the channel. The flatband voltage is the amount of voltage required to shift the curve such that the transition point is at zero bias.



Outline

1) Flat band voltage - What is it and how to measure it?

2) Threshold voltage shift due to trapped charges

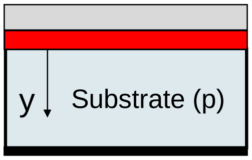
3) Physics of interface traps

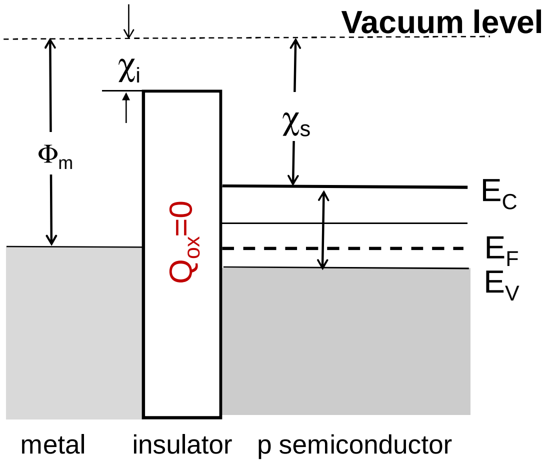
4) Conclusion

Ref: Sec. 16.4 of SDF Chapter 18, SDF

$$V_{th} = V_{th,ideal} + \phi_{MS} - \frac{\gamma_M Q_M}{C_{ox}} - \frac{Q_F}{C_{ox}} - \frac{Q_{IT}(\phi_s)}{C_{ox}}$$

(2) Idealized MOS Capacitor



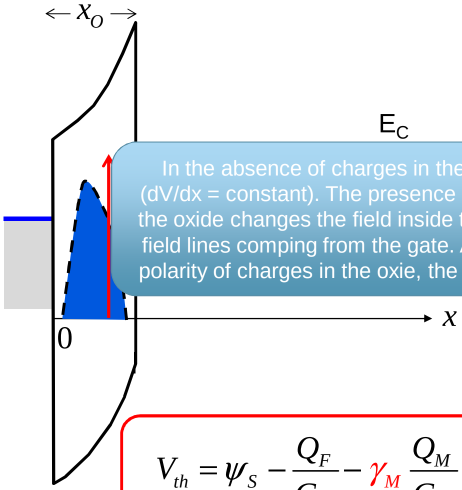


Recall that

$$Q_i = C_{ox}(V_G - V_{th,ideal})$$

$$V_{th,ideal} = \psi_s - \left.\frac{Q_B}{C_{ox}}\right|_{\psi_s = 2\phi_F}$$

Distributed Trapped charge in the Oxide



In the absence of charges in the oxide, the field is constant (dV/dx = constant). The presence of a charge distribution inside the oxide changes the field inside the oxide and effectively traps field lines comping from the gate. As a result, depending on the polarity of charges in the oxie, the threshold voltage is modified.

$$Q_M = \int^{x_O} \rho_{ox}(x)dx$$

$$(x)dx$$

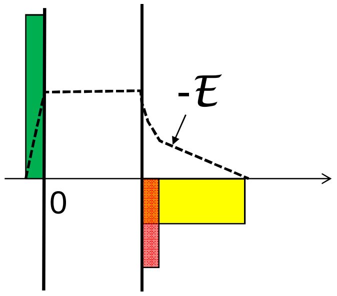
$$\gamma_M \quad x_0 \quad x_0 \int_0^{x_0} \rho_{ox}(x)dx$$

$$V_{th} = \psi_S - \frac{Q_F}{C_{ox}} - \gamma_M \frac{Q_M}{C_{ox}}$$

x_m represents the centroid of the charge distribution – one can think of this as replacing the entire distribution with a delta charge at this point

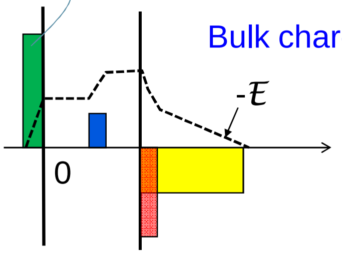
An Intuitive View

Ideal charge-free oxide

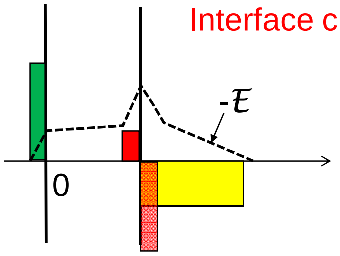


Reduced gate charge

Bulk charge



Interface charge



Gate Voltage and Oxide Charge

$$V_G = V_{ox} + \psi_s$$

Kirchoff's Law – balancing voltages

$$-\frac{d^2V_{ox}}{dx^2} = \frac{d\mathcal{E}_{ox}}{dx} = \frac{\rho_{ox}(x)}{\kappa_{ox}\varepsilon_0}$$

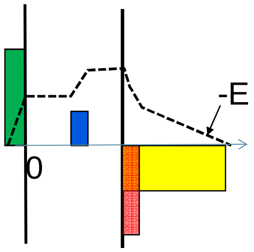
$$\int_{\mathcal{E}(x)}^{\mathcal{E}(x_0)} d\mathcal{E}_{ox} = \int_{x}^{x_0} \frac{\rho_{ox}(x')dx'}{\kappa_{ox}\varepsilon_0}$$

$$-\frac{dV_{ox}}{dx} = \mathcal{E}_{ox}(x_0) - \mathcal{E}_{ox}(x) = \mathcal{E}_{ox}(x_0) - \int_{0}^{x} \frac{\rho_{ox}(x')dx'}{\kappa_{ox}\varepsilon_0}$$

Known from boundary conditions in semiconductor and continuity of E

$$V_{ox} = \frac{\kappa_S}{\kappa_{ox}} x_0 \mathcal{E}_S(x_0) - \int_{0}^{x_0} dx \int_{0}^{x_0} \frac{\rho_{ox}(x')dx'}{\kappa_{ox}\varepsilon_0}$$

$$= \frac{\kappa_S}{\kappa_{ox}} x_0 \mathcal{E}_S(x_0) - \int_{0}^{x_0} \frac{x\rho_{ox}(x)dx}{\kappa_{ox}\varepsilon_0}$$



Gate Voltage and Oxide Charge

$$\Delta V_{ox} = \frac{\kappa_S}{\kappa_o} x_0 \mathcal{E}_S(x_0) - \int_0^{x_0} \frac{x\rho_{ox}(x)dx}{\left(\frac{\kappa_{ox}\varepsilon_0}{x_0}\right)x_0}$$

$$= \frac{\kappa_S}{\kappa_{ox}} x_0 \mathcal{E}_S(x_0) - \frac{1}{C_{ox}x_0}\int_0^{x_0} x\rho_{ox}(x)dx$$

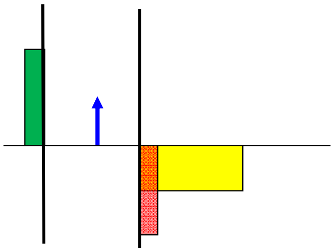
$$V_{th} = \psi_s(=2\phi_F) + \Delta V_{ox}$$

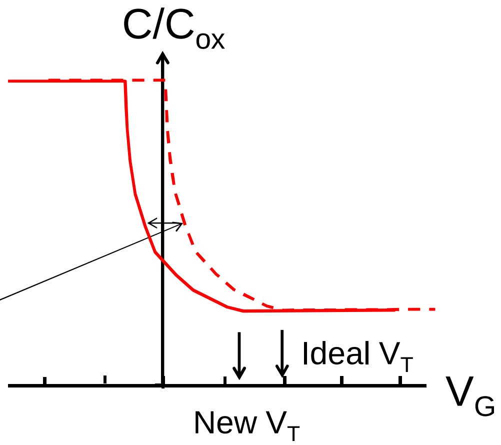
$$= \boxed{\psi_s(=2\phi_F) + \frac{\kappa_S}{\kappa_{ox}} x_0 \mathcal{E}_S(x_0)} - \frac{1}{C_o x_0}\int_0^{x_0} x\rho_{ox}(x)dx$$

$$= V_{th,ideal} - \frac{1}{C_{ox}x_0}\int_0^{x_0} x\rho_{ox}(x)dx$$

$$= V_{th,ideal} - \frac{Q_M}{C_{ox}}\gamma_M$$

Interpretation for Bulk Charge

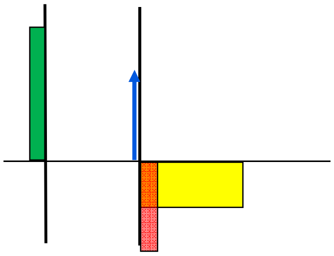


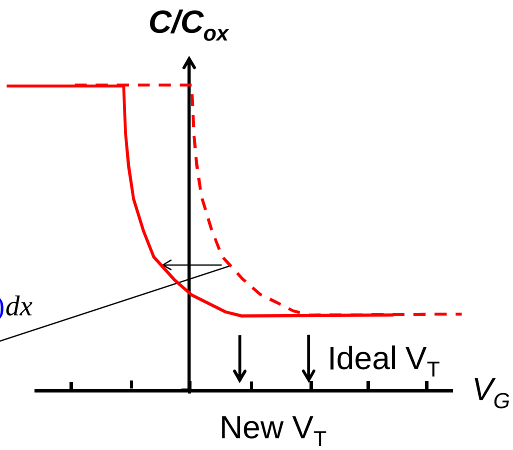


$$V_{th} = V_{th,ideal} - \frac{1}{C_o x_0}\int_0^{x_0} x\rho_{ox}(x)\delta(x-x_1)dx$$

$$= V_{th,ideal} - \boxed{\frac{x_1}{x_0}\frac{Q_M(x_1)}{C_o}}$$

Interpretation for Interface Charge

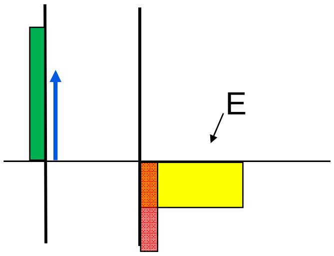


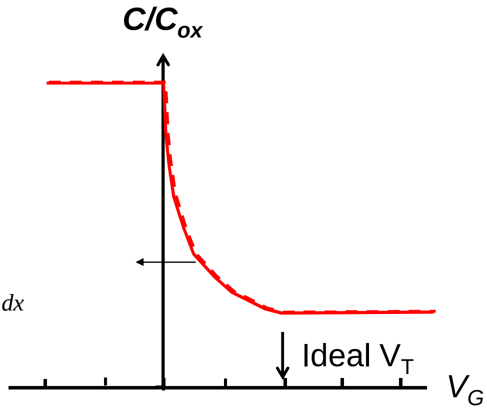


$$V_{th} = V_{th}^{*} - \frac{1}{C_o x_0}\int_0^{x_0} x\rho_{ox}(x)\delta(x-x_o)dx$$

$$= V_{th}^{*} - \frac{Q_F}{C_o}$$

Time-dependent shift of Trapped Charge



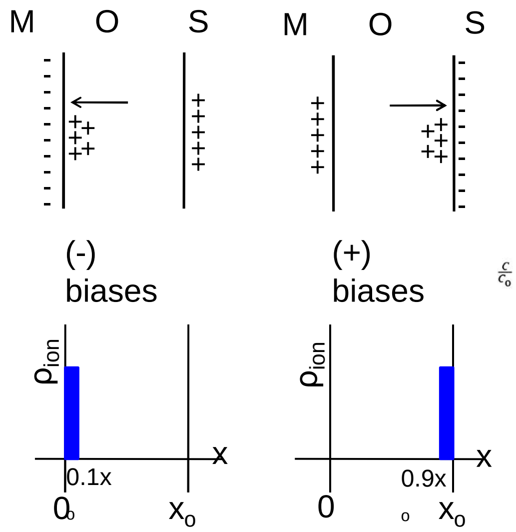


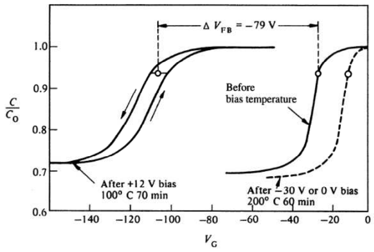
$$V_{th} = V_{th,ideal} - \frac{1}{C_{ox} x_0}\int_0^{x_0} xQ_{ox}(x)\times\delta(x-x_1(t))dx$$

$$= V_{th,ideal} - \frac{x_1(t)}{x_0}\times\frac{Q_{ox}(x)}{C_{ox}}$$

Sodium related bias temperature instability (BTI) issue

Bias Temperature Instability (Experiment)





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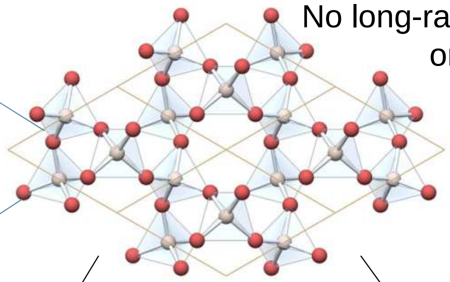
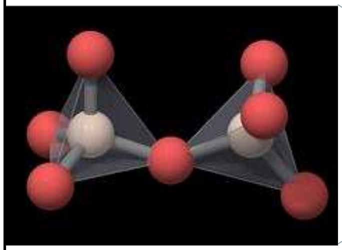
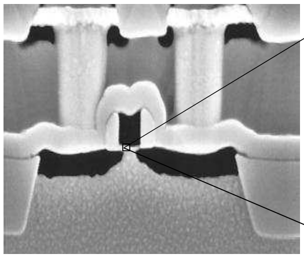
SiO and SiH Bonds

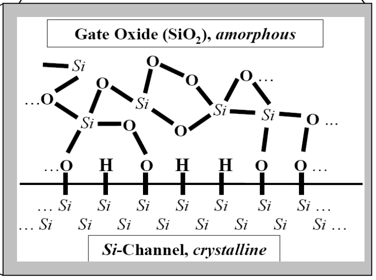


No long-range order

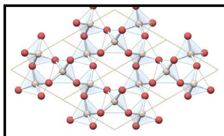


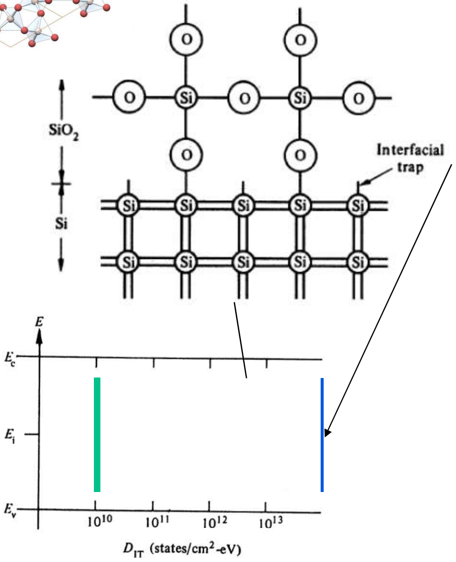
Local ordering tetrahedra

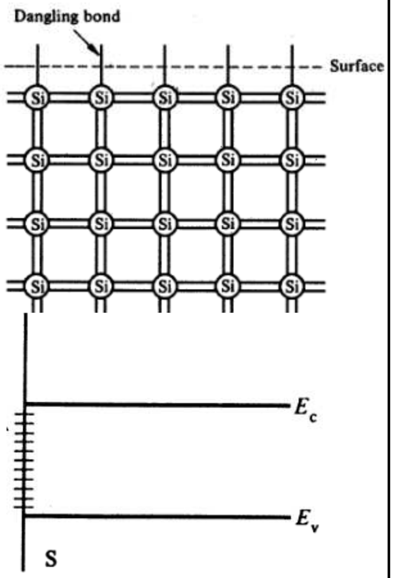




Interface States







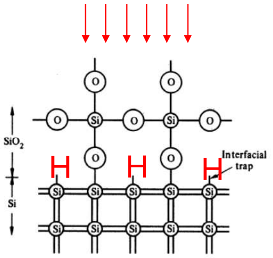
With annealing technology

Unpassivated bonds ~10^{10} cm^{-2}

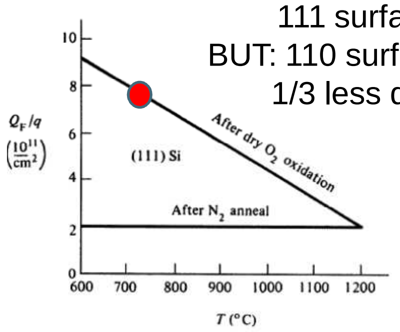
Unpassivated bonds ~10^{14} cm^{-2}

‘Annealing’ of Interface States

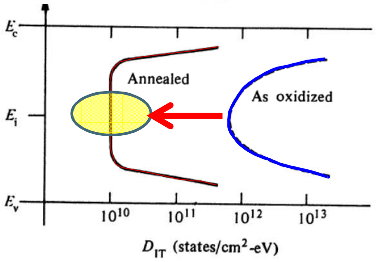
Forming gas anneal



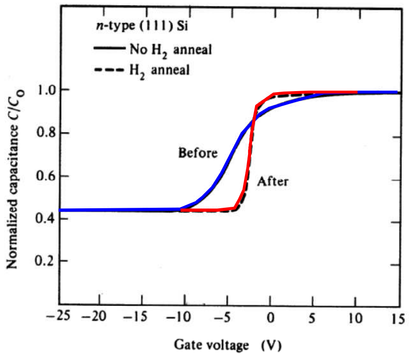
Good MOSFET requires about $10^{10}/cm^2$



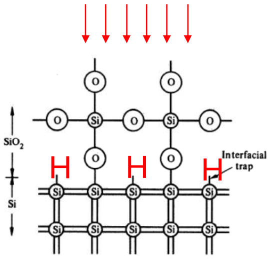
111 surface data
BUT: 110 surface has 1/3 less dangling bonds



C-V Stretch Out



Forming gas anneal



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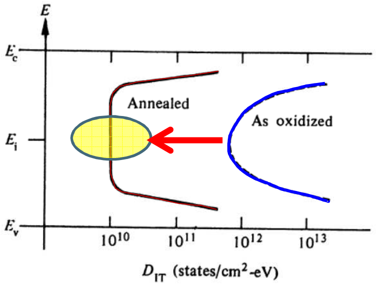
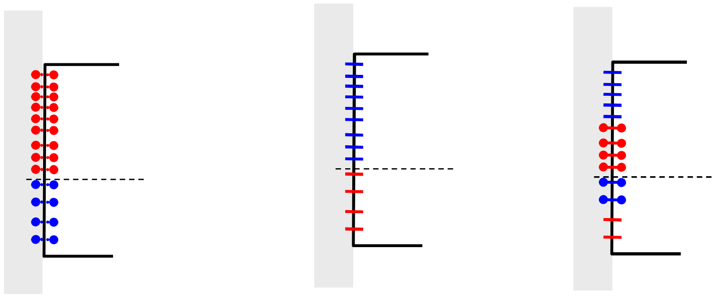


Nature of Donor and Acceptor Traps



Donor level
Positive when empty
Neutral when full

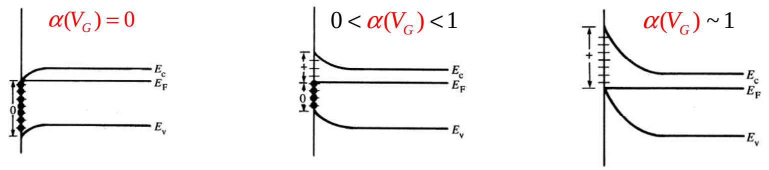
Acceptor level
Neutral when empty
Negative when full

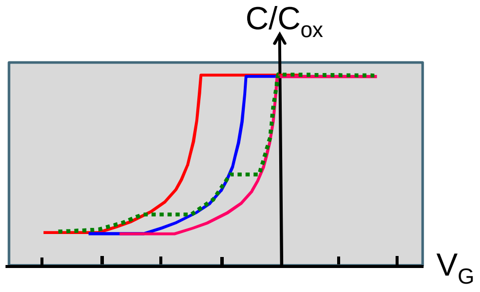
Combination when both are present

Now the surprising part:
Hydrogen passivation can act as a donor and as an acceptor leve
Depends on details of bond configuration

Donor like Interface States

$$V_{th} = V_{th}^* - \frac{1}{C_{ox}x_0}\int_0^{x_0} x\times\alpha(V_G)\times Q_{ox}(x)\delta(x-x_o)\,dx = V_{th}^* - \frac{\alpha(V_G)Q_{ox}(x_0)}{C_{ox}}$$

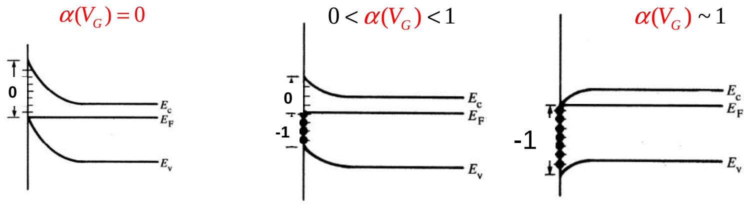


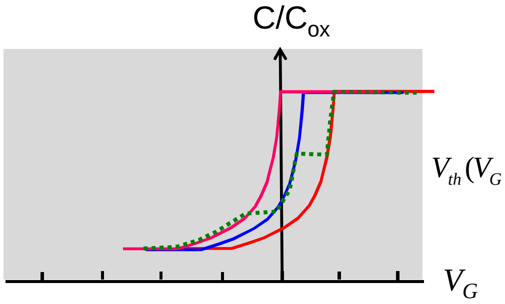


Assume the charges would NOT be voltage dependent
=> solid shift

BUT: charges change with voltage
=> smooth shift

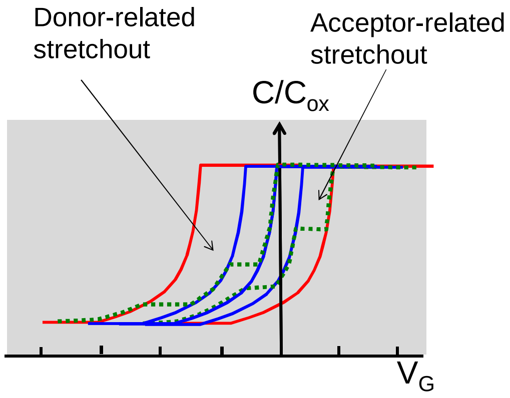
Acceptor like Interface States

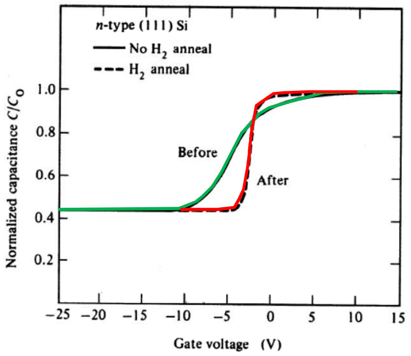




$$V_{th}(V_G)=V_{th}^{*}+\frac{\alpha(V_G)Q_{ox}(x_0)}{C_{ox}}$$

Acceptor and Donor Traps Combined





Summary

1) Non-ideal threshold characteristics are important consideration of MOSFET design.
2) The non-idealities arise from differences in gate and substrate work function, trapped charges, interface states.
3) Although nonindeal effects often arise from transistor degradation, there are many cases where these effects can be used to enhance desirable characteristics.