ECE606: Solid State Devices
Lecture 25
Modern MOSFETs

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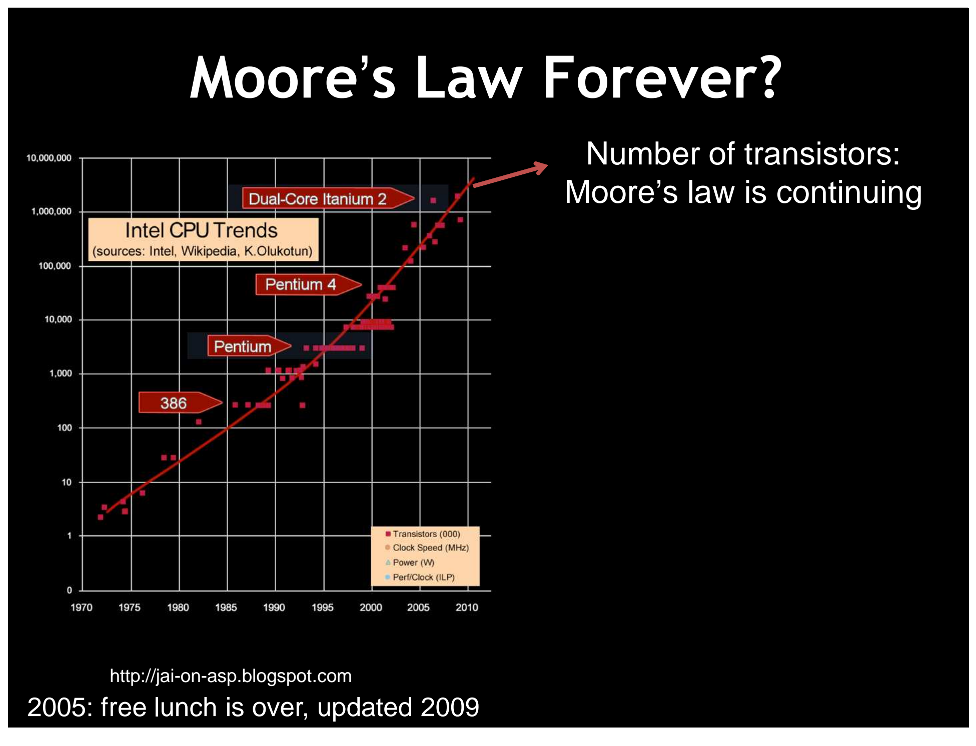
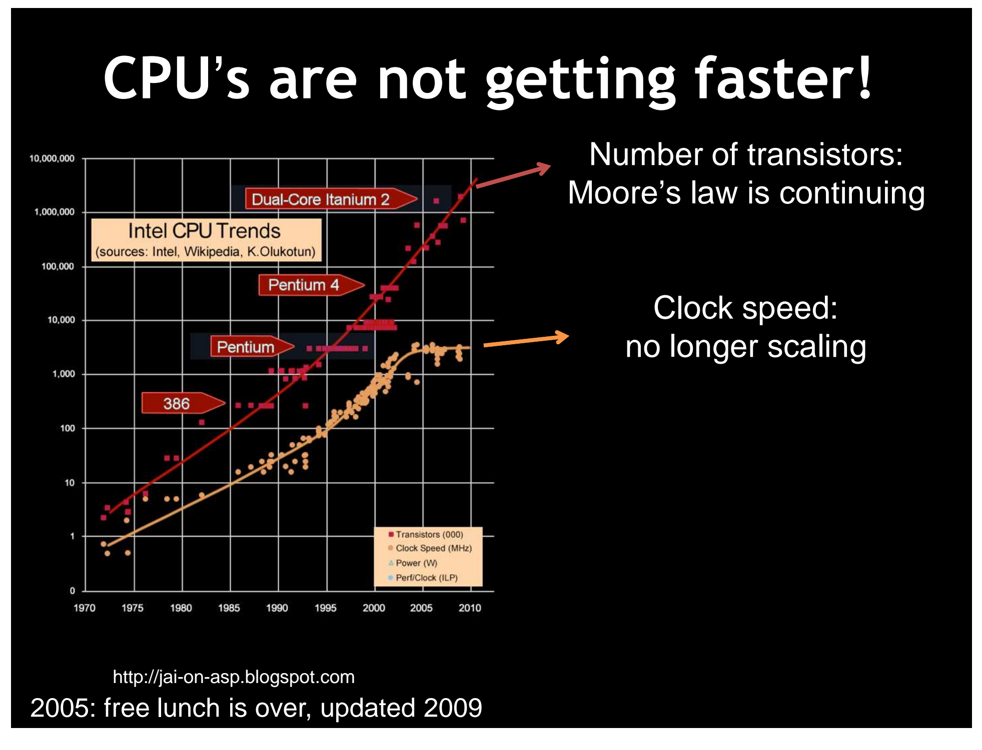
Topic Map

	Equilibrium	DC	Small signal	Large Signal	Circuits
Diode					
Schottky					
BJT/HBT					
MOSFET					


Moore's Law Forever?
Number of transistors:
Moore's law is continuing
Intel CPU Trends
(sources: Intel, Wikipedia, K.Olukotun)
Dual-Core Itanium 2
Pentium 4
Pentium
386
Transistors (000)
Clock Speed (MHz)
Power (W)
Perf/Clock (ILP)
http://jai-on-asp.blogspot.com
2005: free lunch is over, updated 2009


CPU's are not getting faster!
Number of transistors:
Moore's law is continuing
Clock speed:
no longer scaling
Intel CPU Trends
(sources: Intel, Wikipedia, K.Olukotun)
Dual-Core Itanium 2
Pentium 4
Pentium
386
Transistors (000)
Clock Speed (MHz)
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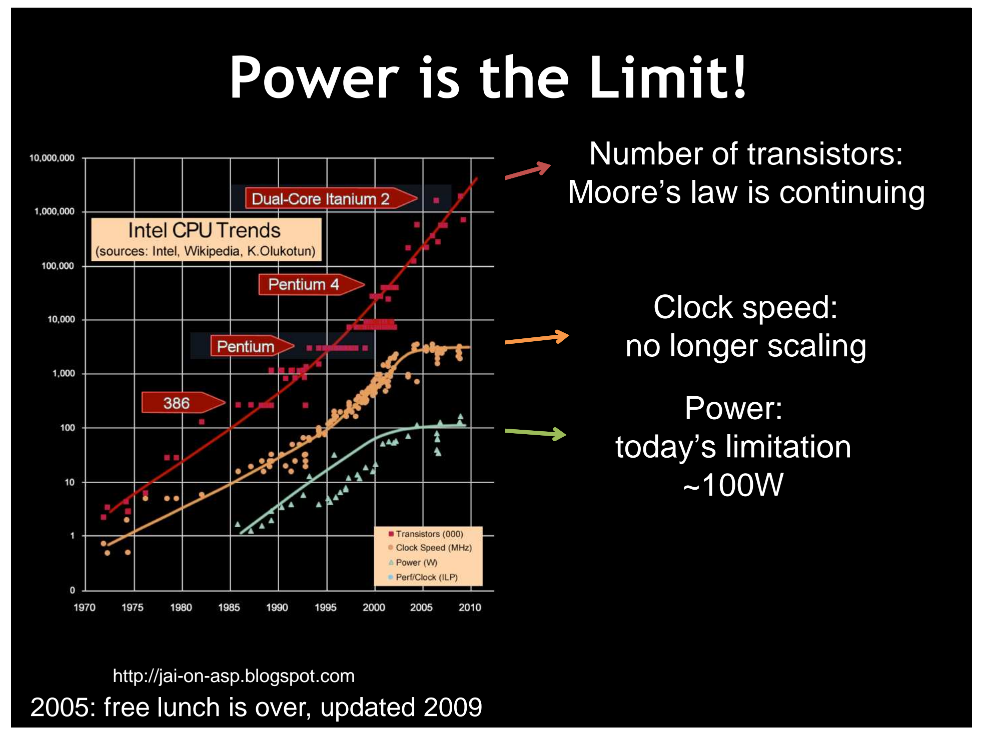
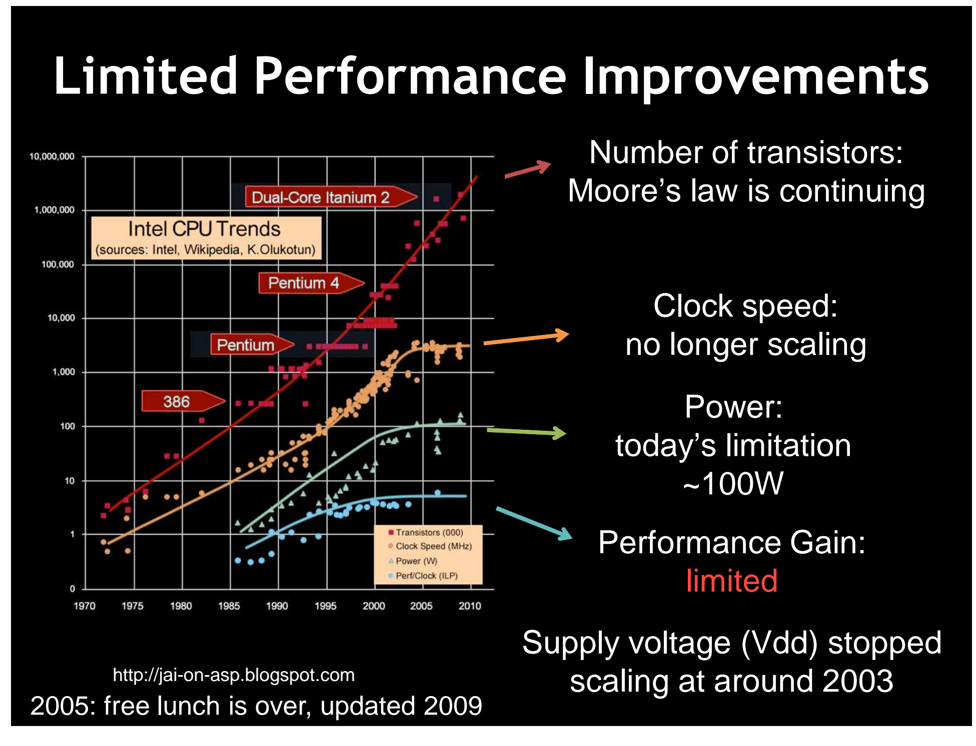
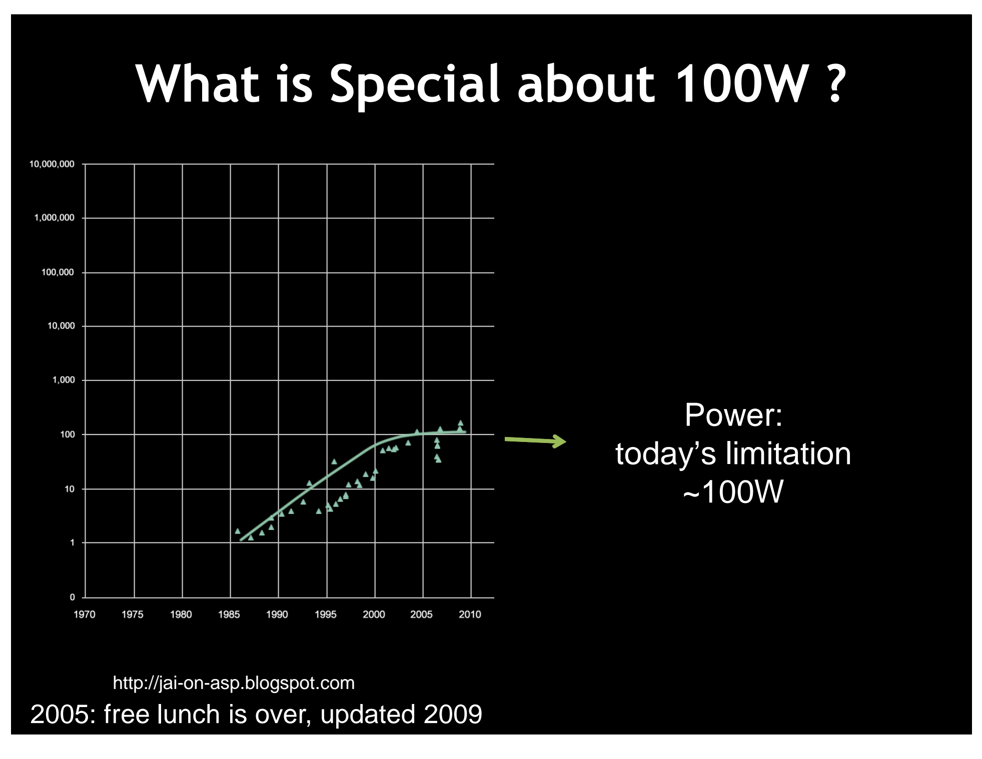
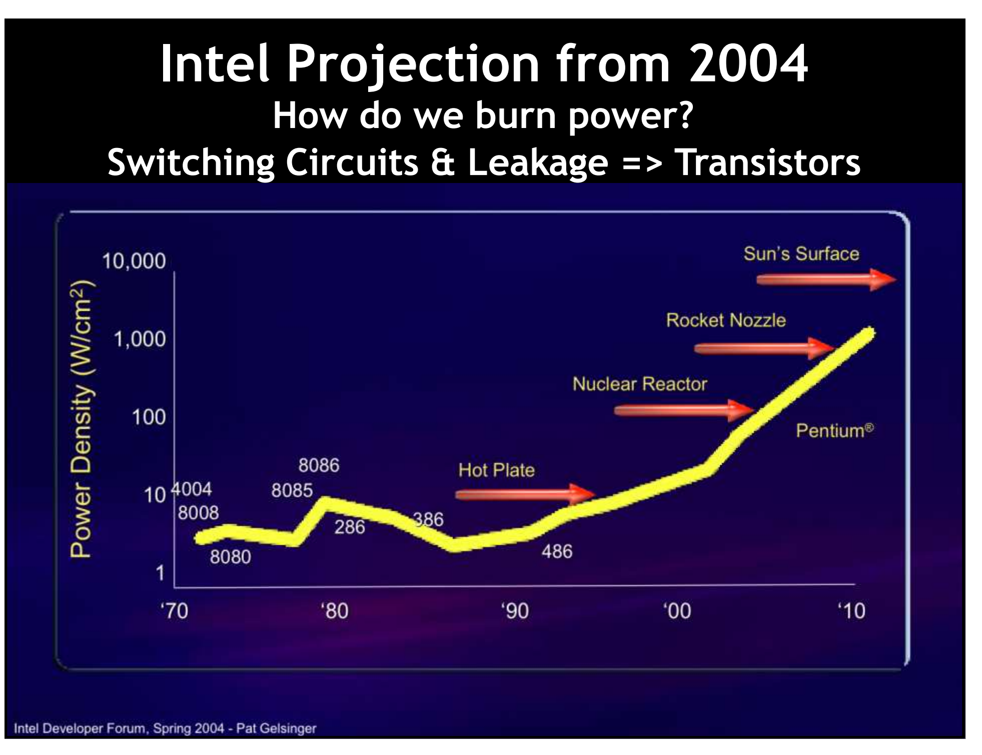
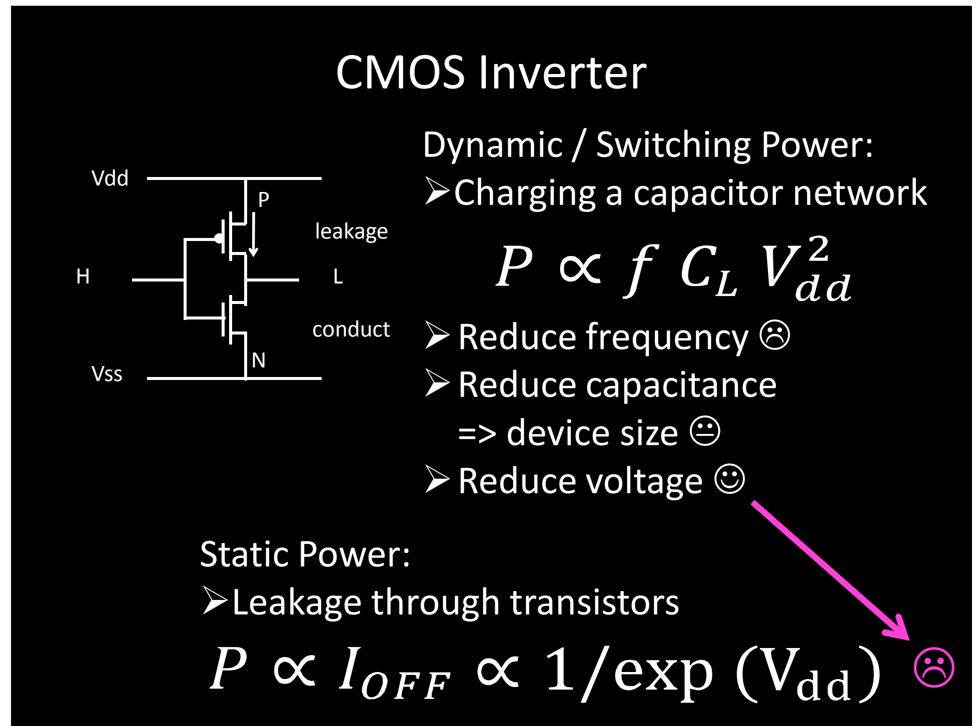
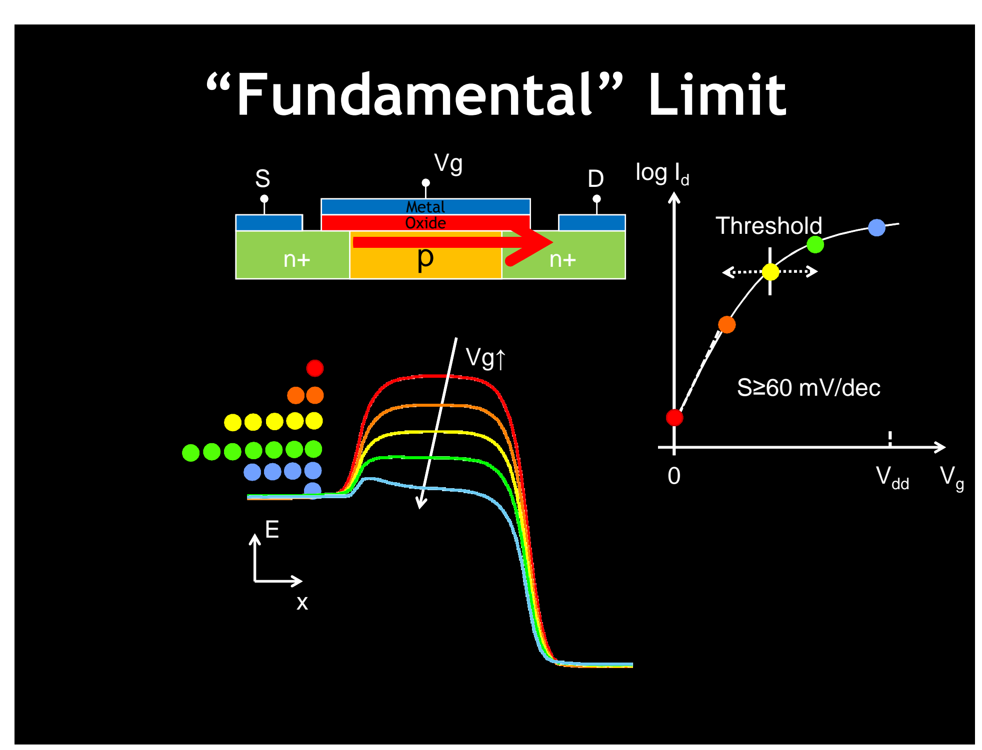

Power is the Limit!
Intel CPU Trends
(sources: Intel, Wikipedia, K.Olukotun)
Dual-Core Itanium 2
Pentium 4
Pentium
386
Transistors (000)
Clock Speed (MHz)
Power (W)
Perf/Clock (ILP)
Number of transistors:
Moore's law is continuing
Clock speed:
no longer scaling
Power:
today's limitation
~100W
http://jai-on-asp.blogspot.com
2005: free lunch is over, updated 2009

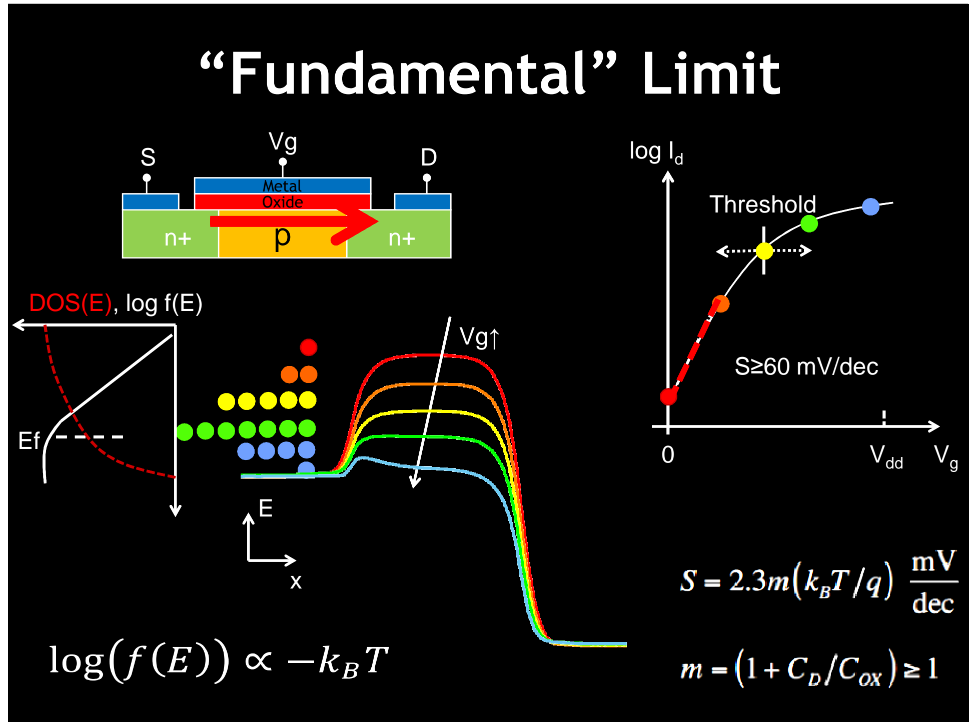

Limited Performance Improvements
Intel CPU Trends
(sources: Intel, Wikipedia, K.Olukotun)
Dual-Core Itanium 2
Pentium 4
Pentium
386
Transistors (000)
Clock Speed (MHz)
Power (W)
Perf/Clock (ILP)
Number of transistors:
Moore's law is continuing
Clock speed:
no longer scaling
Power:
today's limitation
~100W
Performance Gain:
limited
Supply voltage (Vdd) stopped
scaling at around 2003
http://jai-on-asp.blogspot.com
2005: free lunch is over, updated 2009


What is Special about 100W ?
10,000,000
1,000,000
100,000
10,000
1,000
100
10
1
0
1970
1975
1980
1985
1990
1995
2000
2005
2010
Power:
today's limitation
~100W
http://jai-on-asp.blogspot.com
2005: free lunch is over, updated 2009


Intel Projection from 2004
How do we burn power?
Switching Circuits & Leakage => Transistors
Power Density (W/cm²)
10,000
1,000
100
10
1
'70
'80
'90
'00
'10
4004
8008
8080
8085
8086
286
386
486
Pentium®
Hot Plate
Nuclear Reactor
Rocket Nozzle
Sun's Surface
Intel Developer Forum, Spring 2004 - Pat Gelsinger


CMOS Inverter
Vdd
P
leakage
H
L
conduct
N
Vss
Dynamic / Switching Power:
➢Charging a capacitor network
$P \propto f\, C_L\, V_{dd}^2$
➢ Reduce frequency ☹
➢ Reduce capacitance
=> device size 😐
➢ Reduce voltage ☺
Static Power:
➢Leakage through transistors
$P \propto I_{OFF} \propto 1/\exp\,(V_{dd})$ ☹


"Fundamental" Limit
S
Vg
D
Metal
Oxide
n+
p
n+
Vg↑
E
x
log I_d
Threshold
S≥60 mV/dec
0
V_{dd}
V_g

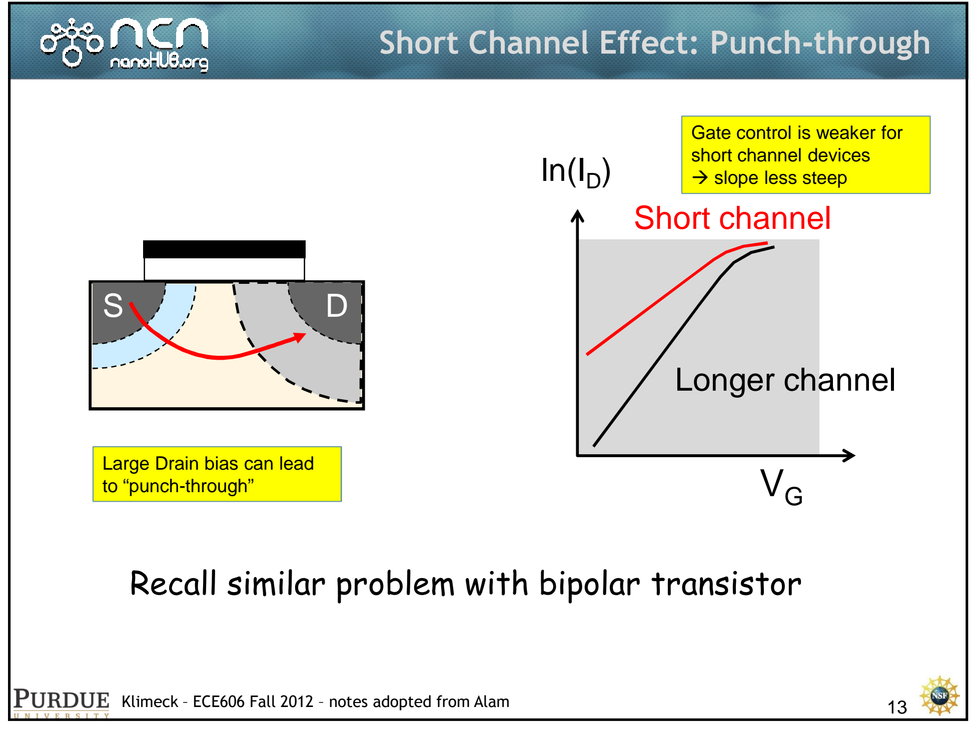


Outline

1. **Short channel effect**
2. Control of threshold voltage
3. Mobility enhancement
4. Conclusion

$$I_D = \frac{\mu C_{ox}}{L_{ch}} (V_G - V_{th}^{*})^2$$

REF: Chapter 19, SDF


Short Channel Effect: Punch-through
nanoHUB.org
S
D
Large Drain bias can lead to "punch-through"
ln(I_D)
Gate control is weaker for short channel devices → slope less steep
Short channel
Longer channel
V_G
Recall similar problem with bipolar transistor
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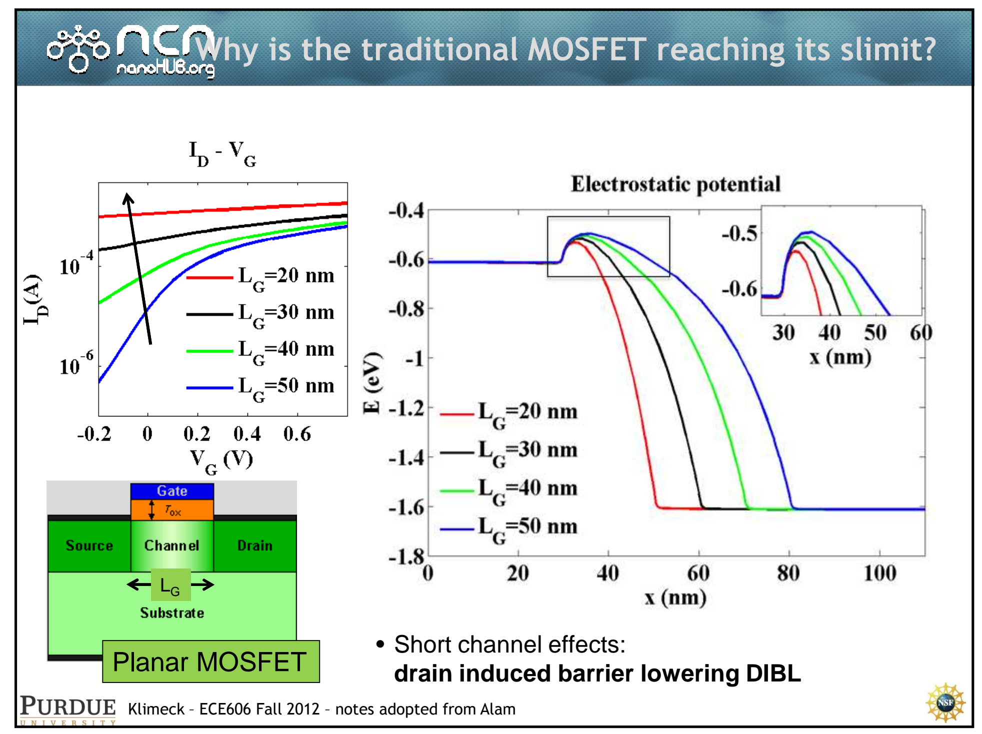
Why is the traditional MOSFET reaching its slimit?
nanoHUB.org
I_D - V_G
I_D(A)
10^-4
10^-6
L_G=20 nm
L_G=30 nm
L_G=40 nm
L_G=50 nm
-0.2
0
0.2
0.4
0.6
V_G (V)
Gate
T_ox
Source
Channel
Drain
L_G
Substrate
Planar MOSFET
Electrostatic potential
E (eV)
-0.4
-0.6
-0.8
-1
-1.2
-1.4
-1.6
-1.8
0
20
40
60
80
100
x (nm)
-0.5
-0.6
30
40
50
60
x (nm)
L_G=20 nm
L_G=30 nm
L_G=40 nm
L_G=50 nm
• Short channel effects:
drain induced barrier lowering DIBL
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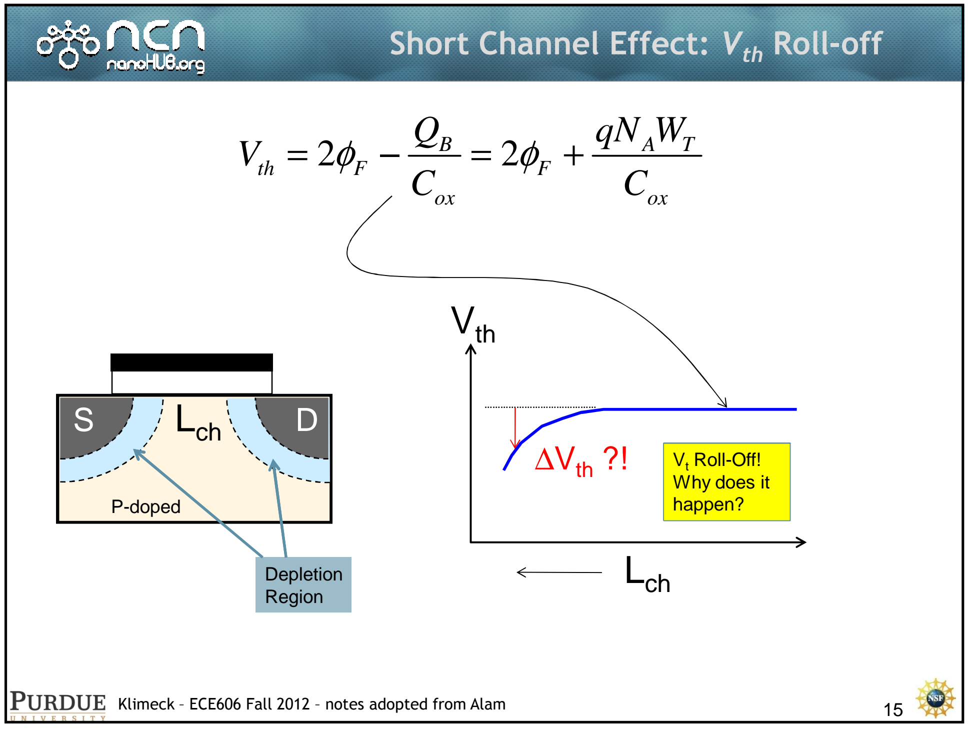
Short Channel Effect: V_{th} Roll-off
nanoHUB.org
$$V_{th} = 2\phi_F - \frac{Q_B}{C_{ox}} = 2\phi_F + \frac{qN_A W_T}{C_{ox}}$$
S
L_{ch}
D
P-doped
Depletion Region
V_{th}
ΔV_{th} ?!
V_t Roll-Off! Why does it happen?
L_{ch}
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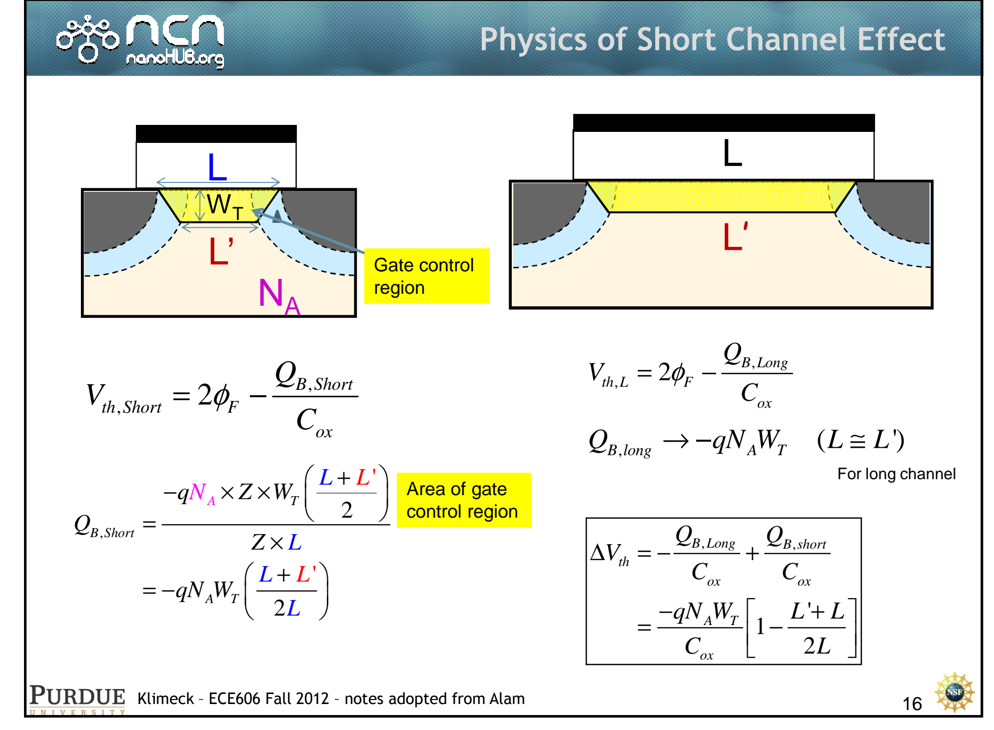
Physics of Short Channel Effect
nanoHUB.org
L
W_T
L'
N_A
Gate control region
L
L'
$$V_{th,Short} = 2\phi_F - \frac{Q_{B,Short}}{C_{ox}}$$
$$Q_{B,Short} = \frac{-qN_A \times Z \times W_T \left(\frac{L+L'}{2}\right)}{Z \times L} = -qN_A W_T \left(\frac{L+L'}{2L}\right)$$
Area of gate control region
$$V_{th,L} = 2\phi_F - \frac{Q_{B,Long}}{C_{ox}}$$
$$Q_{B,long} \to -qN_A W_T \quad (L \cong L')$$
For long channel
$$\Delta V_{th} = -\frac{Q_{B,Long}}{C_{ox}} + \frac{Q_{B,short}}{C_{ox}} = \frac{-qN_A W_T}{C_{ox}}\left[1 - \frac{L'+L}{2L}\right]$$
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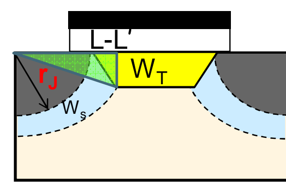
Short Channel Effect

Calculate L' (geometry exercise)

$$(r_J + W_S)^2 = W_T^2 + \left(r_J + \frac{L - L'}{2} \right)^2$$

$$L' = L - 2r_J \left(\sqrt{1 + \frac{2W_T}{r_J}} - 1 \right)$$



r_j junction curvature

Minimize L'

$$\Delta V_{th} = \frac{-qN_A W_T}{C_{ox}} \left[1 - \frac{L' + L}{2L} \right]$$

$$= \frac{-qN_A W_T}{C_{ox}} \frac{r_J}{L} \left(\sqrt{1 + \frac{2W_T}{r_J}} - 1 \right) = \alpha_0$$ Minimum acceptable …

Minimize r_j

How to reduce V_{th} roll-off …

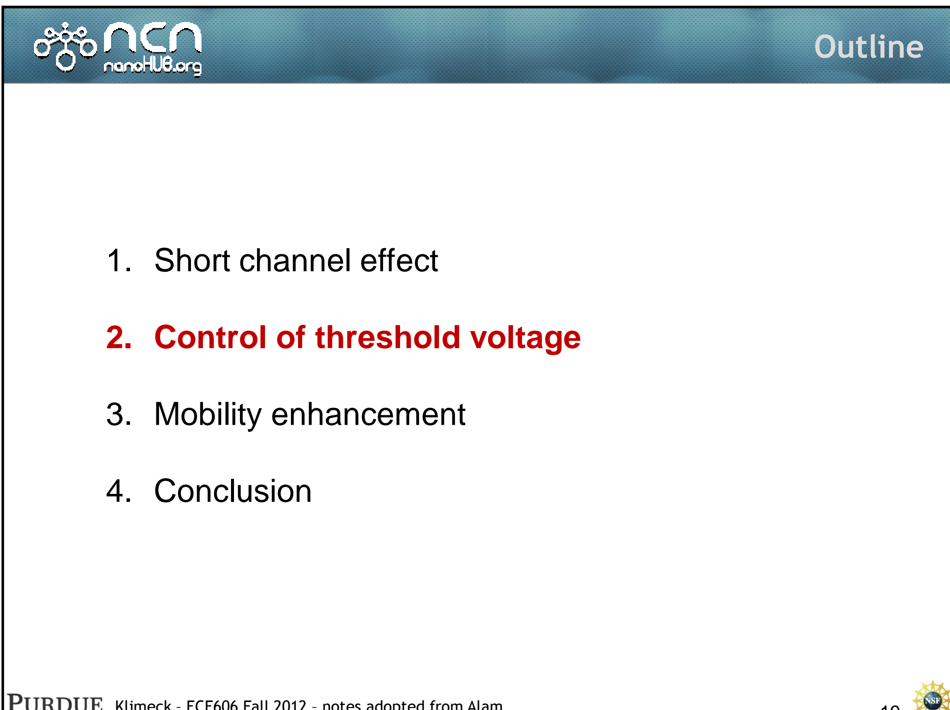
Shallow junction/geometry of transistors
laser annealing of junctions, FINFETs

Reduced substrate doping N_A
consider W_T and junction breakdown

$$L_{min} = \frac{qN_A W_T}{C_{ox}} \frac{r_J}{\alpha_0} \left(\sqrt{1 + \frac{2W_T}{r_J}} - 1 \right)$$

V_{th}, α_0, L_{min}, L_{ch}

Thinner gate oxides
Consider tunneling current
Higher gate dielectric
Consider bulk traps


nanoHUB.org
Outline
1. Short channel effect
2. Control of threshold voltage
3. Mobility enhancement
4. Conclusion
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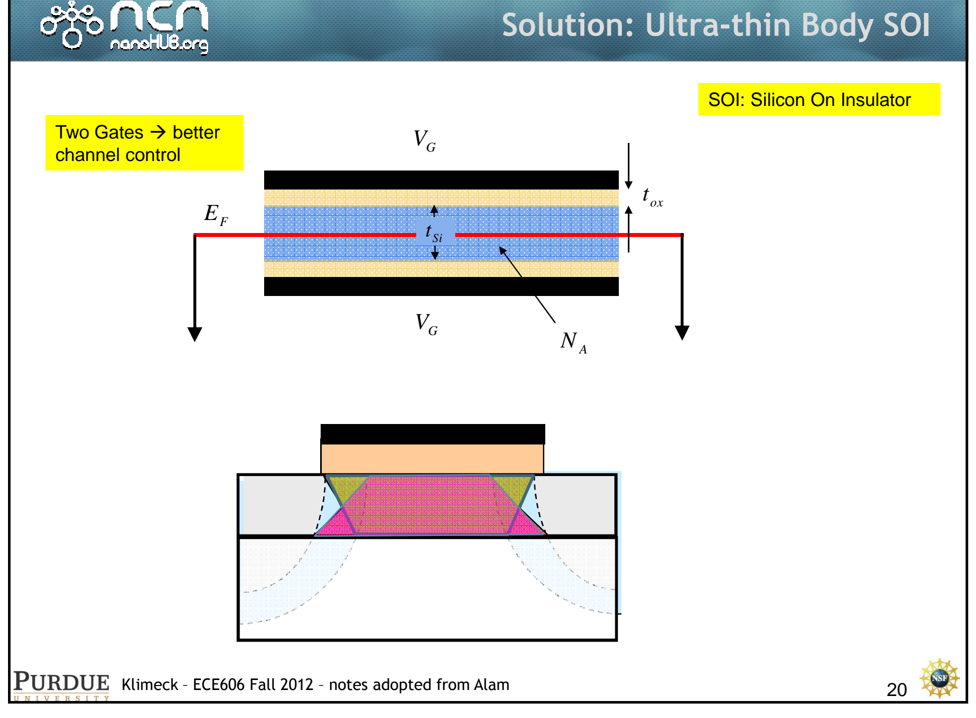
nanoHUB.org
Solution: Ultra-thin Body SOI
SOI: Silicon On Insulator
Two Gates → better channel control
V_G
t_{ox}
E_F
t_{Si}
V_G
N_A
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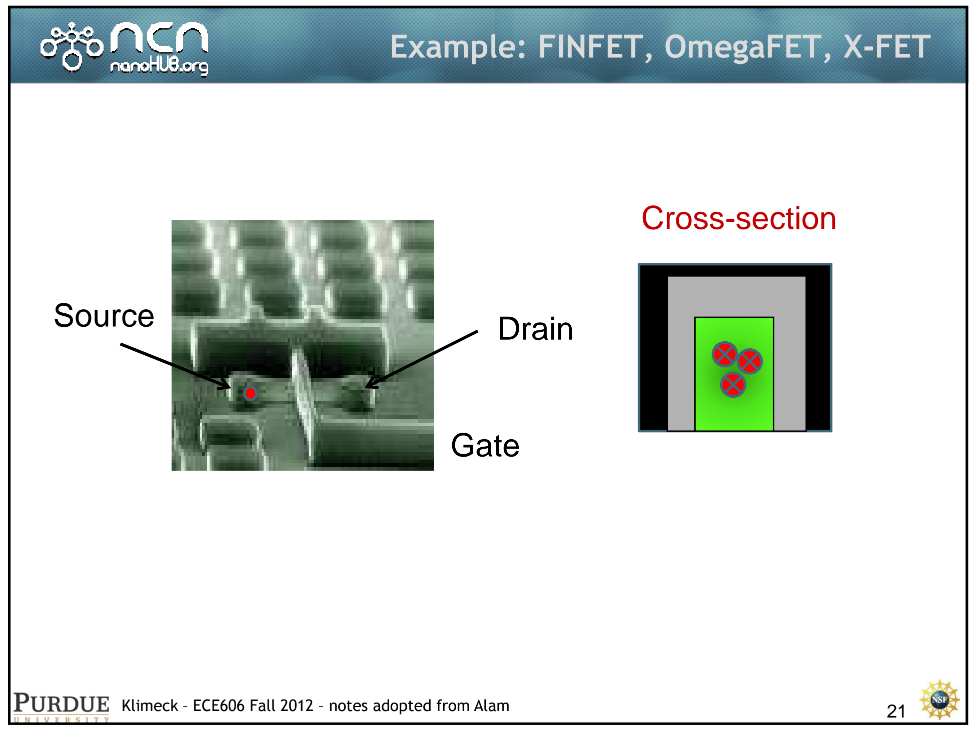
nanoHUB.org
Example: FINFET, OmegaFET, X-FET
Source
Drain
Gate
Cross-section
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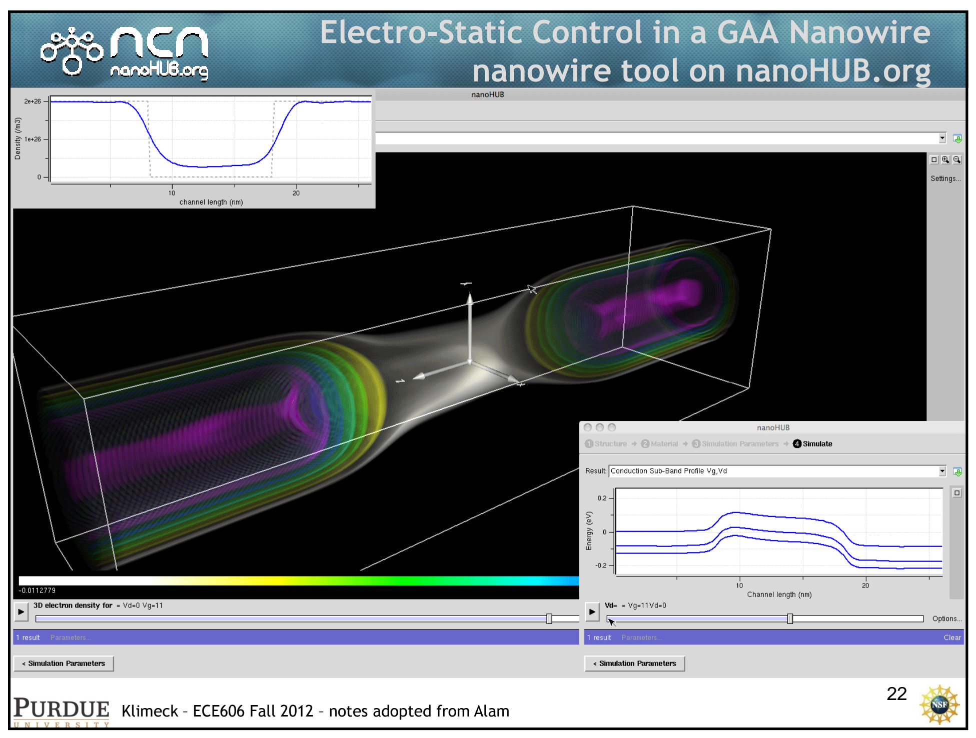
nanoHUB.org
Electro-Static Control in a GAA Nanowire
nanowire tool on nanoHUB.org
channel length (nm)
Conduction Sub-Band Profile Vg,Vd
Channel length (nm)
Energy (eV)
3D electron density for
Simulation Parameters
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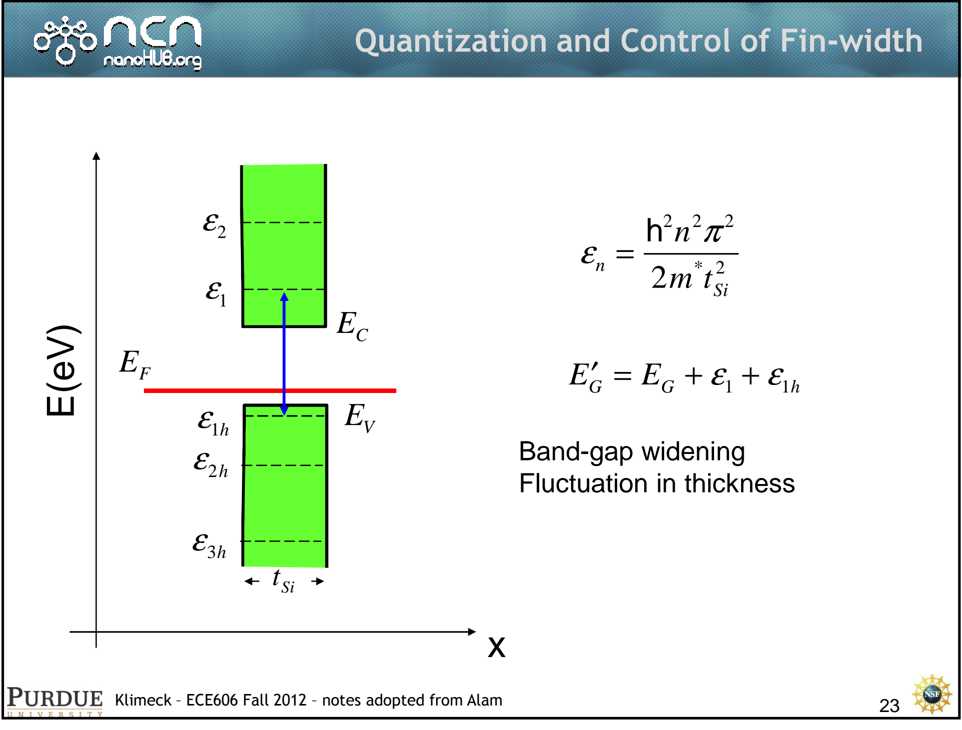
Quantization and Control of Fin-width
E(eV)
ε_2
ε_1
E_C
E_F
E_V
ε_{1h}
ε_{2h}
ε_{3h}
t_{Si}
x
$$\varepsilon_n = \frac{\hbar^2 n^2 \pi^2}{2m^* t_{Si}^2}$$
$$E'_G = E_G + \varepsilon_1 + \varepsilon_{1h}$$
Band-gap widening
Fluctuation in thickness
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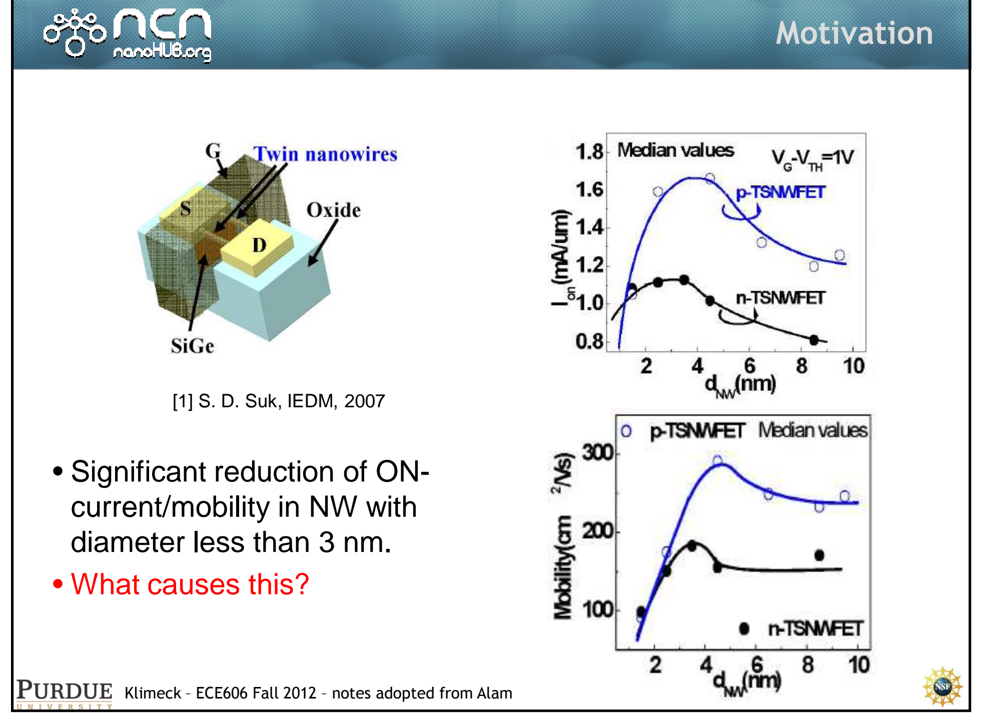
Motivation
G
Twin nanowires
S
Oxide
D
SiGe
[1] S. D. Suk, IEDM, 2007
• Significant reduction of ON-current/mobility in NW with diameter less than 3 nm.
• What causes this?
Median values
V_G-V_{TH}=1V
p-TSNWFET
n-TSNWFET
I_{on} (mA/um)
d_{NW}(nm)
Mobility(cm²/Vs)
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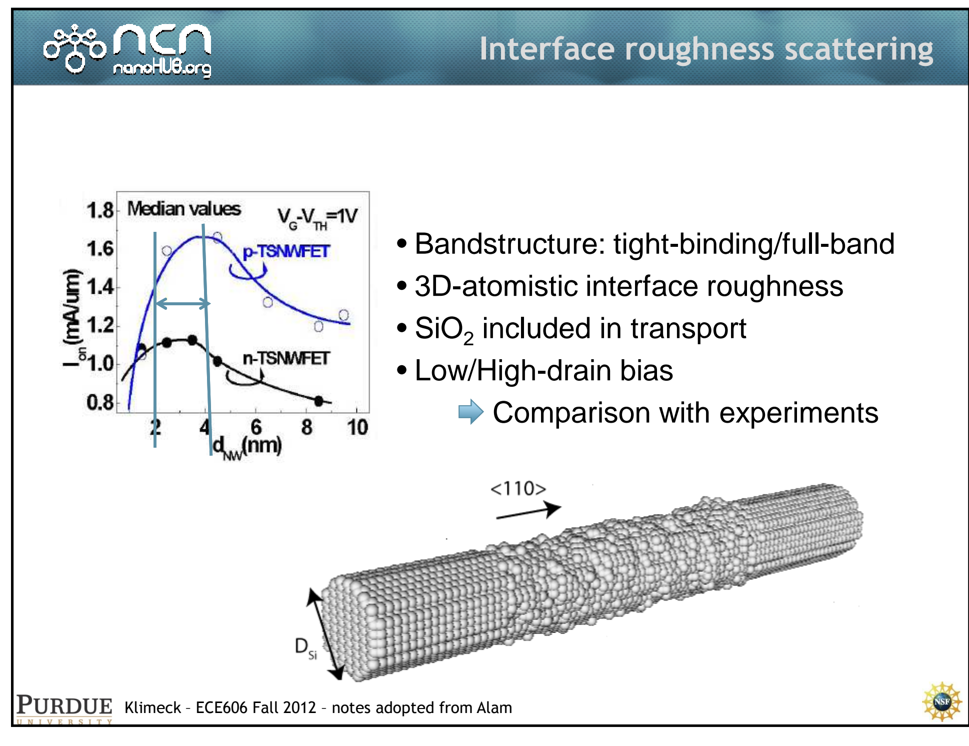
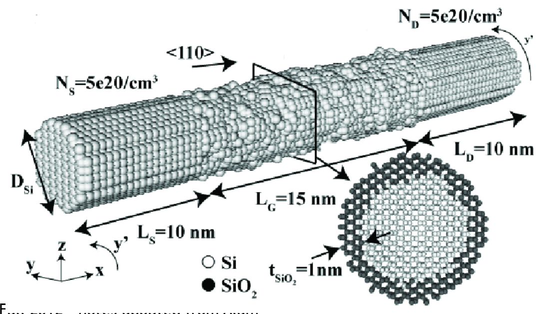
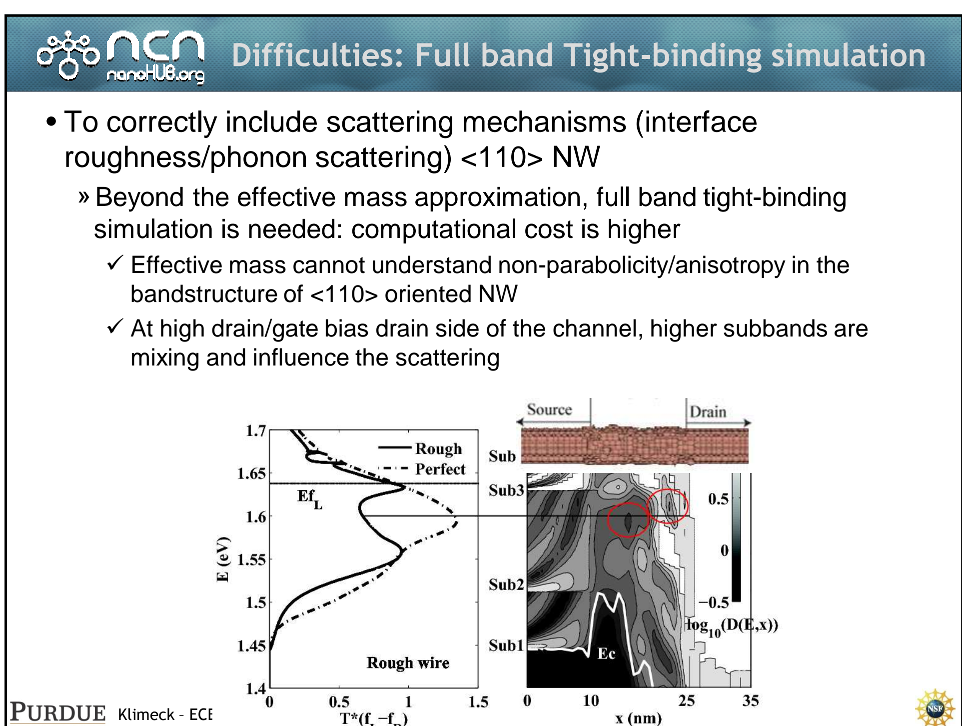


Difficulties: Interface roughness scattering

- Realistic/atomistic rough interface between Si/SiO_2
  - » Adapt experimentally generated statistical function: How do we know the generated interface roughness is correct?
  - » Many statistical samples needed: computational cost high
  - » Electrons may penetrate into the SiO_2 region. How do we count it?
  - » Computational cost increases as we take into account SiO_2 in tight-binding approximation.





nanoHUB.org
Difficulties: Full band Tight-binding simulation
• To correctly include scattering mechanisms (interface roughness/phonon scattering) <110> NW
» Beyond the effective mass approximation, full band tight-binding simulation is needed: computational cost is higher
✓ Effective mass cannot understand non-parabolicity/anisotropy in the bandstructure of <110> oriented NW
✓ At high drain/gate bias drain side of the channel, higher subbands are mixing and influence the scattering
Rough
Perfect
Ef_L
Rough wire
E (eV)
T*(f_L −f_R)
Source
Drain
Sub
Sub3
Sub2
Sub1
Ec
log10(D(E,x))
x (nm)
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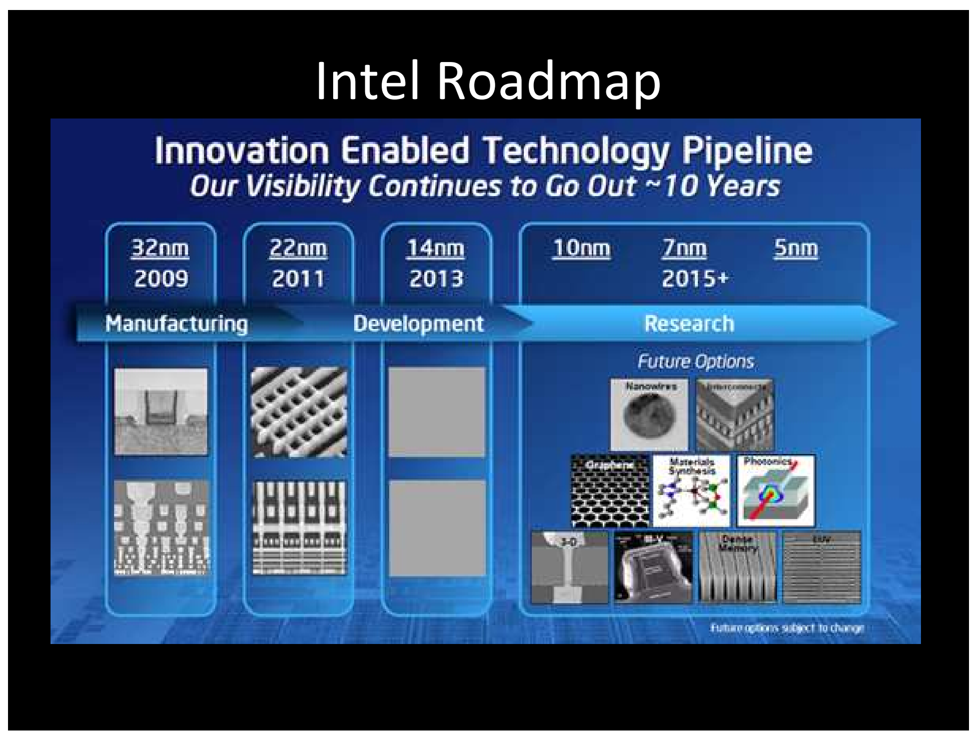
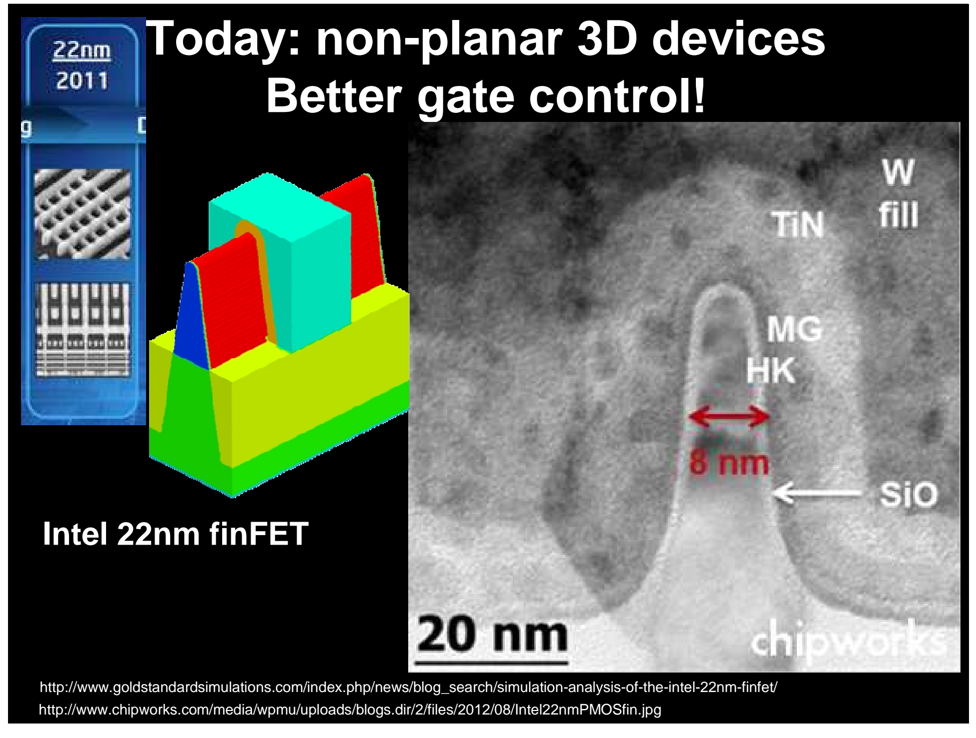
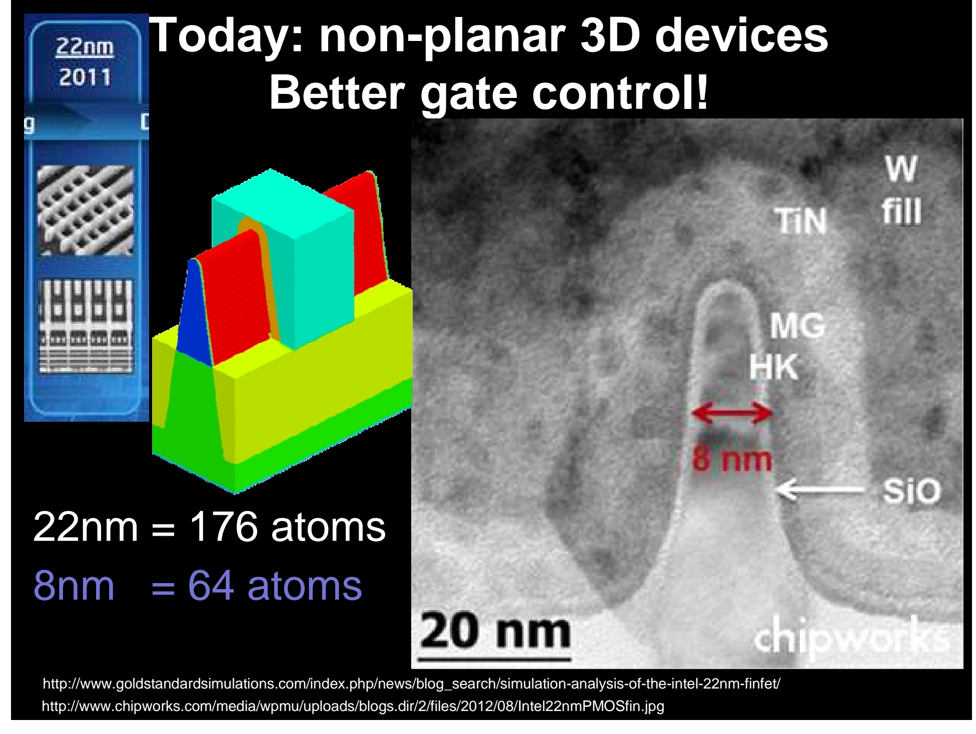
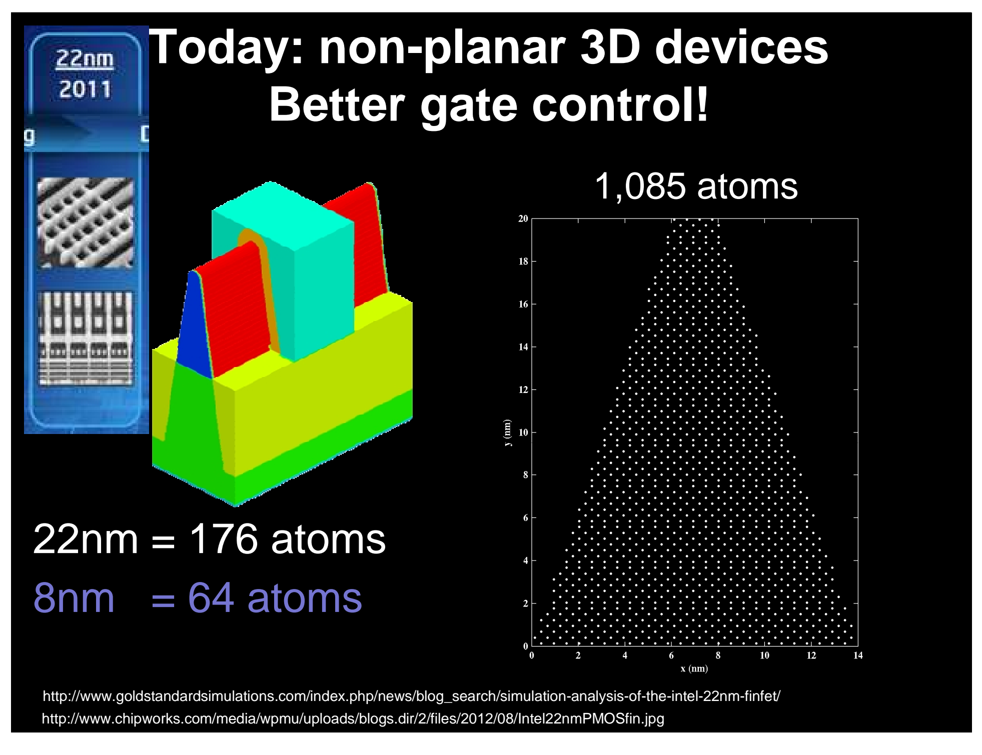
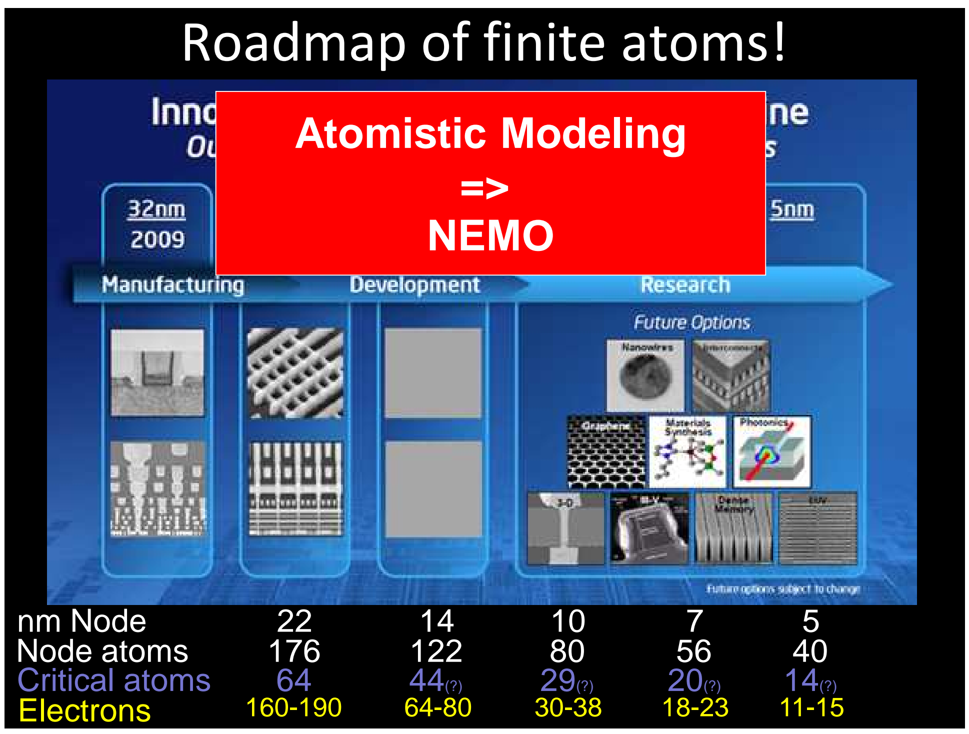


Intel Roadmap
Innovation Enabled Technology Pipeline
Our Visibility Continues to Go Out ~10 Years
32nm 2009
22nm 2011
14nm 2013
10nm
7nm 2015+
5nm
Manufacturing
Development
Research
Future Options
Future options subject to change


Today: non-planar 3D devices
Better gate control!
22nm
2011
W
fill
TiN
MG
HK
8 nm
SiO
Intel 22nm finFET
20 nm
chipworks
http://www.goldstandardsimulations.com/index.php/news/blog_search/simulation-analysis-of-the-intel-22nm-finfet/
http://www.chipworks.com/media/wpmu/uploads/blogs.dir/2/files/2012/08/Intel22nmPMOSfin.jpg

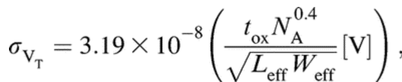

Today: non-planar 3D devices
Better gate control!
22nm
2011
W
fill
TiN
MG
HK
8 nm
SiO
22nm = 176 atoms
8nm = 64 atoms
20 nm
chipworks
http://www.goldstandardsimulations.com/index.php/news/blog_search/simulation-analysis-of-the-intel-22nm-finfet/
http://www.chipworks.com/media/wpmu/uploads/blogs.dir/2/files/2012/08/Intel22nmPMOSfin.jpg


Today: non-planar 3D devices
Better gate control!
22nm
2011
1,085 atoms
22nm = 176 atoms
8nm = 64 atoms
x (nm)
y (nm)
http://www.goldstandardsimulations.com/index.php/news/blog_search/simulation-analysis-of-the-intel-22nm-finfet/
http://www.chipworks.com/media/wpmu/uploads/blogs.dir/2/files/2012/08/Intel22nmPMOSfin.jpg

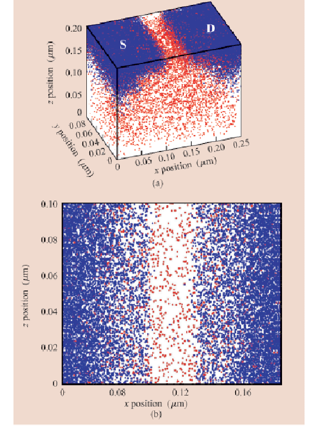

Roadmap of finite atoms!
Atomistic Modeling
=>
NEMO
32nm
2009
5nm
Manufacturing
Development
Research
Future Options
Nanowires
Graphene
Materials Synthesis
Photonics
3-D
III-V
Dense Memory
EUV
Future options subject to change
nm Node 22 14 10 7 5
Node atoms 176 122 80 56 40
Critical atoms 64 44(?) 29(?) 20(?) 14(?)
Electrons 160-190 64-80 30-38 18-23 11-15

Variability in Vth at Low Doping

$$V_{th} = 2\phi_F - \frac{Q_B}{C_{ox}} = 2\phi_F - \frac{qN_D W_T}{C_{ox}}$$



$$\sigma_{V_T} = 3.19 \times 10^{-8} \left(\frac{t_{ox} N_A^{0.4}}{\sqrt{L_{eff} W_{eff}}} [\mathrm{V}] \right),$$



Variation of V_T in short channel devices

Stronger effect of dopant number fluctuations on V_T

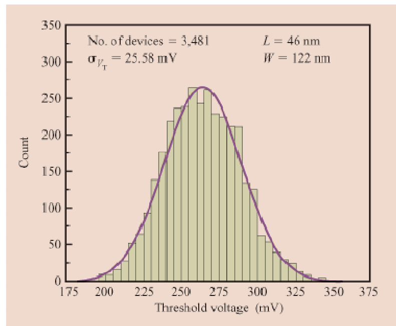


Figure 2

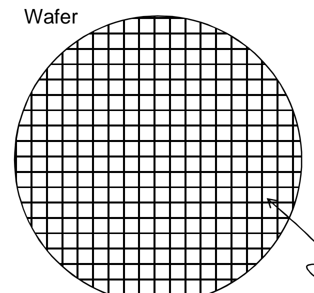
Threshold voltage histogram for FETs in the 90-nm-technology node.

IBM Journal of Res. And Tech. 2003.

Variability in Threshold Voltage

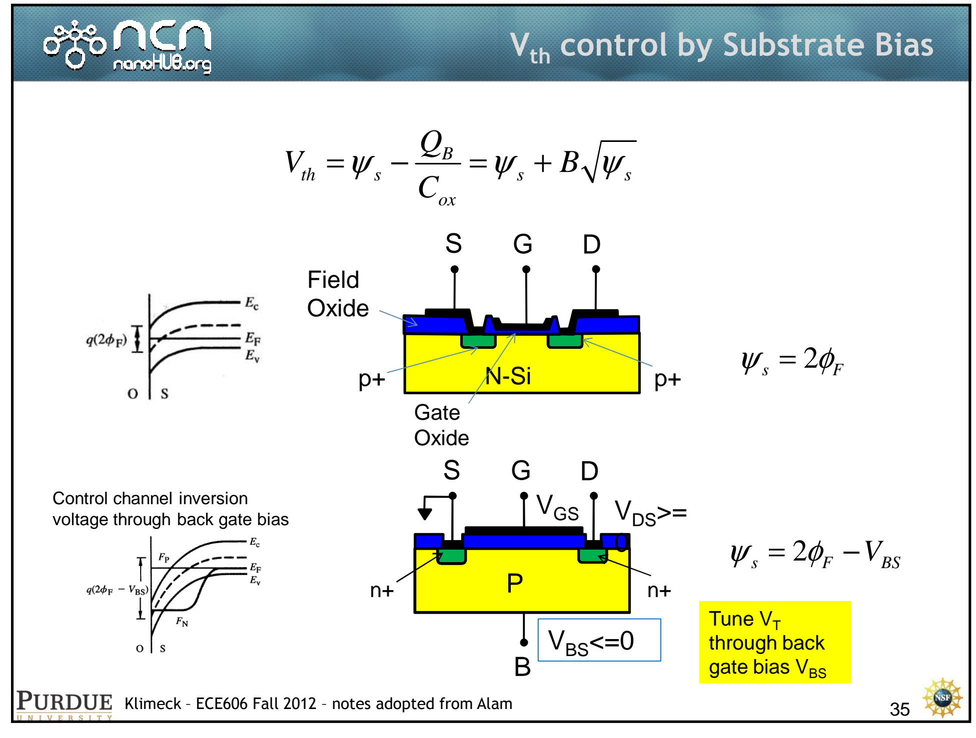
$$V_{th} = 2\phi_F - \frac{Q_B}{C_{ox}} = 2\phi_F - \frac{qN_A W_T}{C_{ox}}$$

$$\sigma_{V_T} = 3.19 \times 10^{-8} \left(\frac{t_{ox} N_A^{0.4}}{\sqrt{L_{eff} W_{eff}}} [\mathrm{V}] \right),$$



$$I_D = \frac{\mu C_{ox}}{L_{ch}} (V_G - V_{th}^*)^2$$

If every transistor has different V_{th} and therefore different current, circuit design becomes difficult


Vth control by Substrate Bias
$V_{th} = \psi_s - \frac{Q_B}{C_{ox}} = \psi_s + B\sqrt{\psi_s}$
S G D
Field Oxide
p+
N-Si
p+
Gate Oxide
$\psi_s = 2\phi_F$
S G D
Control channel inversion voltage through back gate bias
V_{GS}
V_{DS}>=
n+
P
n+
V_{BS}<=0
B
$\psi_s = 2\phi_F - V_{BS}$
Tune V_T through back gate bias V_{BS}
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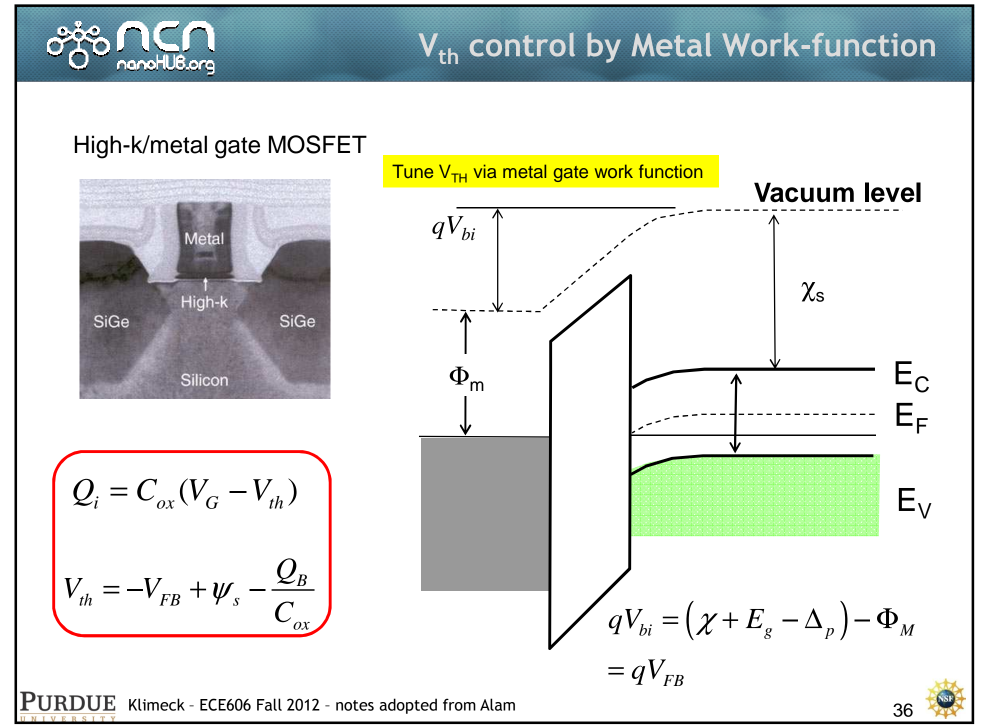
Vth control by Metal Work-function
High-k/metal gate MOSFET
Metal
High-k
SiGe
SiGe
Silicon
Tune V_{TH} via metal gate work function
Vacuum level
qV_{bi}
χ_s
Φ_m
E_C
E_F
E_V
$Q_i = C_{ox}(V_G - V_{th})$
$V_{th} = -V_{FB} + \psi_s - \frac{Q_B}{C_{ox}}$
$qV_{bi} = (\chi + E_g - \Delta_p) - \Phi_M = qV_{FB}$
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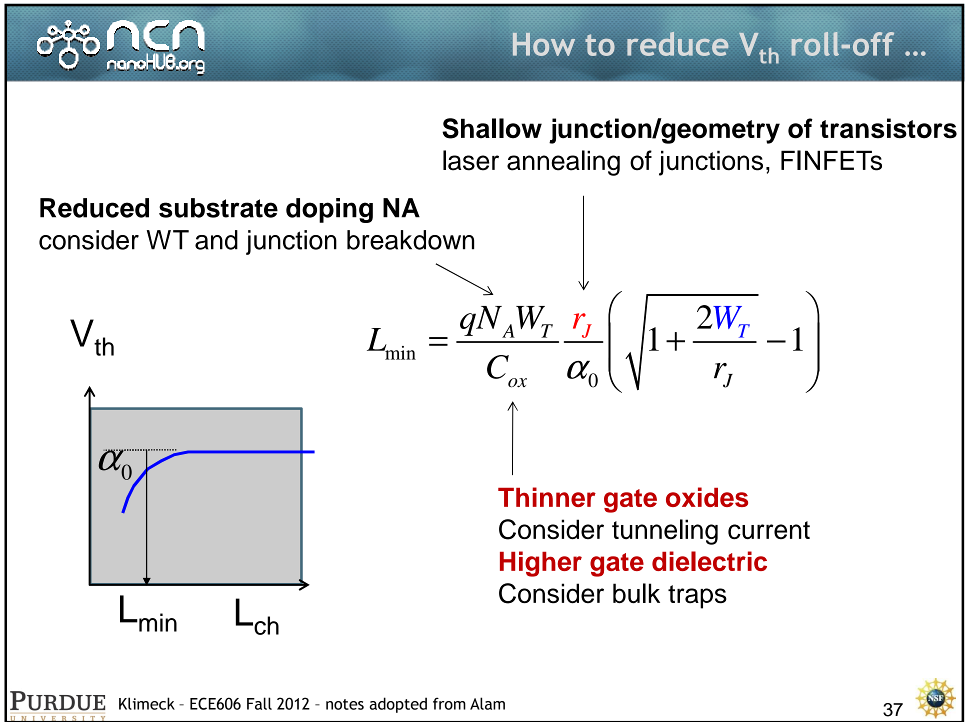

How to reduce V_{th} roll-off …
Shallow junction/geometry of transistors
laser annealing of junctions, FINFETs
Reduced substrate doping NA
consider WT and junction breakdown
V_{th}
α_0
L_{min}
L_{ch}
$L_{min} = \frac{qN_A W_T}{C_{ox}} \frac{r_J}{\alpha_0} \left(\sqrt{1 + \frac{2W_T}{r_J}} - 1 \right)$
Thinner gate oxides
Consider tunneling current
Higher gate dielectric
Consider bulk traps
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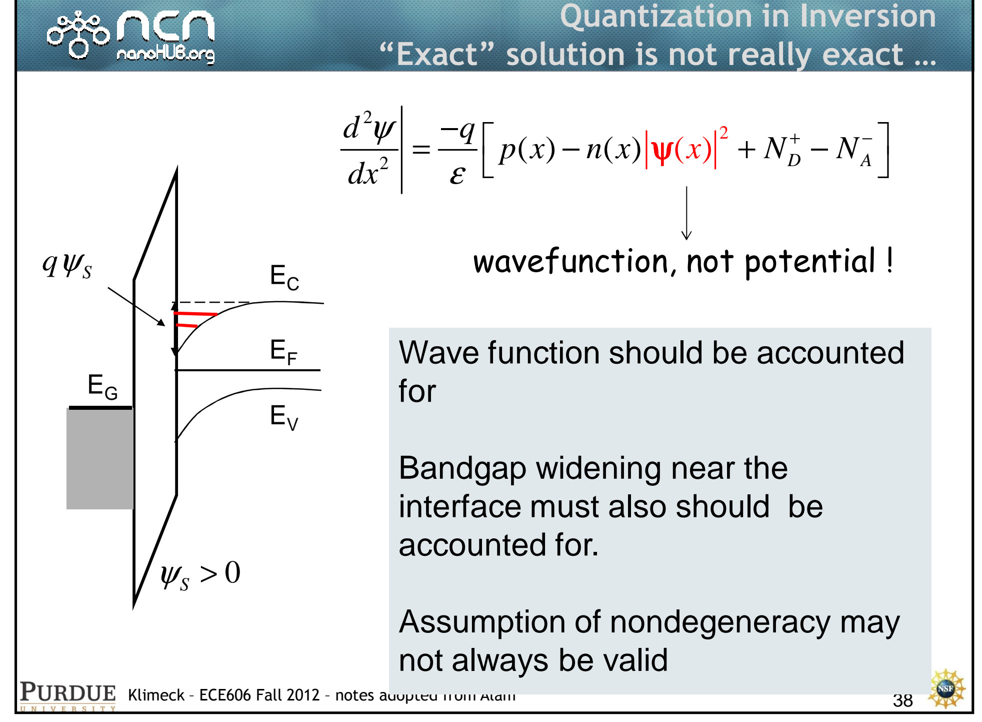

Quantization in Inversion
"Exact" solution is not really exact …
$\left.\frac{d^2\psi}{dx^2}\right| = \frac{-q}{\varepsilon}\left[p(x) - n(x)\left|\psi(x)\right|^2 + N_D^+ - N_A^- \right]$
wavefunction, not potential !
$q\psi_S$
E_C
E_F
E_G
E_V
$\psi_S > 0$
Wave function should be accounted for
Bandgap widening near the interface must also should be accounted for.
Assumption of nondegeneracy may not always be valid
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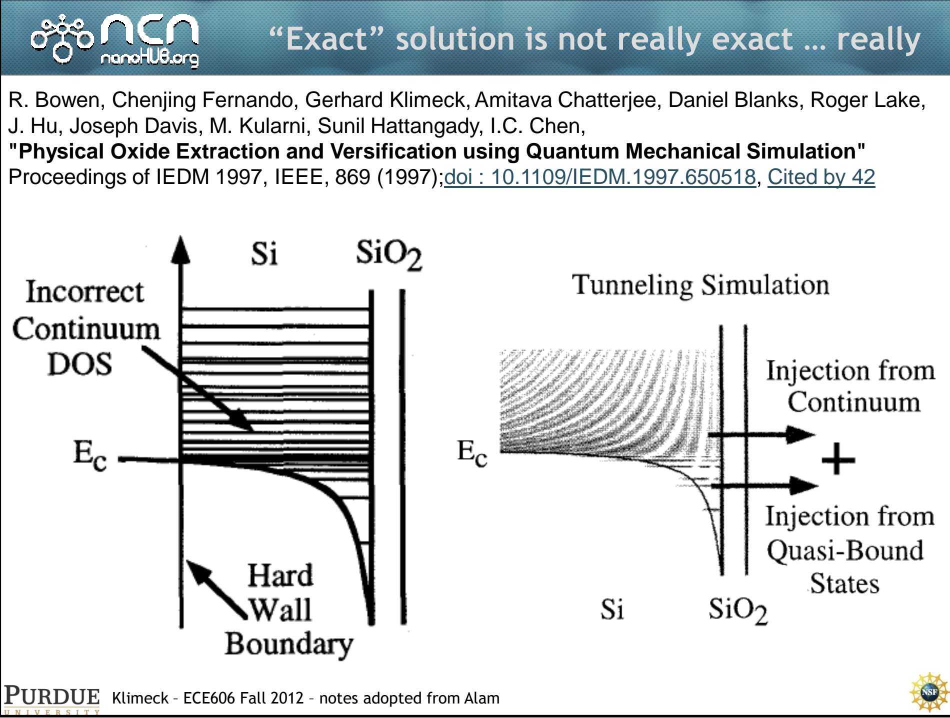

“Exact” solution is not really exact … really
R. Bowen, Chenjing Fernando, Gerhard Klimeck, Amitava Chatterjee, Daniel Blanks, Roger Lake, J. Hu, Joseph Davis, M. Kularni, Sunil Hattangady, I.C. Chen,
"Physical Oxide Extraction and Versification using Quantum Mechanical Simulation"
Proceedings of IEDM 1997, IEEE, 869 (1997);doi : 10.1109/IEDM.1997.650518, Cited by 42
Si
SiO2
Incorrect Continuum DOS
Ec
Hard Wall Boundary
Tunneling Simulation
Injection from Continuum
+
Injection from Quasi-Bound States
Si
SiO2
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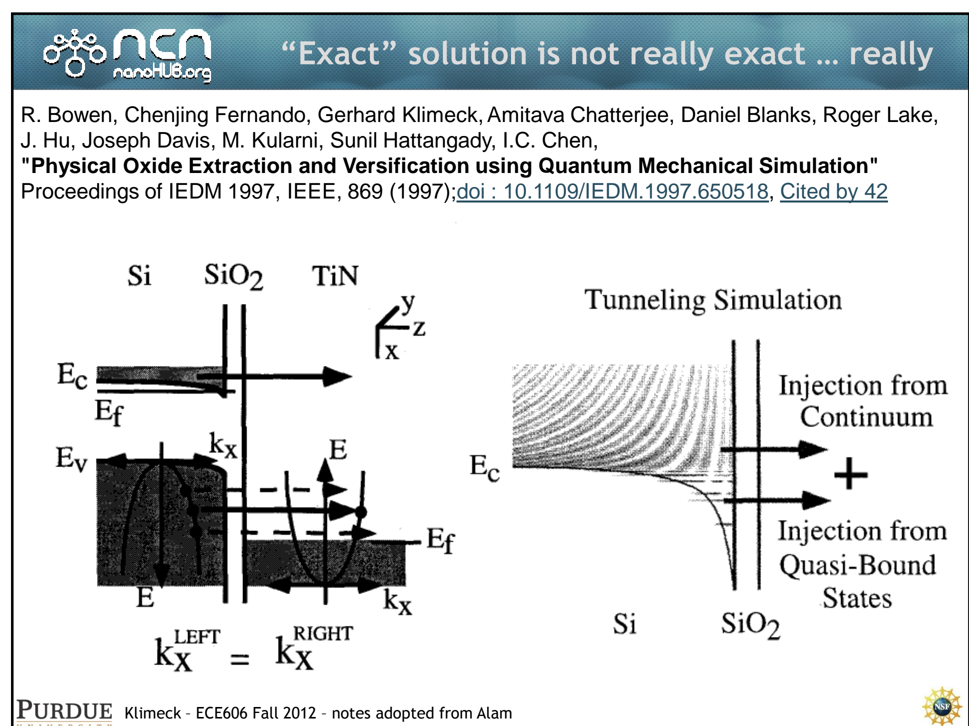

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Si
SiO2
TiN
y
z
x
Ec
Ef
Ev
kx
E
Ef
E
kx
kx LEFT = kx RIGHT
Tunneling Simulation
Injection from Continuum
+
Injection from Quasi-Bound States
Si
SiO2
PURDUE UNIVERSITY
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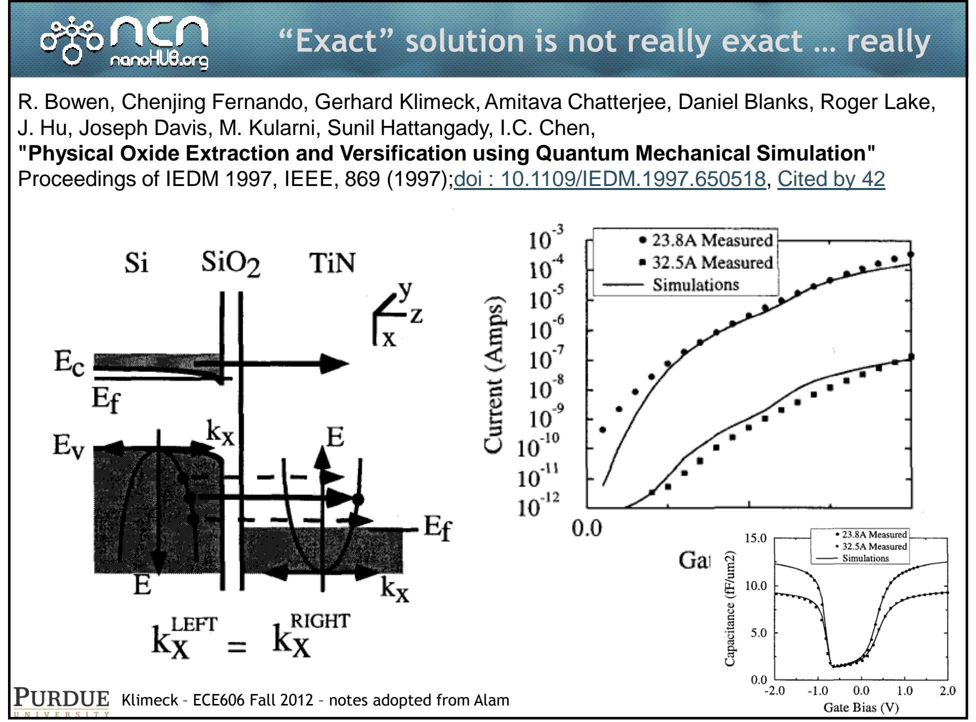
“Exact” solution is not really exact … really
R. Bowen, Chenjing Fernando, Gerhard Klimeck, Amitava Chatterjee, Daniel Blanks, Roger Lake, J. Hu, Joseph Davis, M. Kularni, Sunil Hattangady, I.C. Chen,
"Physical Oxide Extraction and Versification using Quantum Mechanical Simulation"
Proceedings of IEDM 1997, IEEE, 869 (1997);doi : 10.1109/IEDM.1997.650518, Cited by 42
Si
SiO2
TiN
Ec
Ef
Ev
kx
E
Ef
E
kx
kx LEFT = kx RIGHT
23.8A Measured
32.5A Measured
Simulations
Current (Amps)
Capacitance (fF/um2)
Gate Bias (V)
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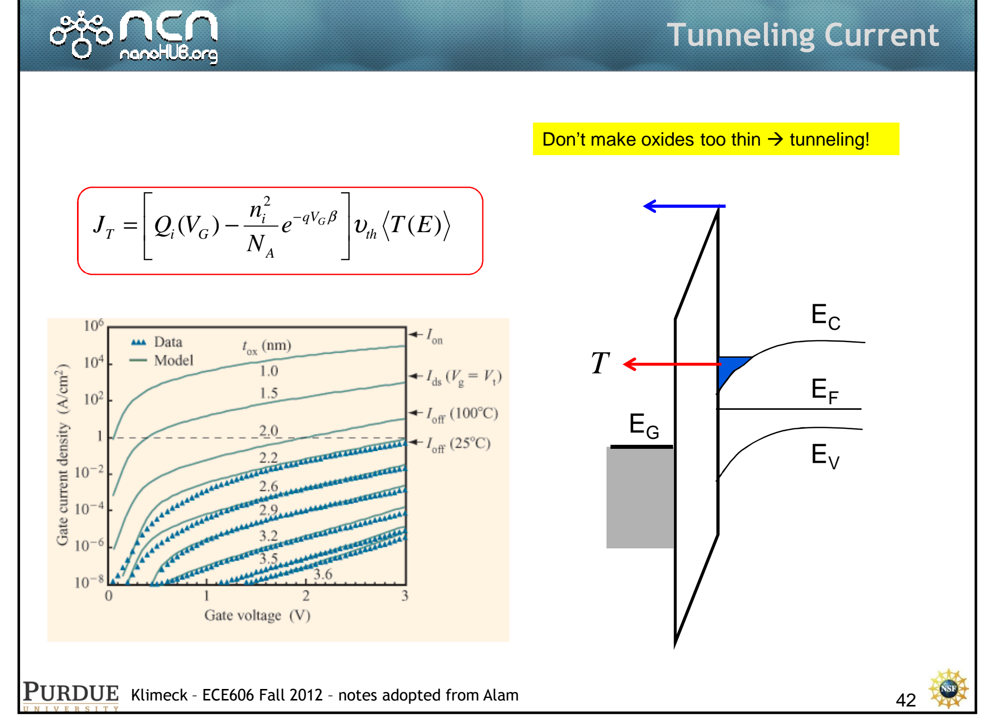
Tunneling Current
Don't make oxides too thin → tunneling!
$J_T = \left[Q_i(V_G) - \frac{n_i^2}{N_A} e^{-qV_G\beta} \right] v_{th} \langle T(E) \rangle$
Data
Model
t_{ox} (nm)
Gate current density (A/cm²)
Gate voltage (V)
I_{on}
I_{ds} ($V_g = V_t$)
I_{off} (100°C)
I_{off} (25°C)
T
EC
EF
EV
EG
PURDUE
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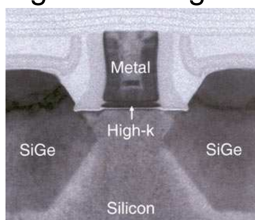
How to make Vth Roll-off small …

$$L_{\min} = \frac{qN_A W_T}{\frac{\kappa_{ox}\varepsilon_0}{x_0}} \frac{r_J}{\alpha} \left(\sqrt{1 + \frac{2W_T}{r_J}} - 1 \right)$$

High k oxides allow for smaller L_{min} but lot of defects

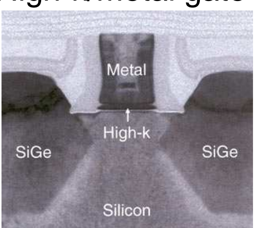
High-k/metal gate MOSFET

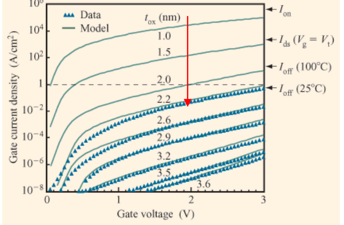


- Shallow junction and geometry of transistors
  laser annealing of junctions, FINFET
- Substrate doping NA
  consider WT and junction breakdown
- Thinner gate oxides
  consider tunneling current
- Higher gate dielectric
  consider bulk traps

Advantages of High-k Dielectric …

High-k/metal gate MOSFET





$$L_c = \frac{qN_A W_T}{\frac{\kappa_{ox}\varepsilon_0}{x_0}} \frac{r_J}{\alpha} \left(\sqrt{1 + \frac{2W_T}{r_J}} - 1 \right)$$

$$I_D = \frac{\mu C_{ox}}{L_{ch}} (V_G - V_{th}^*)^2$$

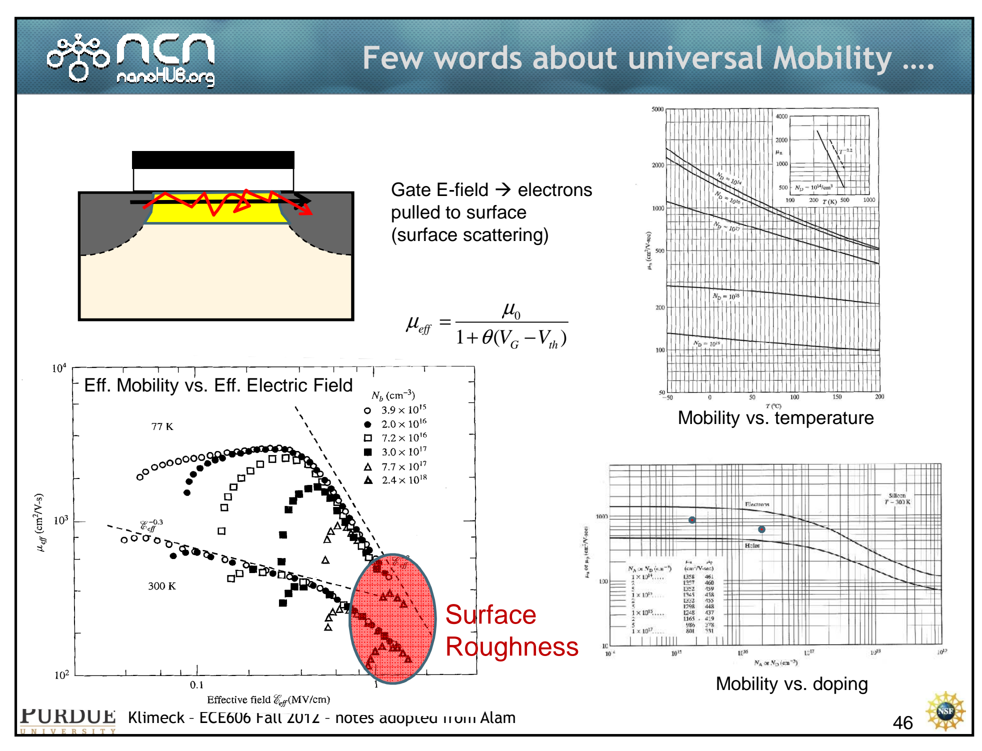
Thicker oxide (x_0) for same capacitance …

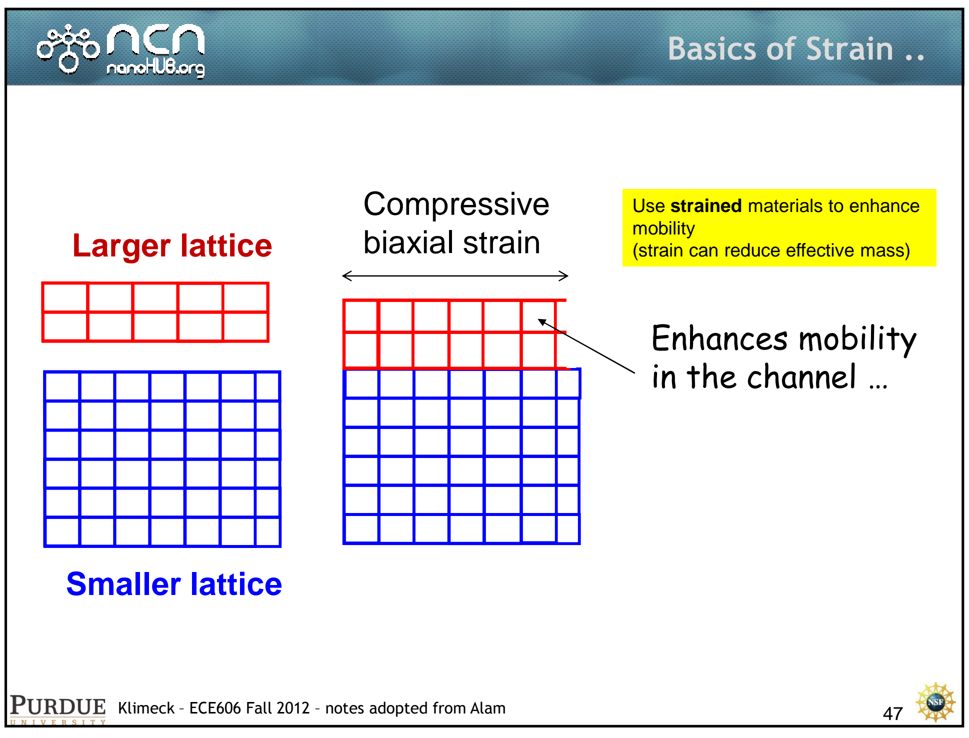
… ensures the drive-current is not reduced
, but tunneling current is suppressed.

Outline

1. Short channel effect
2. Control of threshold voltage
3. **Mobility enhancement**
4. Conclusion

$$I_D = \frac{\mu C_{ox}}{L_{ch}}(V_G - V_{th}^{*})^2$$

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Basics of Strain ..
Larger lattice
Compressive
biaxial strain
Use strained materials to enhance mobility
(strain can reduce effective mass)
Enhances mobility
in the channel …
Smaller lattice
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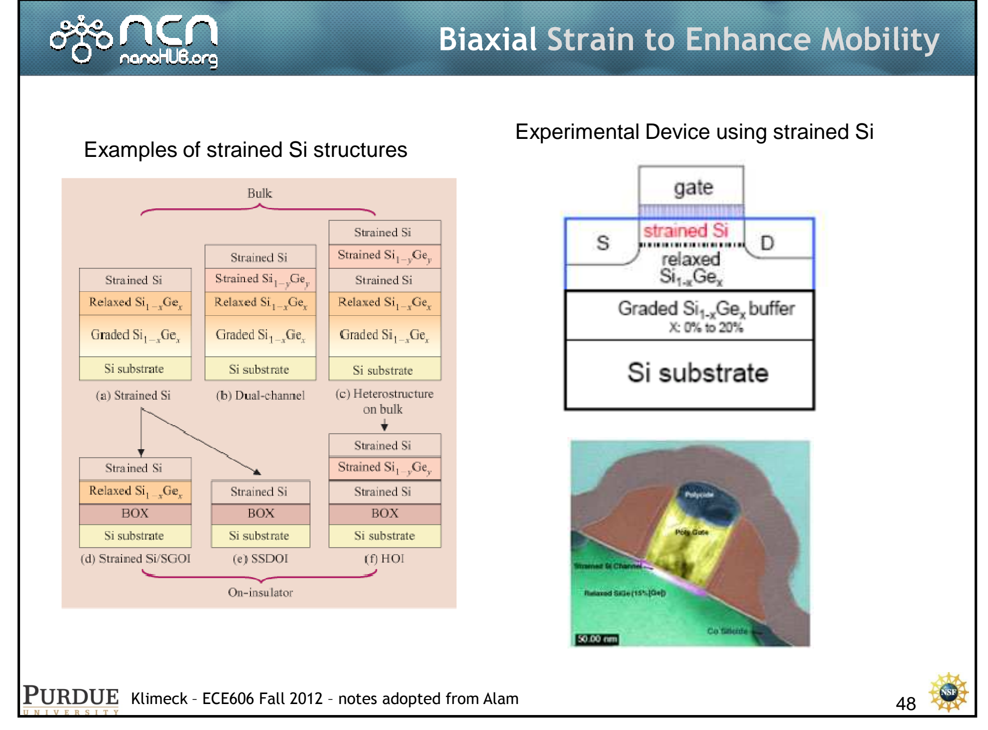
nanoHUB.org
Biaxial Strain to Enhance Mobility
Examples of strained Si structures
Bulk
Strained Si
Relaxed Si1-xGex
Graded Si1-xGex
Si substrate
(a) Strained Si
Strained Si1-yGey
(b) Dual-channel
(c) Heterostructure on bulk
BOX
(d) Strained Si/SGOI
(e) SSDOI
(f) HOI
On-insulator
Experimental Device using strained Si
gate
S
strained Si
D
relaxed
Si1-xGex
Graded Si1-xGex buffer
X: 0% to 20%
Si substrate
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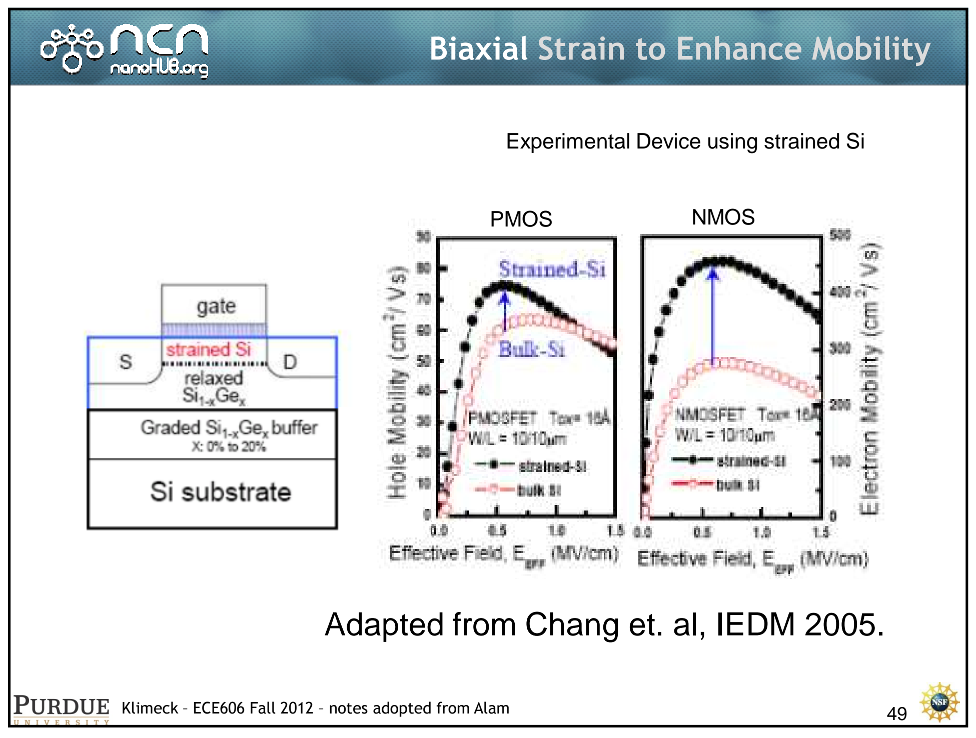
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Biaxial Strain to Enhance Mobility
Experimental Device using strained Si
gate
strained Si
S
D
relaxed
Si1-xGex
Graded Si1-xGex buffer
X: 0% to 20%
Si substrate
PMOS
NMOS
Strained-Si
Bulk-Si
Hole Mobility (cm²/ V s)
Electron Mobility (cm²/ V s)
PMOSFET Tox= 18Å
W/L = 10/10μm
NMOSFET Tox= 18Å
W/L = 10/10μm
strained-Si
bulk Si
Effective Field, EEFF (MV/cm)
Adapted from Chang et. al, IEDM 2005.
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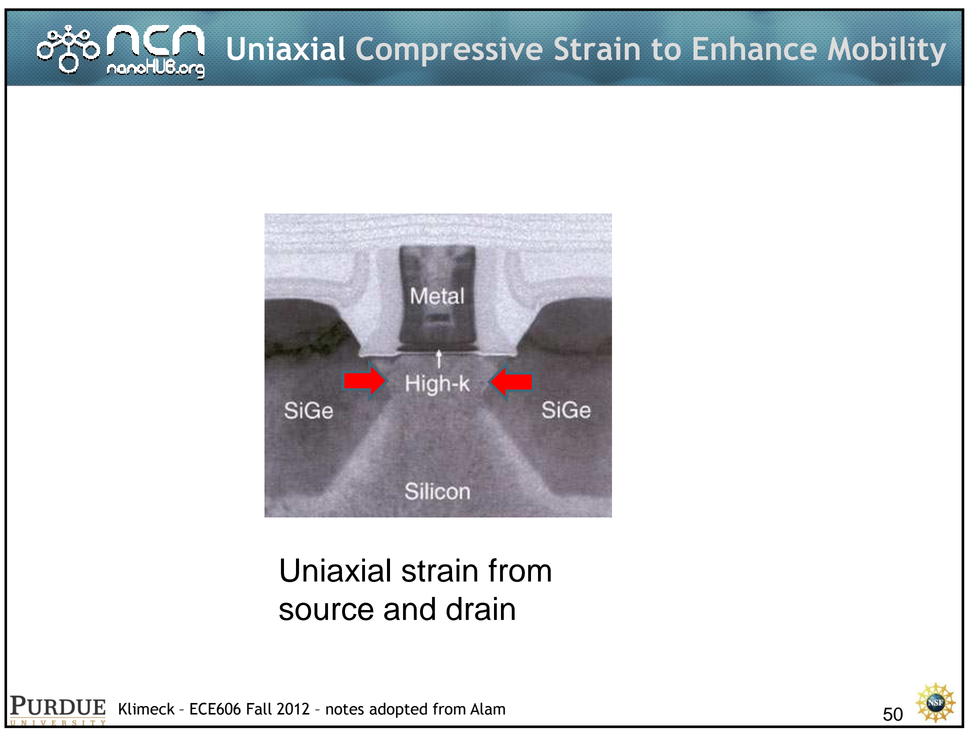
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Uniaxial Compressive Strain to Enhance Mobility
Metal
High-k
SiGe
SiGe
Silicon
Uniaxial strain from
source and drain
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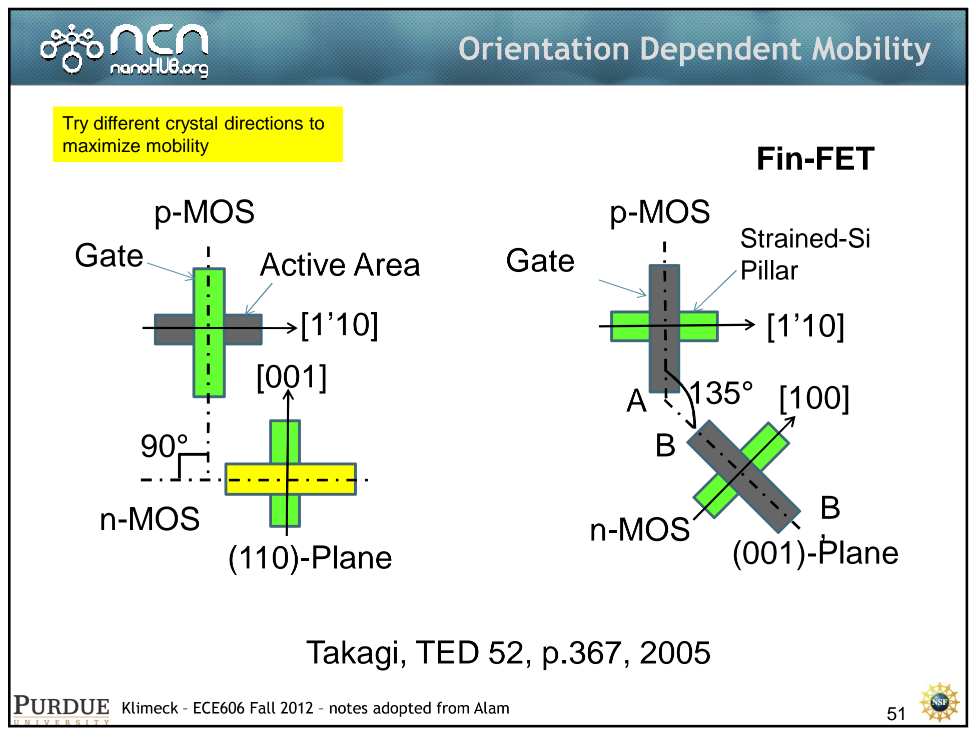
Orientation Dependent Mobility
nanoHUB.org
Try different crystal directions to maximize mobility
Fin-FET
p-MOS
Gate
Active Area
[1'10]
[001]
90°
n-MOS
(110)-Plane
p-MOS
Gate
Strained-Si Pillar
[1'10]
A
135°
[100]
B
B
n-MOS
(001)-Plane
Takagi, TED 52, p.367, 2005
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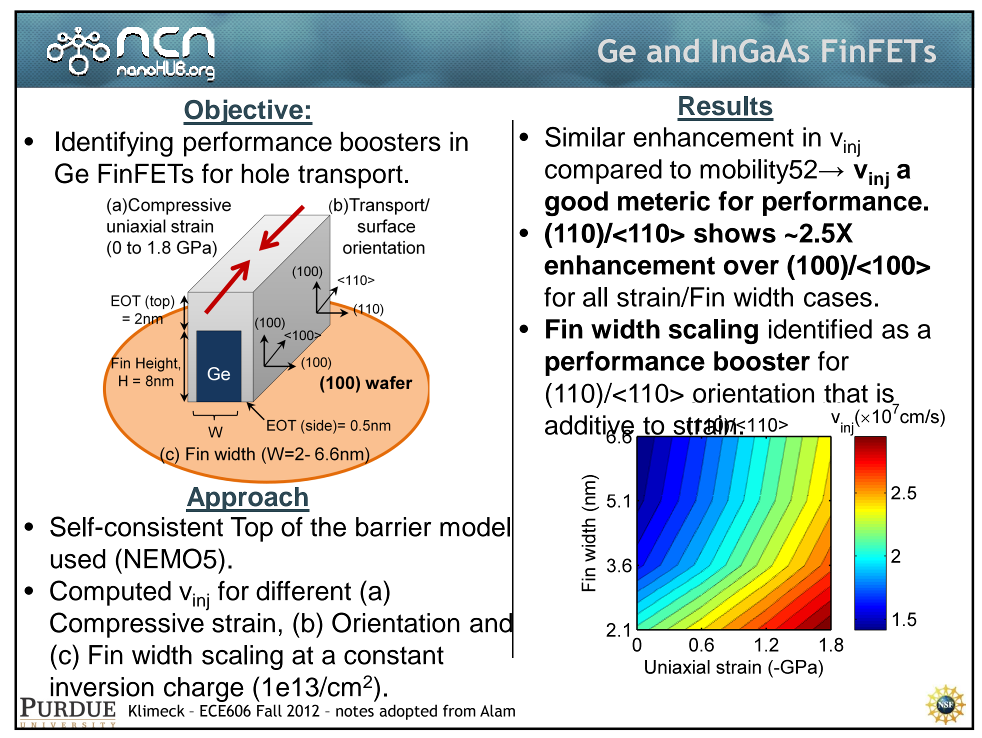
Ge and InGaAs FinFETs
nanoHUB.org
Objective:
Identifying performance boosters in Ge FinFETs for hole transport.
(a)Compressive uniaxial strain (0 to 1.8 GPa)
(b)Transport/ surface orientation
EOT (top) = 2nm
Fin Height, H = 8nm
Ge
W
EOT (side)= 0.5nm
(100) wafer
(c) Fin width (W=2- 6.6nm)
Approach
Self-consistent Top of the barrier model used (NEMO5).
Computed v_{inj} for different (a) Compressive strain, (b) Orientation and (c) Fin width scaling at a constant inversion charge (1e13/cm^2).
Results
Similar enhancement in v_{inj} compared to mobility52→ v_{inj} a good meteric for performance.
(110)/<110> shows ~2.5X enhancement over (100)/<100> for all strain/Fin width cases.
Fin width scaling identified as a performance booster for (110)/<110> orientation that is additive to strain.
(110)/<110>
v_{inj} ($\times 10^7$ cm/s)
Fin width (nm)
Uniaxial strain (-GPa)
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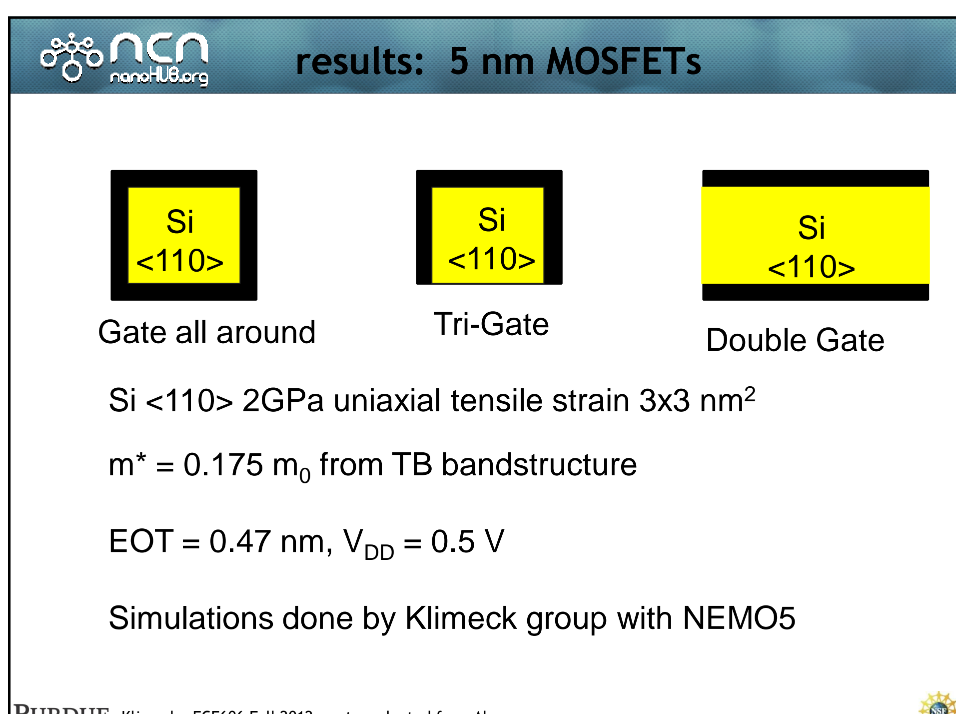
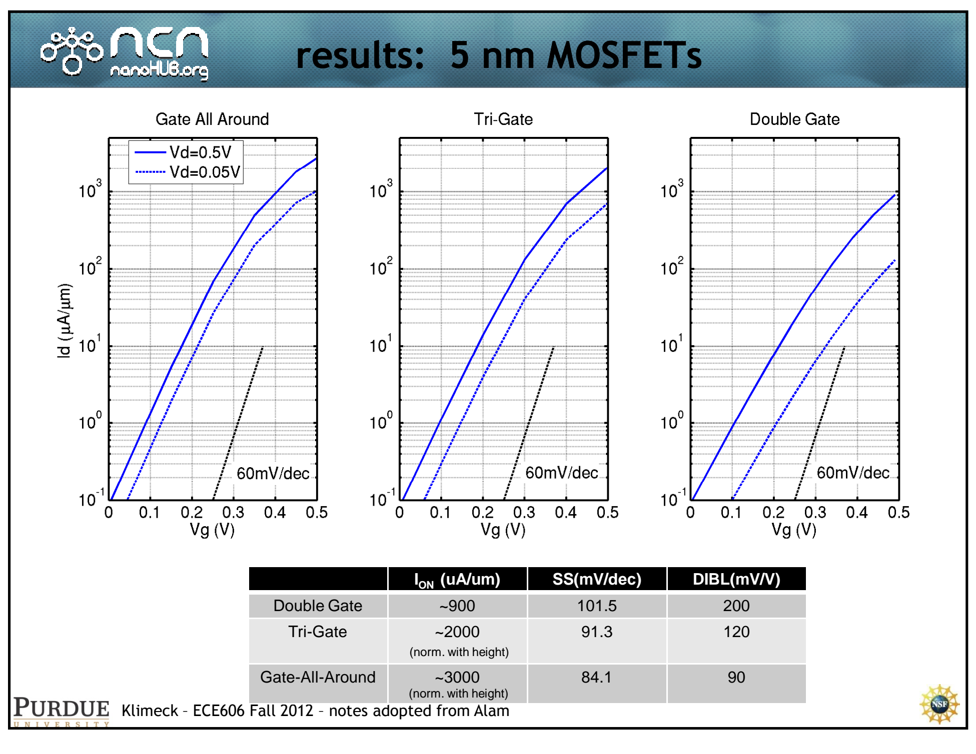
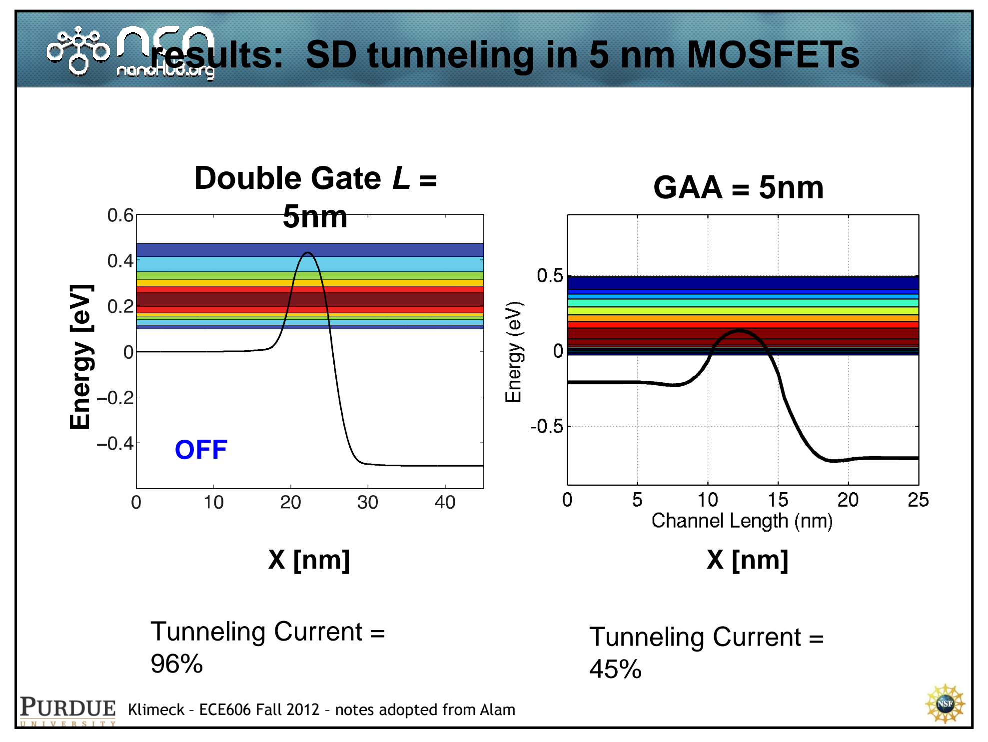




	I_{ON} (uA/um)	SS(mV/dec)	DIBL(mV/V)
Double Gate	~900	101.5	200
Tri-Gate	~2000 (norm. with height)	91.3	120
Gate-All-Around	~3000 (norm. with height)	84.1	90


results: SD tunneling in 5 nm MOSFETs
Double Gate L = 5nm
Energy [eV]
OFF
X [nm]
GAA = 5nm
Energy (eV)
Channel Length (nm)
X [nm]
Tunneling Current = 96%
Tunneling Current = 45%
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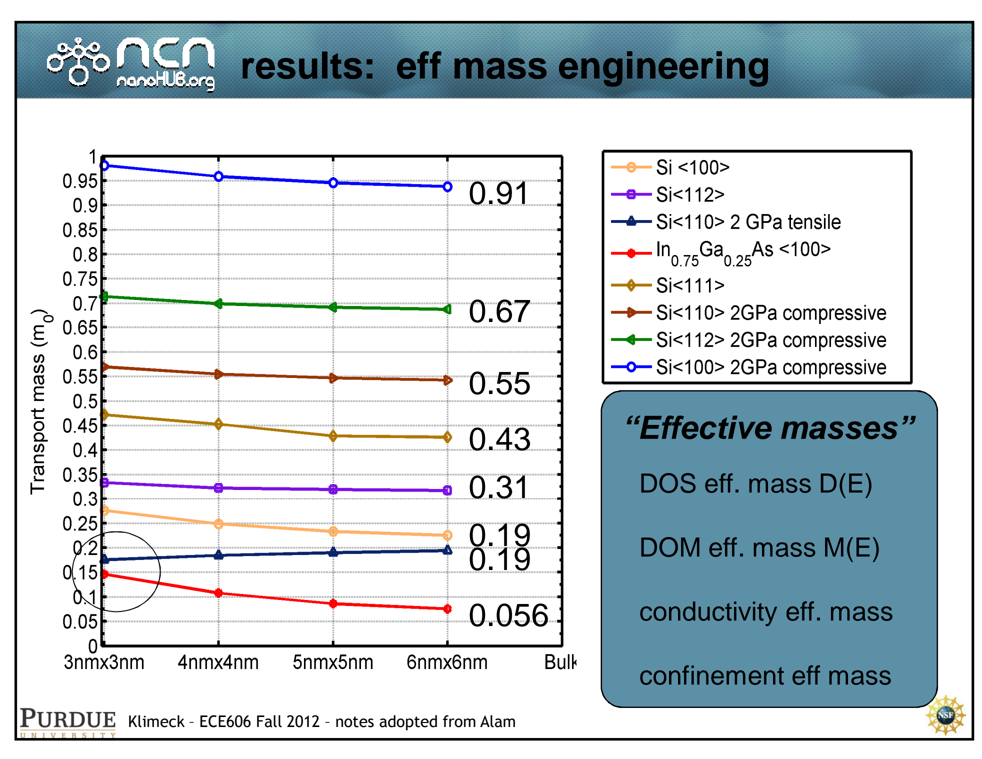
results: eff mass engineering
Transport mass (m_0)
3nmx3nm
4nmx4nm
5nmx5nm
6nmx6nm
0.91
0.67
0.55
0.43
0.31
0.19
0.19
0.056
Si <100>
Si<112>
Si<110> 2 GPa tensile
$In_{0.75}Ga_{0.25}As$ <100>
Si<111>
Si<110> 2GPa compressive
Si<112> 2GPa compressive
Si<100> 2GPa compressive
"Effective masses"
DOS eff. mass D(E)
DOM eff. mass M(E)
conductivity eff. mass
confinement eff mass
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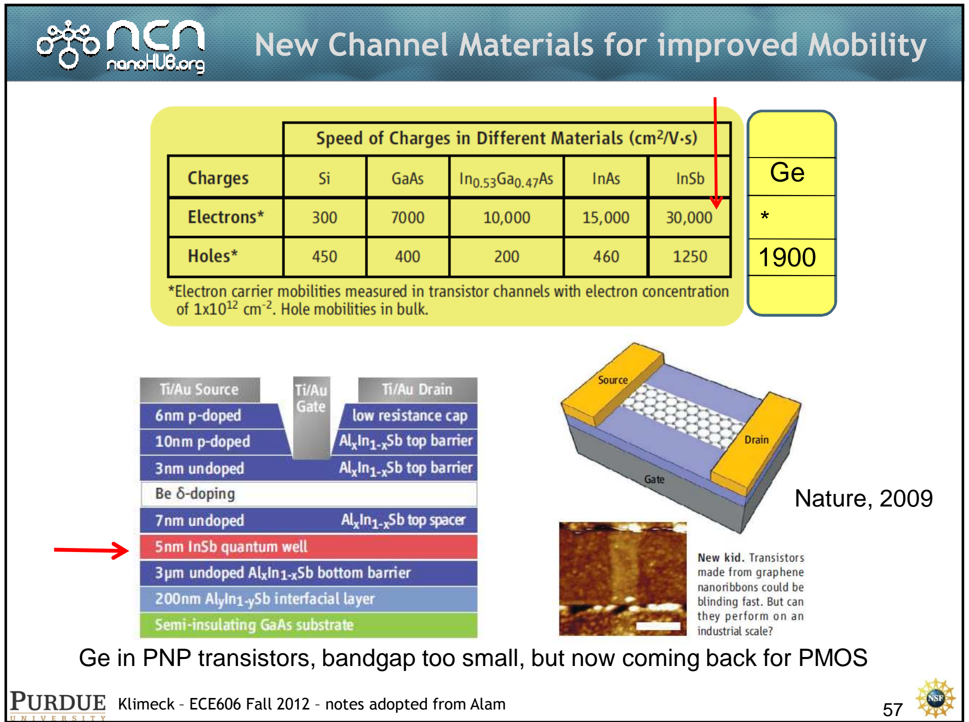

	Speed of Charges in Different Materials (cm²/V·s)					Ge
Charges	Si	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb	
Electrons*	300	7000	10,000	15,000	30,000	*
Holes*	450	400	200	460	1250	1900

*Electron carrier mobilities measured in transistor channels with electron concentration of $1x10^{12}$ cm^{-2}. Hole mobilities in bulk.

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Summary

1) Short channel effect is a serious concern for MOSFET scaling.

2) Many novel solutions at the material, device, circuit level have been proposed to reduce short channel effect.

3) The success of these efforts are now reflected in effective MOSFET channel lengths of 30 nm.