High Performance Deep-Submicron Inversion-Mode InGaAs MOSFETs with maximum G_m exceeding 1.1 mS/μm: New HBr Pretreatment and Channel Engineering

Y. Q. Wu, M. Xu, R.S. Wang, O. Koybasi and P. D. Ye

School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906, U.S.A.
Tel: 1-765-494-7611, Fax: 1-765-496-7443, Email: yep@purdue.edu

Abstract

High performance deep-submicron inversion-mode InGaAs MOSFET with ALD Al_2O_3 as gate dielectric has been demonstrated. Transistors with gate lengths down to 150 nm have been fabricated and characterized. Record high extrinsic transconductance of 1.1 mS/μm has been achieved at V_{ds} = 2.0 V with 5 nm Al_2O_3 as gate dielectric. G_m can be further improved to 1.3 mS/μm by reducing the gate oxide thickness to 2.5 nm at V_{ds} = 1.6 V. HBr pre-treatment, retro-grade structure and halo-implantation processes are introduced for the first time into III-V MOSFET to further improve high-k/InGaAs interface quality and on-state/off-state performance of the devices. The key transistor scaling metrics such as *S.S.*, *DIBL*, V_T of these treated devices are compared with the controlled devices with channel lengths from 250 nm to 150 nm.

Introduction

Using In-rich InGaAs as surface channel, high-performance inversion-mode high-k/III-V NMOSFETs have been demonstrated. [1-8] By further improving on-state performance, such as maximum drain current I_{dss} and peak transconductance G_m, the off-state performance or subthreshold characteristics need to be seriously evaluated for digital applications. In this paper, we report deep-submicron inversion-mode NMOSFETs on $In_{0.7}Ga_{0.3}As$ using 2.5 nm-5.0 nm ALD Al_2O_3 as high-k gate dielectrics with G_m exceeding 1.1-1.3 mS/μm. The record G_m is about 50-75% larger than the values reported previously and is *for the first time* beyond 1 mS/μm on any III-V MOSFETs with oxides as gate dielectrics [4,8,9]. We ascribe it to the improvement of high-k/InGaAs interface by the introduction of HBr pre-cleaning on InGaAs before ALD and the scaling of the devices. The scaling metrics, such as threshold voltage (V_T), I_{on}/I_{off} ratio, sub-threshold swing (*S.S.*), the drain induced barrier lowing (*DIBL*), as a function of the gate length from 150 nm to 250 nm are systematically studied. *Retro-grade structure* and *halo-implantation* are *first time* introduced to III-V MOSFET field to improve the off-state performance of InGaAs MOSFETs.

Experiments

Fig. 1 and Table 1 show the schematic cross section of the uniform device structure and the device fabrication flow. ALD Al_2O_3 as gate dielectric was grown *directly* on MBE InGaAs surface. A 500 nm p-doped 4×10^{17} cm^{-3} buffer layer, a 300 nm p-doped 1×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$ and a 12 nm 1×10^{17} cm^{-3} $In_{0.7}Ga_{0.3}As$ channel layer were sequentially grown by MBE on a 2-inch InP p+ substrate for all samples except for the retro-grade sample. For the retro-grade structure illustrated in Fig. 15, 50 nm heavily p-doped 1×10^{18} cm^{-3} layer was inserted 20 nm beneath the channel surface with a 12 nm 1×10^{17} cm^{-3} $In_{0.7}Ga_{0.3}As$ layer as the channel. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 10 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C as an encapsulation layer after NH_4OH treatment. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 20 keV through the 10 nm thick Al_2O_3 layer. The implantation condition was chosen carefully to achieve the desired junction depth and S/D doping concentration. Implantation activation was achieved by rapid thermal anneal (RTA) at 600 °C for 15 s in a N_2 ambient. The reduction of activation temperature from 750 °C to 600 °C results in much improved S/D junction leakage while achieving similar activation efficiency and contact resistance [9]. A 2.5 nm or 5 nm Al_2O_3 film was regrown by ALD after removing the encapsulation layer by BOE solution and various surface preparation. $(NH_4)_2S$ was used to treat the controlled samples while a HBr / $(NH_4)_2S$ combination was used as the novel pretreatment. HBr treated InGaAs surface is hydrophilic and is believed to be helpful to passivate InGaAs surface from surface recombination velocity measurements [10]. After 400-500 °C PDA process, the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA process at 320 °C for 30 s also in a N_2 ambient. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 100 nm to 250 nm. All patterns were defined by a Vistec VB-6 UHR electron-beam lithography (EBL) system. A Keithley 4200 was used for MOSFET output characteristics.

Results and discussion

A well-behaved I-V characteristic of a 160 nm-gate-length inversion-mode $In_{0.7}Ga_{0.3}As$ NMOSFET with 5 nm Al_2O_3 as gate dielectric is demonstrated in Fig. 2 with I_{dss} of 925 μA/μm and G_m of 1.1 mS/μm at maximum supply voltage of V_{DD}=2.0V. The contact resistance R_C of 350 Ω·μm is measured by TLM. After subtracting the contact resistance, the resulting intrinsic G_m is as high as 1.8 mS/μm as illustrated in Fig. 3. Fig. 4 shows I_d and I_s at V_{ds}=2.0V, 1.6V and 0.05V, respectively. It is clear that I_{sub} (the reverse-biased pn-junction leakage current) determines the leakage floor and I_d at V_{gs} < 0. There is no Fermi-level pinning at V_{gs} < 0 since the gate still controls the

channel well as shown in I_s with 7-8 orders of magnitude change with the gate bias. The analysis on I_s reflects more accurately the intrinsic properties of devices by avoiding the substrate leakage. The major contribution of the difference of drain and source current comes from the non-optimized S/D junctions, which can be improved by the refined implant condition and following thermal activation. Fig. 5 summarizes the increase of I_{dss} and G_m, the on-state performance, by reducing the channel length L_{ch} from 250 nm to 150 nm. However, off-state performance, such as *S.S.* in Fig.6 and *DIBL* in Fig.7, starts to degrade and show the short-channel effect due to 25 nm-range deeply implanted S/D.[9] Fig.8 shows the threshold voltage V_T determined by linear extrapolation at V_{ds}=0.05V or I_{ds}=1μA/μm metrics.

Reduction of Al_2O_3 down to 2.5 nm (EOT≈1nm) can improve the electrostatic control of the channel significantly. Fig.9 and Fig.10 compare I_{dss} and G_m of 2.5 nm and 5 nm Al_2O_3 devices without HBr treatment at V_{DD}=1.6V. Record high extrinsic transconductance G_m of 1.3 mS/μm is reached at L_{ch}=150 nm. Improved off-state characteristics are summarized in Fig.11-Fig.14. *S.S.* improves through the better gate control by reducing the effect from the interface trap capacitance. This comparison shows the potential of both on-state and off-state performance of the deep-submicron InGaAs MOSFETs for logic applications. The availability of even higher dielectric constant material, i.e., ALD $LaLuO_3$ (k=24-26), provides a pathway to further scale down the InGaAs MOSFETs.

Channel engineering–retro-grade structure illustrated in Fig.15 and halo-implantation as shown in Fig.16–has been studied to further improve off-state performance. The underlying heavily doped InGaAs layer beneath the channel of the retro-grade structure would improve the *S/D* punch-through. The halo-implantation was performed by implanting Zn with ±30 degree angles to the normal. Fig. 17 and Fig. 18 summarize I_{dss} and G_m of 4 different types of devices with 5 nm Al_2O_3 at all L_{ch} measured. Uniform channel as shown in Fig.1 without HBr pretreatment is used as a control sample. HBr treated sample (without channel engineering) has the best on-performance among the four and is attributed to the improved interface. Both retro-grade sample and halo-implanted sample are degraded on-current and peak G_m, which are expected from inducing scattering and reducing channel mobility. This is a trade-off for the improved off-state performance such as *S.S.* and *DIBL* as demonstrated in Fig.19 and Fig.20. The control sample has the largest *S.S.* and *DIBL* among the four. The *S.S.* of HBr-treated sample has about 25% improvement over the control sample, indicating clearly the significant reduction of interface trap density. The retro-grade and halo-implanted sample also have better *S.S.* over control sample because of the improved gate electro-static control and reduced short channel effect. It should be pointed out that *S.S.* of devices in deep-submicron region is not only affected by interface trap density, but also by short-channel effect, and can be dominated by the latter when entering the sub-100 nm region. Halo-implanted sample has the best *DIBL* among the four shown in Fig. 20, which indicates that it has the best-improved short-channel effect. The combination of HBr and channel-engineering could result in even better scaling metrics and is currently being investigated. Fig. 21 shows V_T vs L_{ch} using I_{ds}=1μA/μm metrics at V_{ds}=1.6V. The typical roll-off of V_T at shorter gate lengths is also observed here. All treated samples have better V_T roll-off than control sample. Fig. 22 summarizes I_{on}/I_{off} vs L_{ch} of 4 different types of devices from I_d. I_{on}/I_{off} is chosen as I_{on} (V_{ds}=1.6V, V_{gs}=2/3V_{ds}+V_T)/I_{off} (V_{ds}=1.6V, V_{gs}=-1/3V_{ds}+V_T), where V_T is determined by 1μA/μm metric. The similar definition is also used in Fig. 14 for I_s. Junction leakage is the dominant factor currently for I_d at V_{gs}<0 or I_{off}. For retro-grade sample, I_{sub} or I_{off} is higher due to heavily p-doped $2x10^{18}/cm^3$ layer in source/drain as shown in Fig. 15. This junction leakage mainly comes from the non-optimized *S/D* junctions after implantation and activation which can be greatly improved by better control of the process. If eliminating the junction leakage or I_{on}/I_{off} taken from I_s, I_{on}/I_{off} is improved to 10^4-10^6 at 150-200 nm gate lengths as shown in Fig. 14. Without considering the contribution from short-channel effect, with the lowest *S.S.* of 126 mV/dec. for HBr treated samples at V_{ds}=0.05V, the upper limit for interface trap density D_{it} is $2.8x10^{12}/cm^2$-eV. More detailed interface characterizations by CV and GV methods are on-going.

Conclusion

We have demonstrated high-performance deep-submicron inversion-mode InGaAs MOSFETs with record G_m exceeding 1.1 mS/μm. HBr pre-cleaning, retro-grade structure and halo-implantation processes are first time introduced into III-V MOSFETs to steadily improve high-k/InGaAs interface quality and on-state/off-state performance of the devices. Much more work on high-k/InGaAs interface and InGaAs ultra-shallow junction are needed to make III-V an alternative technology at CMOS 15 nm technology node.

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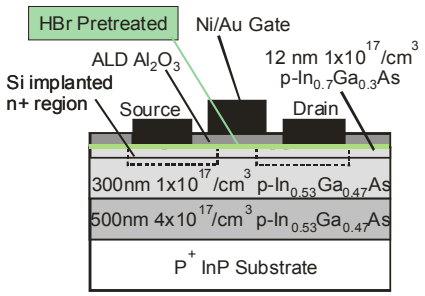

Fig. 1 Schematic view of an inversion-mode n-channel $In_{0.7}Ga_{0.3}As$ ($1\times10^{17}/cm^3$) MOSFET with 5nm ALD Al_2O_3 as gate dielectric. The device is not self-aligned. HBr pretreatment before ALD is an important step to improve interface quality.

1)	NH_4OH surface treatment and ALD Al_2O_3 10nm deposition
2)	S/D patterning and Si implantation (20KeV / $1\times10^{14}/cm^2$)
3)	Si implanted S/D activation using RTA (600°C 15s in N_2)
4)	Diluted HBr and $(NH_4)_2S$ treatment (controlled sample with only $(NH_4)_2S$ treatment) and 2.5 - 5nm ALD re-growth
5)	PDA: 400-500 °C 30s in N_2
6)	S/D contact patterning and Au/Ge/Ni ohmic metal and 320°C anneal
7)	Gate patterning, Ni/Au evaporation and lift-off

Table 1 Fabrication process flow for inversion-mode high-k/InGaAs MOSFETs. 10 nm Al_2O_3 acts as an encapsulation layer to protect the surface during implantation and the following activation. All patterns were defined by a Vistec VB-6 UHR electron beam lithography system.

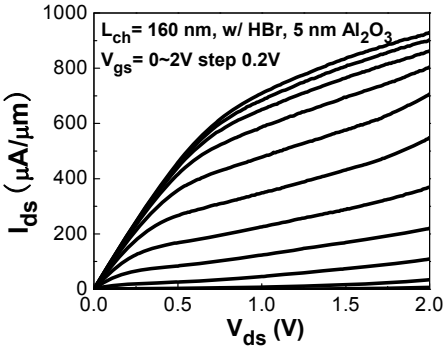

Fig. 2 I_{ds} vs V_{ds} as a function of V_{gs} for a 5nm Al_2O_3 InGaAs MOSFET with HBr pretreatment.

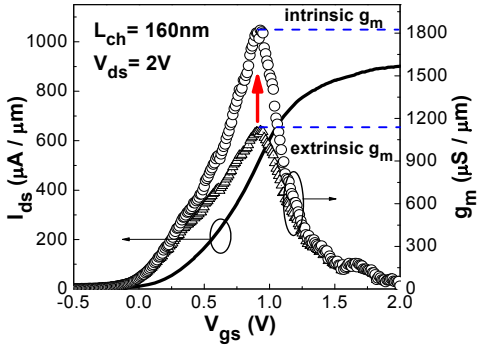

Fig.3 Extrinsic I_{ds} and g_m vs V_{gs}. The maximum extrinsic G_m reaches 1.1 mS/μm.

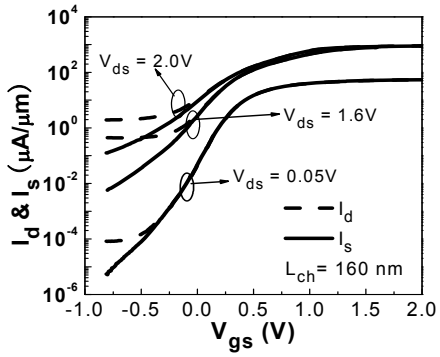

Fig.4 I_d and I_s at three V_{ds} of the same $In_{0.7}Ga_{0.3}As$ MOSFET with L_{ch}=160 nm.

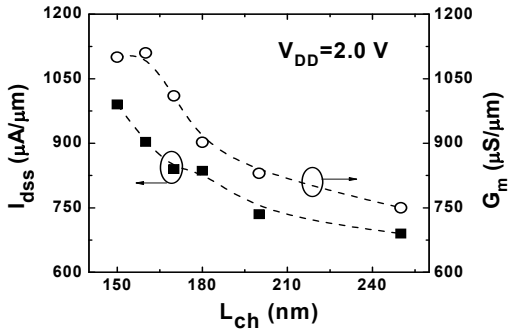

Fig. 5 Scaling characteristics of maximum drain current and peak transconductance vs L_{ch}.

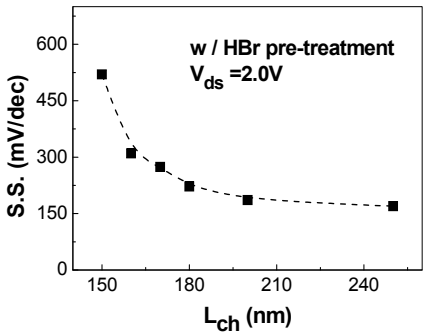

Fig.6 Subthresold slope (*S.S.*) vs L_{ch}.

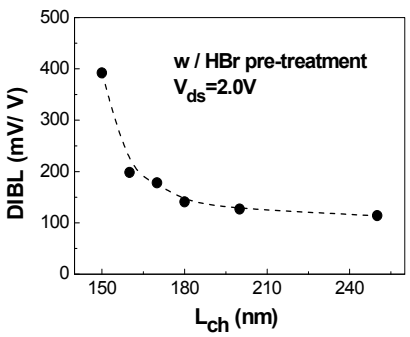

Fig.7 *DIBL* vs L_{ch} of the same devices.

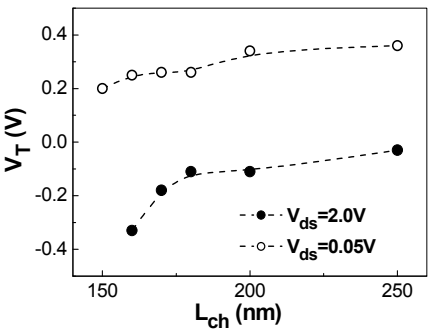

Fig.8 V_T vs L_{ch} determined by linear extrapolation (V_{ds}=0.05V) and I_{ds}=1μA/μm metrics at saturation region (V_{ds}=2.0V).

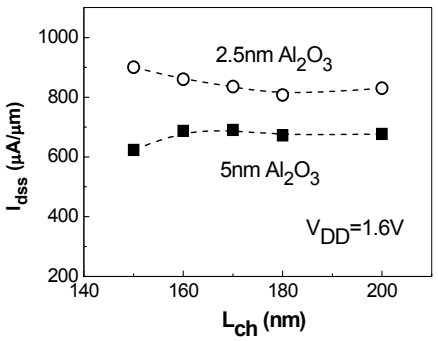

Fig. 9 Comparison of I_{dss} vs L_{ch} for the devices with 2.5nm and 5nm thick gate dielectrics w/o HBr pretreatment and at V_{ds}=1.6V.

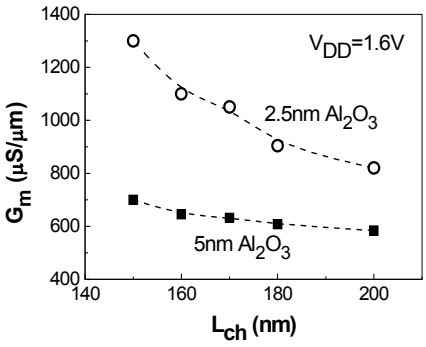

Fig. 10 Comparison of peak G_m vs L_{ch} for the devices with 2.5nm and 5nm Al_2O_3 w/o HBr pretreatment and at V_{ds}=1.6V.

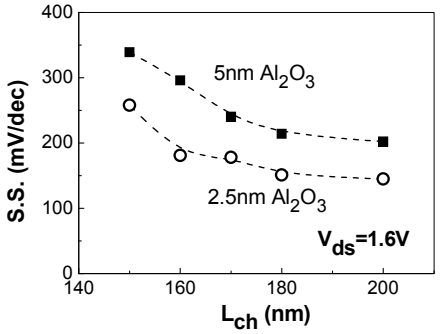

Fig. 11 Comparison of *S.S.* vs L_{ch} for the devices with 2.5 nm and 5 nm Al_2O_3.

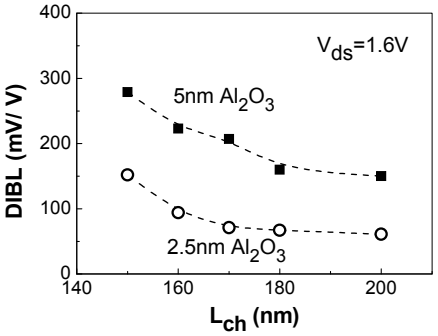

Fig. 12 Comparison of *DIBL* vs L_{ch} for the devices with 2.5 nm and 5 nm Al_2O_3.

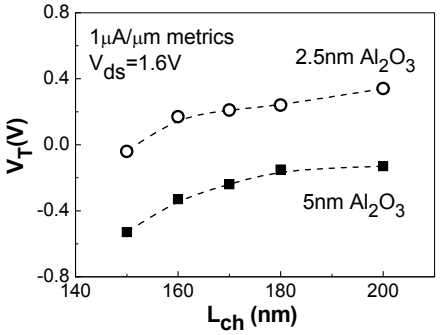

Fig. 13 Comparison of V_T vs L_{ch} for for the devices with 2.5 nm and 5 nm Al_2O_3.

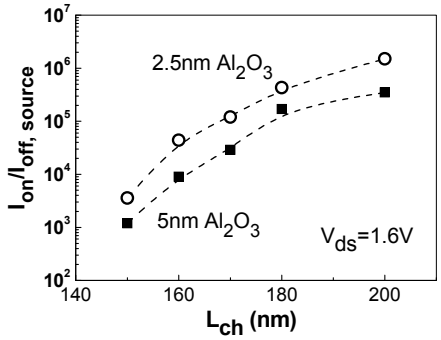

Fig. 14 Comparison of I_{on}/I_{off} obtained from I_s vs L_{ch} for the devices with 2.5 nm and 5 nm Al_2O_3.

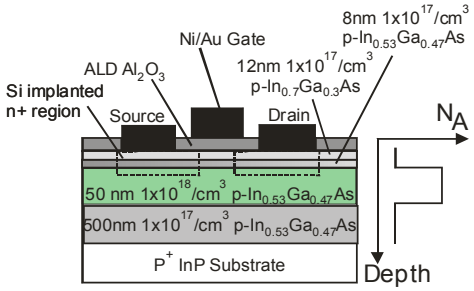

Fig. 15 Schematic view of a device with a retro-grade (RG) structure used for reducing the short-channel effect.

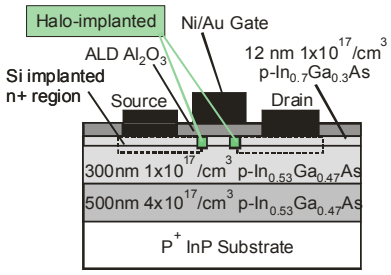

Fig. 16 Schematic view of a device with halo-implantation (Halo). Halo condition is Zn, 50KeV, 6×10^{12}/cm^2 with ±30 degrees.

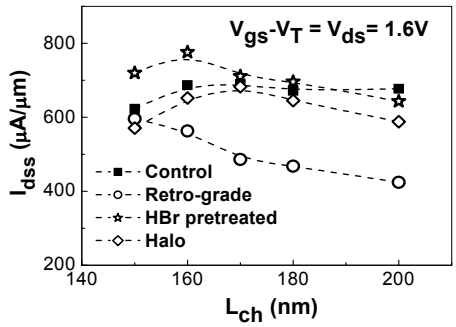

Fig. 17 Comparison of I_{dss} vs L_{ch} for 4 different types of devices. Note V_{gs}=1.6V+V_T is applied for fair comparison.

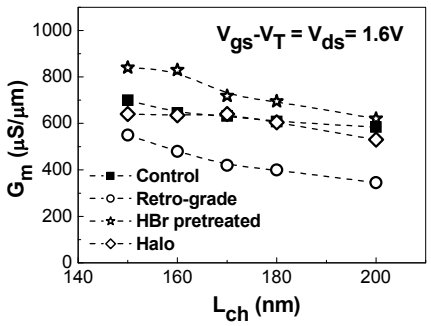

Fig. 18 Comparison of G_m vs L_{ch} for 4 different types of devices. Note G_m<1mS/μm is because V_{ds}=1.6V instead of V_{ds}=2V in Fig.3.

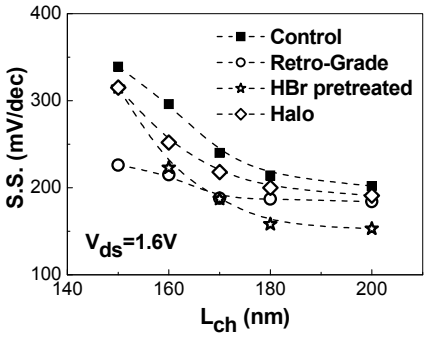

Fig. 19 Comparison of *S.S.* vs L_{ch} for 4 different types of devices. The best value at V_{ds}=1.6V is 150 mV/decade.

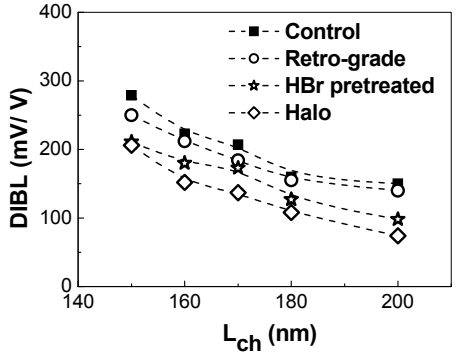

Fig. 20 Comparison of *DIBL* vs L_{ch} for 4 different types of devices.

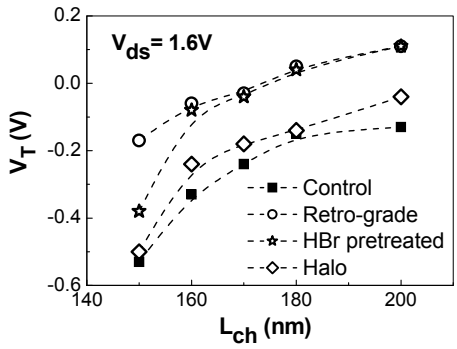

Fig. 21 Comparison of V_T vs L_{ch} for 4 different types of devices using 1μA/μm metrics.

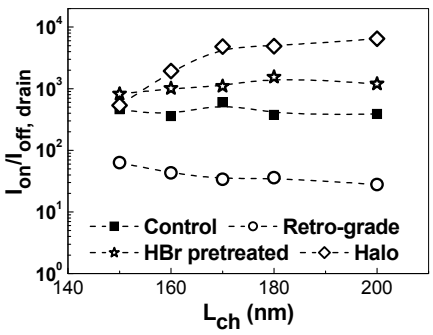

Fig. 22 Comparison of I_{on}/I_{off} obtained from I_D vs L_{ch} for the 4 types of devices. Halo-implanted devices show promising in terms of I_{on}/I_{off} ratio. I_{off} is limited by reversely biased implanted pn junctions at current process.