New Insight into Fermi-Level Unpinning on GaAs: Impact of Different Surface Orientations

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Abstract

We have systematically studied NMOSFETs, MOSCAPs, and the interfacial chemistry on GaAs (100), (110), (111)A and (111)B-four different crystalline surfaces with *direct* ALD Al_2O_3. We found that a much higher drain current on GaAs(111)A NMOSFET can be achieved compared to that obtained on the other 3 surfaces. Also, the results of MOS-CAPs and the interfacial chemistry obtained on the (111)A surface are very different from those others. These experimental results conclusively demonstrate that Fermi-level on the GaAs (111)A surface is indeed unpinned and Fermi-level pinning is not an intrinsic property of GaAs, but is orientation dependent thus related to surface chemistry.

Introduction

GaAs is of great importance for the understanding of III-V interfaces and also has practical applications due to its high electron mobility, high saturation velocity, and wide bandgap. Although encouraging results are obtained on SiH_4-passivated GaAs inversion NMOSFETs [1,2], high-performance GaAs MOSFETs with directly deposited high-k dielectrics remain a big challenge, most showing minuscule drain currents. [3-6] Some researchers suspect that the Fermi-level energy (E_F) of GaAs is intrinsically pinned at the mid-gap with directly deposited ALD Al_2O_3 as proposed by the unified defect model [7]. In this paper, we systematically study NMOSFETs, MOS-CAPs, and the interfacial chemistry on GaAs (100), (110), (111)A and (111)B -four different crystalline surfaces with ALD Al_2O_3 in *direct* contact with the GaAs substrates. We conclude E_F on the GaAs (111)A surface is indeed unpinned with the results of GaAs PMOSFETs on (111)A. [8]

Experiments

Fig. 1 and Table 1 show the schematic cross section of a GaAs inversion-mode MOSFET and the device fabrication flow. The ALD Al_2O_3 gate dielectric was grown *directly* on semi-insulating GaAs substrates with the four different surface orientations. For GaAs MOSCAPs, an 8nm ALD Al_2O_3 gate dielectric was deposited at 300°C after HCl and $(NH_4)_2S$ based surface pretreatment and with post-deposition annealing. [9]

Results and Discussions

In order to describe E_F pinning issues on GaAs more accurately, we use the following terminology. "Fermi-level pinning" refers to when the E_F at the oxide/GaAs interface is absolutely pinned. That is, the E_F is invariant with respect to gate bias and the associated CV curve is flat. This behavior was commonly observed in many early GaAs MOSCAP reports. "Fermi-level unpinning" refers to when E_F at the oxide/GaAs interface can move $2\Psi_B$ resulting in strong inversion caused by the gate bias, where Ψ_B is E_F from the intrinsic Fermi-level. Due to the low density of states in GaAs, E_F for 10^{17}-10^{18}/cm^3 doping concentrations locates at band edges and $2\Psi_B$ requires E_F movement almost across the whole bandgap of GaAs. Perhaps the most controversial effect is when E_F can be modulated by the gate bias, but it cannot reach strong inversion at the band edges, due to a large amount of interface traps with levels in the bandgap. This situation is referred to as a condition where the "Fermi-level is partially (or weakly) pinned". For ALD high-k on GaAs, it is also useful to divide the GaAs bandgap to upper half and lower half, because electrical properties of upper half interface are more controlled by the Ga-oxide and lower half by the As-oxide.

A well-behaved I-V characteristic of a 4μm-gate-length inversion GaAs NMOSFET on (111)A surface is demonstrated in Fig. 4 with maximum drain current of 30 μA/μm, which is *a factor of 85,000 or 25,000 larger* than that obtained on (100) or (110) as shown in Fig. 2 and Fig. 3. The similar low inversion currents on GaAs (100) or (110) and even zero-current on GaAs (111)B lead to the conclusion of E_F pinning in past studies. The GaAs (111)A surface is astonishingly different and E_F is unpinned, resulting in a large drain current. Together with the demonstrated reasonable drain current on GaAs PMOSFETs on (111)A surface[8], we conclude that the E_F is unpinned on GaAs (111)A surface with direct ALD Al_2O_3.

Fig. 5 shows the I_{DS} versus V_{GS} at V_{DS}=2V and V_{DS}=0.05V of the same device in Fig. 4. There is no E_F pinning detected since the gate controls the channel well with 7-8 orders of magnitude change in I_{DS} with the gate bias. The threshold voltage is determined to be 0.45V by the linear extrapolation method as an enhancement-mode MOSFET. The ratio I_{on} (I_{DS} at V_{GS}=4V, V_{DS}=2V)/I_{off} (I_{DS} at V_{GS}=0, V_{DS}=2V) is 1.28×10^4, which is one order of magnitude better than that of inversion-mode InGaAs MOSFETs [10], due to the wide band-gap of GaAs. Fig. 6 shows the trans-conductance G_m versus V_{GS} at V_{DS}=2V and V_{DS}=0.05V with the peak G_m of 14 μS/μm at V_{DS}=2V. Fig. 7 depicts the peak effective mobility of 1402 cm^2/Vs obtained from the G_m at V_{DS}=0.05V in Fig. 6 and 100 kHz C-V in the inset for the inversion charge. Although the low-field mobility is higher than that for the universal Si mobility, the high-field mobility is still quite low due to the interface traps. This limits the inversion charge and drain current.

Although an inversion-mode MOSFET with a large drain current is the most straightforward and conclusive evidence for E_F unpinning, CV measurements are very useful to quantitatively characterize the interface properties. CV data from MOSCAPs should be consistent with I-V characteristics of MOSFETs if CV data are interpreted *correctly*. Fig. 8 illustrates the temperature dependence of the accumulation capacitance of majority carriers on a n-type MOSCAP on (111)A. The frequencies range from 1kHz to 373 kHz. The frequency dispersion on n-type GaAs(111)A is quite small, compared to most reported data in literature without a Si interface passiva-

tion layer. This frequency dispersion at accumulation is temperature *insensitive*. Parasitic effects could contribute to the frequency dispersion instead of interface traps. The small reduction of maximum capacitance is because of the *decrease* of accumulation charges at the very low temperature (10K) from the low density of states for GaAs. The results on (111)B, (110) and (100) are very different, as shown in Fig. 9 for the (100) surface as a representative case. The maximum capacitance reduces by 70% and the frequency dispersion disappears at 10 K. This leads us to conclude that room temperature capacitance at positive gate biases is not a real accumulation capacitance of electrons. It is interface trap related so that it has a large frequency dispersion. The E_F is partially pinned at upper half bandgap of GaAs on (100), (110) and (111)B surfaces. It cannot be moved beyond the flat-band condition or even into the conduction band. With this kind of pinned depletion layer, majority carriers (electrons) are trapped and de-trapped from the interface with a strong frequency or temperature dependence, as expected. Majority carrier temperature-dependent multi-frequency CV measurement in the accumulation region is another test vehicle for E_F pinning.

Table 2 summarizes the substantial surface orientation impact on inversion current, low temperature capacitance reduction, and the calculated position of E_F relative to the conduction band edge (E_c), (E_F-E_c). This difference is estimated from the capacitance at 10K due to the near-complete freeze-out of interface traps. It agrees quite well with Medici simulations of drain current versus E_F position for L_g=4 μm NMOSFETs in Fig.10. The conclusion is that E_F is already in the conduction band resulting in a 30 μA/μm inversion drain current and is therefore unpinned on GaAs(111)A. E_F could be partially pinned at 0.2-0.4 eV below the conduction band minima for (110), (100), and (111)B, which is consistent with the CV measurement results in Fig. 8 and Fig. 9.

Figs. 11 and 12 show the temperature dependence of CV curves for p-type MOSCAPs on (111)A and (100). The accumulation capacitance and frequency dispersion is weakly dependent on temperature. This is because the lower half of the bandgap of GaAs is unpinned on both (111)A and (100). The result is also consistent with reasonable drain currents on GaAs PMOSFETs on both surfaces, as reported in Ref.[8]. The interface properties of GaAs lower half bandgap is mainly controlled by As-oxides. The ALD "self-cleaning" effect removes most of As-oxides on GaAs [11-14] and unpins the lower half bandgap of GaAs on (100), (110) and (111)A. The weak temperature dependence in p-type MOSCAPs, compared to n-type MOSCAPs in Fig.8, is due to the larger effective mass of holes, and thus larger density of states than electrons. Calculated ideal CV curves fit well on the (111)A at both accumulation and inversion sides but not on the (100) at the inversion side as shown in Fig.13. Only if the E_F is unpinned and moves $2\Psi_B$ across the whole bandgap, can the maximum depletion depth be reached and the C_{min} of high-frequency CV fits the theoretical curve. Figs.14 and 15 show the real inversion CVs at 150°C on (111)A and the measured interface trap density (D_{it}) distribution in the band-gap from conductance method. No D_{it} peaks are detected at midgap [7] on GaAs (111)A.

Angle-resolved high-resolution monochromatic XPS studies were obtained on companion samples and shown in Figs.16-18. Data at three takeoff angles relative to the sample surface were acquired ranging from 75° (bulk/interface sensitive) to 45° (surface sensitive). The Ga 2*p* spectra (Fig. 16) reveals that significantly less Ga_2O_3 (Ga 3+ oxidation state) occurs at the Al_2O_3/GaAs (111)A interface, which leads to unpinning the upper half of the bandgap, while the Ga 1+ state (likely Ga_2O) remains.[15] Prior work has indicated that excessive amounts of the Ga 3+ oxide can degrade capacitor [16] and transistor performance. [17]

Figure 17 presents the As 2*p* spectra showing the reduction ("self-cleaning") of surface As-oxides by the ALD process to levels near the detection limit [11-14]. This self-cleaning unpins the lower half of the band-gap of GaAs on (100), (110) and also (111)A surfaces, as seen in the electrical characterization. However, substantial As-oxide formation is observed on the As-terminated GaAs(111)B surface (not shown), as may be expected due to kinetic limitations of the cleaning reaction.

Figure 18 shows the Ga 2*p* peak areas obtained from XPS analysis for all orientations studied. It is seen that the formation of Ga 3+ and Ga 1+ oxides is at or below the detection limit for the GaAs(111)A surface, which provided superior device characteristics. We also note that in all orientations investigated, trace amounts of F (and C) were observed at the interface (surface). The origin of the C is largely attributed to atmospheric exposure prior to XPS analysis, while the origin of the F is attributed to device processing. The relative amount of F appears to vary by ~20% among the orientations, with the GaAs(111)A surface the smallest. Further work in examining the origin and role of F is underway.

Conclusion

We have demonstrated a real inversion-mode NMOSFET on GaAs(111)A with good drain current. Through systematic studies on GaAs(111)A, (111)B, (110), (100), we discovered that the Fermi-level on GaAs (111)A is fully unpinned through supporting data from MOSFETs, MOSCAPs and XPS. The lower half of the bandgap of GaAs (100) and (110) is also unpinned due to the "self-cleaning" of As-oxide by ALD.

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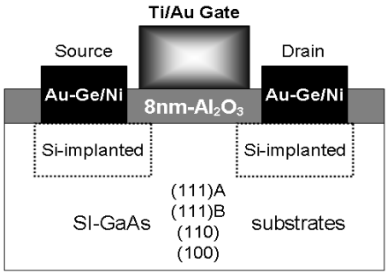

Fig. 1 Schematic view of an inversion GaAs NMOSFET with an ALD Al_2O_3 gate dielectric.

1)	Native oxide removal by HCl solution
2)	$(NH_4)_2S$ surface treatment and 30nm ALD Al_2O_3 as encapsulation layer
3)	S/D patterning and Si implantation (30KeV/1x10^{14} cm^{-2} & 80KeV/1x10^{14} cm^{-2})
4)	S/D activation using RTA (820^{o}C, 15s in N_2)
5)	Al_2O_3 encapsulation layer removal by BOE solution
6)	$(NH_4)_2S$ surface treatment and 8nm ALD Al_2O_3 re-growth
7)	600^{o}C, 30s PDA in N_2
8)	S/D contact patterning and Au/Ge/Ni ohmic metal evaporation and 400^{o}C RTA
9)	Gate patterning and Ti/Au evaporation

Table 1 Process flow for inversion-mode GaAs NMOSFETs. 30nm Al_2O_3 encapsulation layer was used to protect the surface during implantation and the following activation.

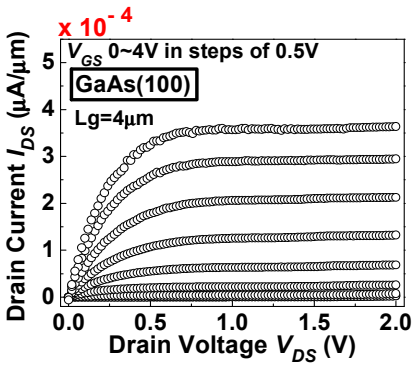

Fig. 2 Output characteristic (I_{DS}~V_{DS}) for Al_2O_3/GaAs(100) NMOSFET with 4μm gate length. The maximum drain current is 3.5x10^{-4} μA/μm.

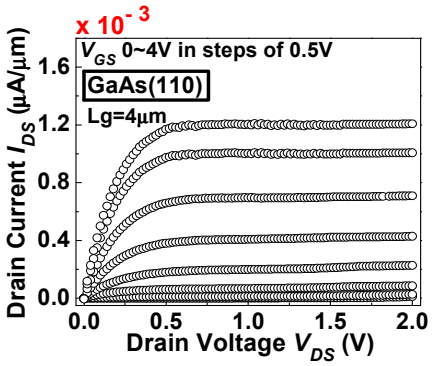

Fig. 3 Output characteristic (I_{DS}~V_{DS}) for Al_2O_3/GaAs(110) NMOSFET with 4μm gate length. The maximum drain current is 1.2x10^{-3} μA/μm.

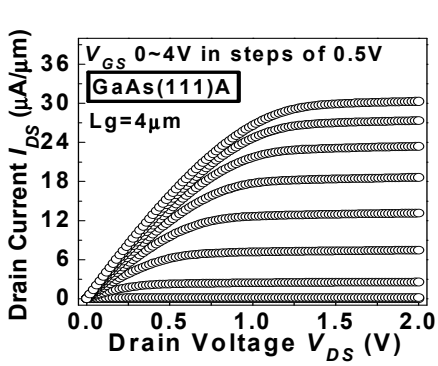

Fig. 4 Output characteristic (I_{DS}~V_{DS}) for Al_2O_3/GaAs(111)A NMOSFET with 4μm gate length. The maximum drain current is 30 μA/μm.

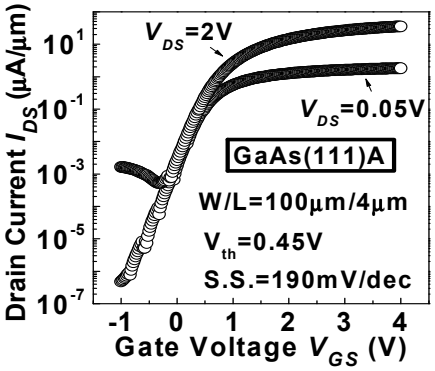

Fig. 5 Transfer characteristic of 4μm gate length NMOSFET on GaAs(111)A. I_{on}/I_{off} (@ V_{DS}=2V) is about 1.28×10^4.

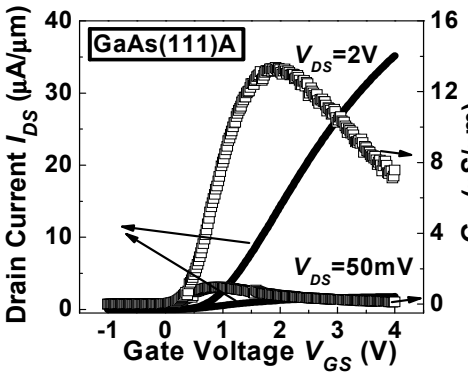

Fig. 6 Trans-conductance (G_m) versus gate bias (V_{GS}) of 4μm gate length NMOSFET on GaAs(111)A. The peak G_m is 14μS/μm.

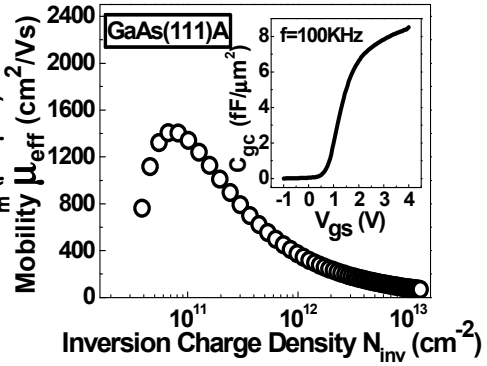

Fig. 7 Effective mobility μ_{eff} from 20μm gate length NMOSFET on GaAs(111)A. The peak electron effective mobility is 1402 cm^2/Vs.

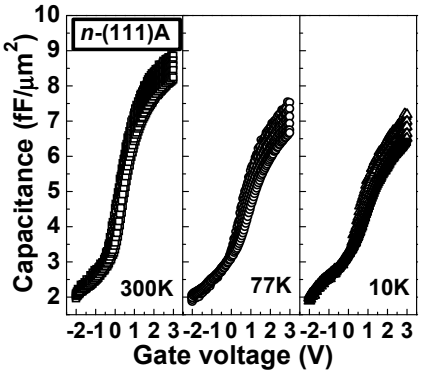

Fig. 8 C-V of Ni/8nm-Al_2O_3/n-GaAs(111)A measured at 300K, 77K, 10K. The small drop of the accumulation capacitance is caused by reduction of accumulation charge at low temperatures.

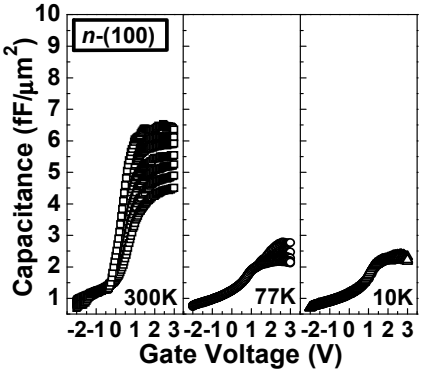

Fig. 9 C-V of Ni/8nm-Al_2O_3/n-GaAs(100) measured at 300K, 77K, 10K. The significant drop of the accumulation capacitance is caused by the partial Fermi-level pinning at a certain location in the band-gap.

n-GaAs Surfaces	I_{DS} (μA/μm) @V_{GS}=3V	$C_{max,10K}/C_{ox}$	(E_C-E_F) (eV)
(111)A	24	82%	-0.04
(111)B	---	32%	0.4
(110)	7.0x10^{-4}	33%	0.2
(100)	2.0x10^{-4}	28%	0.3

Table 2 Summary of surface band bending at the final bias on the 4 different GaAs surfaces. The negative value on (111)A surface demonstrates real accumulation is achieved. On the other 3 surfaces, the positive band bending means Fermi-level is partially pinned at some certain locations. The (E_C-E_F) is consistent with the corresponding drain current.

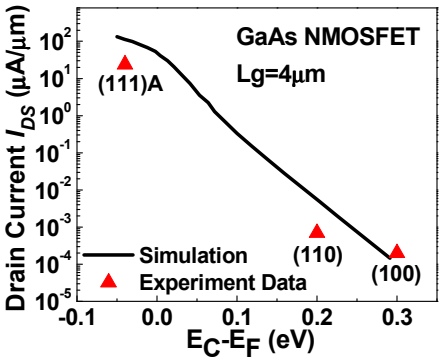

Fig. 10 Simulated drain current as a function of Fermi-level location E_F relative to the conduction band edge E_C. The experimental data (in Table 2) follows the simulation line well, showing the extracted (E_C-E_F) in Table 2 is valid.

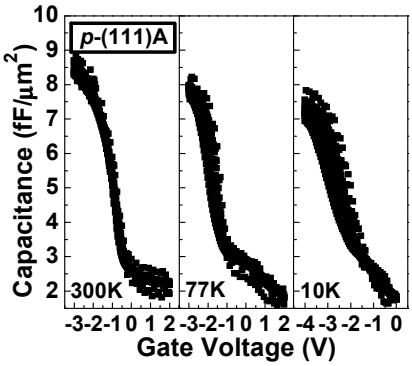

Fig. 11 C-V of Ni/8nm-Al_2O_3/p-GaAs(111)A measured at 300K, 77K, 10K. Similar to that on n-GaAs(111)A, there is a small drop of the accumulation capacitance, which is caused by the reduction of accumulation charges at low temperatures.

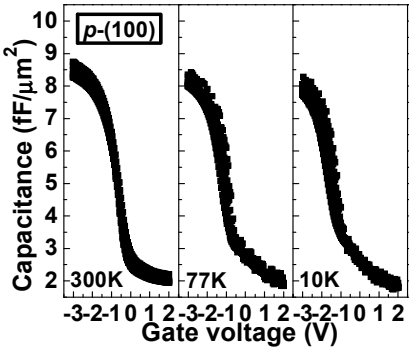

Fig. 12 C-V of Ni/8nm-Al_2O_3/p-GaAs(100) measured at 300K, 77K, 10K. Unlike that on n-GaAs(100), there is only a small drop of the accumulation capacitance. This indicates that the Fermi-level is not pinned when moving towards the valence band edge E_V.

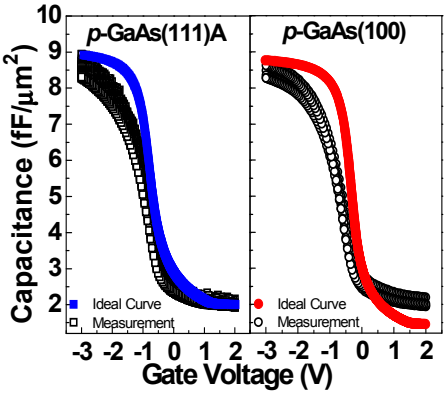

Fig. 13 Ideal high-frequency C-V plots at 27°C. On p-GaAs(111)A, the ideal curve fits very well at both accumulation and inversion sides, demonstrating that Fermi-level can move across the whole band gap. On p-GaAs(100), there is a discrepancy at inversion side, indicating the Fermi-level cannot reach strong inversion.

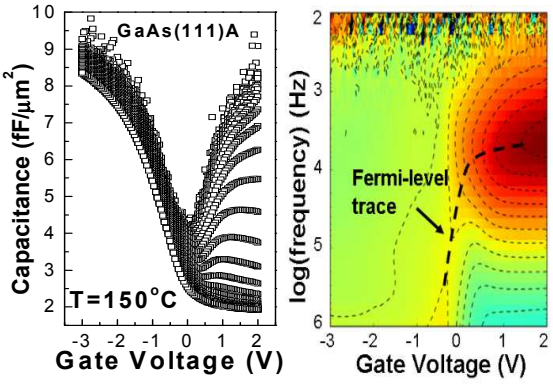

Fig. 14 *C-V* plot of Ni/8nm-Al_2O_3/p-GaAs(111)A at 150°C (left). It shows clear inversion characteristics. The corresponding *G-V* plot from 100Hz to 1MHz (right) shows the Fermi-level trace turns to be independent of frequency at 10 KHz, demonstrating real minority carrier (electron) response from inversion.

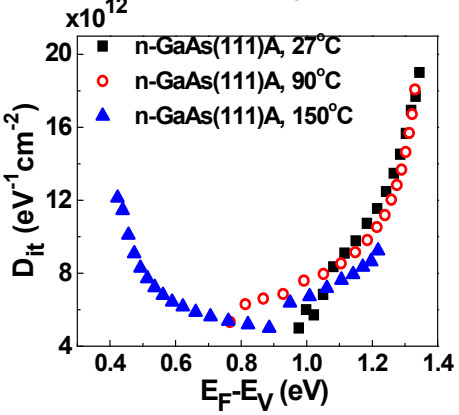

Fig. 15 Interface trap density extracted from temperature-dependent conductance method. There is no detectable peak distribution in the mid of bandgap. This is beneficial to move the Fermi-level on (111)A across the whole bandgap, compared to a possible peak distribution on GaAs(100) surface which is an obstacle to the Fermi-level movement.[7]

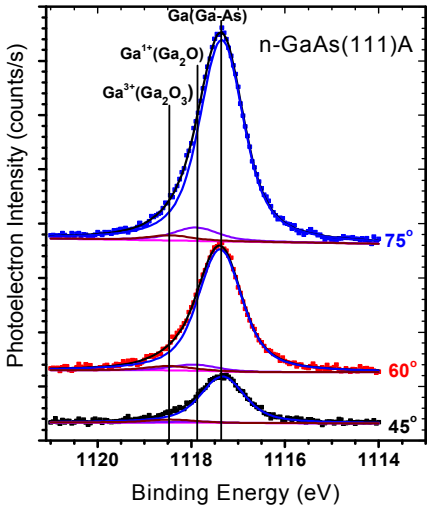

Fig. 16 XPS spectra of Ga 2p region at different take-off angles. Ga-oxides are near the detection limit for GaAs(111)A surface. More Ga-oxides are detected on (111)B, (110) and (100) surfaces.

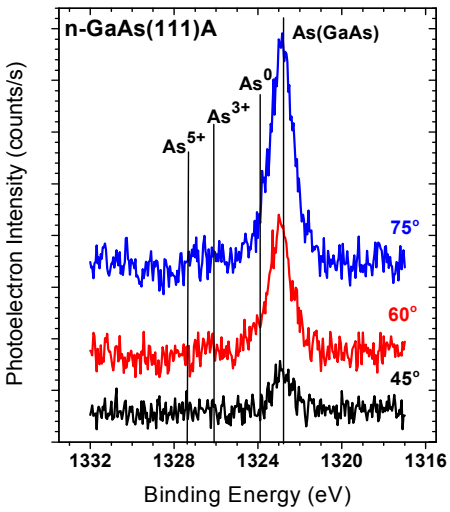

Fig. 17 As 2p XPS spectra at different take-off angles. Minimal As-oxides are detected at the interface for the GaAs(111)A surface. Similar results are seen for (110) and (100).

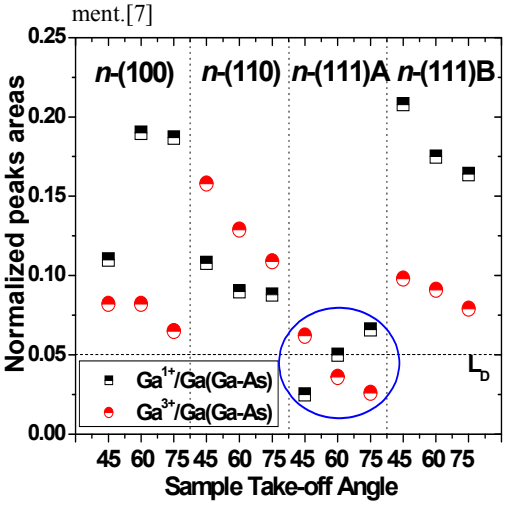

Fig. 18 Ga 2p XPS peak area ratios for various GaAs surface orientations and take-off angles. The GaAs(111)A surface has minimal Ga-oxide formation compared to the other orientations. L_D notes the detection limit. This correlates with the Fermi-level unpinning on GaAs (111)A from surface analysis.