Observation of quantum-Hall effect in gated epitaxial graphene grown on SiC (0001)

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Epitaxial graphene films examined were formed on the Si-face of semi-insulating 4H-SiC substrates by a high temperature sublimation process. A high-*k* gate stack on the epitaxial graphene was realized by inserting a fully oxidized nanometer thin aluminum film as a seeding layer, followed by an atomic-layer deposition process. The electrical properties of epitaxial graphene films are retained after gate stack formation without significant degradation. At low temperatures, the quantum-Hall effect in Hall resistance is observed along with pronounced Shubnikov–de Haas oscillations in diagonal magnetoresistance of gated epitaxial graphene on SiC (0001). © *2009 American Institute of Physics*. [doi:10.1063/1.3254329]

Graphene, a monolayer of carbon atoms tightly packed into a two-dimensional (2D) hexagonal lattice, has recently been shown to be thermodynamically stable and exhibits astonishing transport properties, such as an electron mobility of $\sim 15\,000$ $cm^2/V\,s$ and an electron velocity of $\sim 10^8$ cm/s at room temperature.[1] High-quality monolayer graphene has been obtained in small (tens of microns) areas by exfoliation of highly ordered pyrolytic graphite and transferred onto SiO_2 substrates for further device fabrication.[2,3] However, this exfoliation process cannot form the basis for a large-scale manufacturing process. Recent reports of large-area epitaxial graphene by thermal decomposition of SiC wafers have provided the missing pathway to a viable electronics technology.[4–9] An interesting question that remains to be addressed is whether the electrical properties of epitaxial graphene on SiC are essentially same as those in exfoliated graphene films.[10,11] For example, the well-known quantum-Hall effect (QHE), a distinguishing feature of a 2D electronic material system, has not been observed up to now in epitaxial graphene.[4]

The advantage of epitaxial graphene for nanoelectronic applications resides in its planar 2D structure that enables conventional top-down lithography and processing techniques. Except for opening the bandgap by forming graphene nanoribbons, an additional challenge for graphene based electronics is the formation of high-quality, ultrathin dielectrics with low interface trap density. A perfect graphene surface is chemically inert, which does not lend itself to conventional atomic-layer deposited (ALD) high-*k* dielectrics.[12–14] In this Letter, we report on ALD high-*k* gate stack integration on epitaxial graphene films by inserting a fully oxidized aluminum film as a seeding layer.[15] The gate stack formation does not degrade the electrical properties of epitaxial graphene films. The QHE is observed in gated epitaxial graphene films on SiC (0001), along with pronounced Shubnikov–de Haas (SdH) oscillations in magnetotransport.

The graphene films were grown on semi-insulating 4H-SiC substrates in an Epigress VP508 SiC hot-wall chemical vapor deposition reactor. The off-cut angle of the substrate is nominally 0°. Prior to growth, substrates are subjected to a hydrogen etch at 1600 °C for 5 min, followed by cooling the samples to below 700 °C. After evacuating hydrogen from the system, the growth environment is pumped to an approximate pressure of 2×10^{-7} mbar before temperature ramping at a rate of 10–20 °C/min and up to a specified growth temperature.

The growth conditions, film morphology, and electrical properties of the epitaxial graphene films differ markedly between films grown on the C-face and films grown on the Si-face. The formation of graphene on C-face is very rapid at the growth temperature of 1500–1650 °C in vacuum. At growth temperatures ≥1550 °C, several-micron large regions of smooth graphene films are obtained with tens of nanometers high ridges as domain boundaries.[16] Without gate stacks, the multilayer graphene films on C-face are mostly p-type with a typical Hall mobility of 5000–6000 $cm^2/V\,s$. On Si face, continuous few-layer graphene only starts to form at 1550 °C. The growth on Si-face is much slower, making it possible to form single layer graphene with a better controlled process.[17] The morphology of graphene films on the Si-face is quite homogenous compared with those films on the C-face. However, the typical Hall mobility of graphene on Si-face is $\sim 1300–1600$ $cm^2/V\,s$. The carriers are always n-type from Hall measurements without gate dielectrics. The particular graphene films shown in this Letter were grown at 1600 °C for 10 min in vacuum.

The detailed device structure is shown in Fig. 1(a). The device isolation was achieved by O_2 plasma mesa dry etching. 1 nm of aluminum metal film was evaporated onto the sample by electron-beam evaporation at $\sim 10^{-6}$ Torr and fully oxidized in an oxygen rich ambient for 1 h as a seeding layer for ALD growth. 30 nm Al_2O_3 as gate dielectric was deposited at 300 °C using an ASM F-120 reactor with trimethyl aluminum and water vapor as the precursors. The metal

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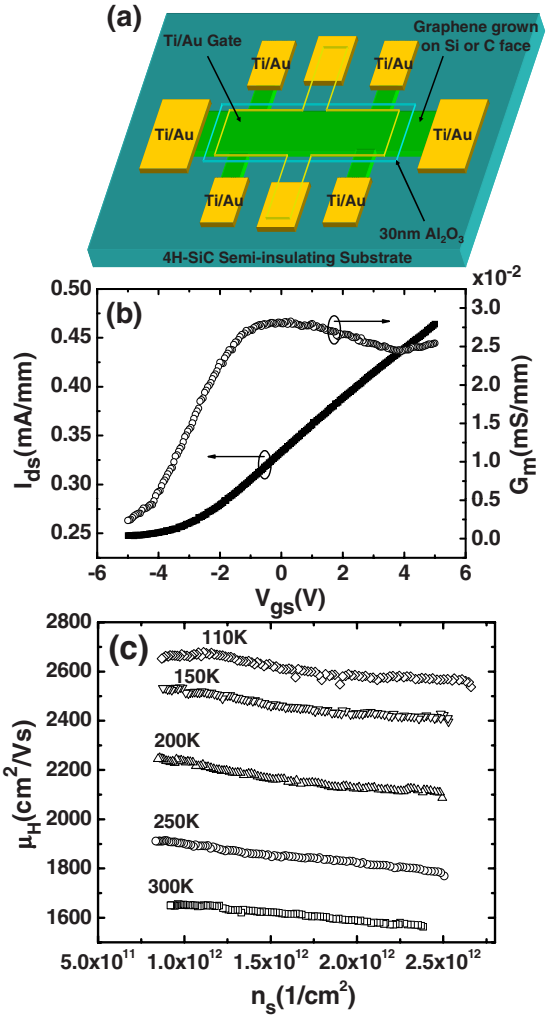

FIG. 1. (Color online) (a) Schematic view of the graphene Hall-bar device structure on SiC (0001) with ALD Al_2O_3 as gate dielectric. (b) Drain current (left) and transconductance (right) vs gate bias at drain voltage of 50 mV for the fabricated graphene FET, as shown in (a). (c) Hall mobility of the epitaxial graphene on SiC (0001) vs carrier density at various measurement temperatures.

contacts and gate electrodes were subsequently patterned and deposited, both using electron-beam evaporated Ti/Au. The active device area for magnetotransport has a width of 10 μm and a length of 22 μm. Four-point magnetotransport measurements are performed in a 1T Abbess Hall system (110–300 K) or a variable temperature (0.4–70 K) ^{3}He cryostat in magnetic fields up to 18 T using standard low frequency lock-in technique. The external magnetic field (B) is applied normal to the graphene plane.

Figure 1(b) shows the dc I_{ds}-V_{gs} and G_m-V_{gs} characteristics with a gate bias from −5.0 to 5.0 V and V_{ds}=50 mV on a Hall-bar device with a partially covered gate, as shown in Fig. 1(a). The left and right terminals of the Hall-bar serve as source and drain. The measured graphene field-effect transistor (FET) has a designed gate length (L_g) of 30 μm and a gate width (L_w) of 10 μm. The drain current can be modulated by ~46% with a few volts gate bias, similar to the previous work with SiO_2 as gate dielectric.[5] The device cannot be turned off due to the zero bandgap of graphene films. The monotonic reduction in drain current with negative gate bias also confirms that the carriers in graphene films on SiC (0001) are n-type. The slope of the drain current shows that

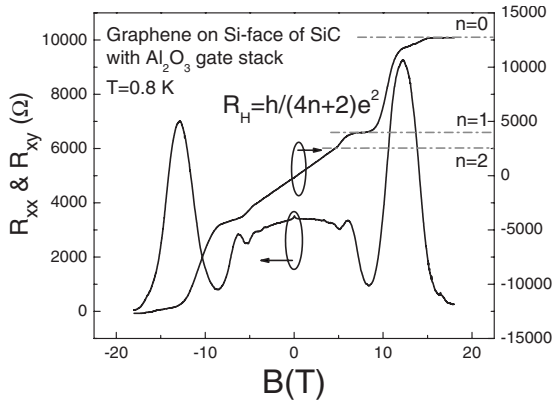

FIG. 2. Hall resistance and magnetoresistance measured in the device in Fig. 1(a) at T=0.8 K and with floating gate bias. The horizontal dashed lines corresponding to $h/(4n+2)e^2$ values. The QHE of the electron gas in epitaxial graphene is shown one quantized plateau and two developing plateau in R_{xy} with vanishing R_{xx} in the corresponding magnetic field regime.

the peak extrinsic transconductance (G_m) is ~2.8 $\times 10^{-2}$ mS/mm, due to its extraordinarily large gate length and low drain bias. The channel mobility cannot be accurately measured by field-effect mobility $\mu = [(\Delta I_d/V_{ds})/(L_w/L_g)]/C_{ox}\Delta V_{gs}$ due to the following reasons. Here, C_{ox} is determined by $\varepsilon_0\varepsilon_r A/d$, where ε_0 is the permittivity of free space, ε_r is 8.0 for ALD Al_2O_3 without annealing, A is the unit area, and d is the gate oxide thickness. First, quantum capacitance plays a critical role for single-layer graphene[18] instead of multilayer graphene.[5] Second, the real voltage across the modulated gate area is much smaller than V_{ds} because of the partial gate design and the highly resistive area of graphene not covered by the gate. Third, the channel mobility could be underestimated without correction of bulk and interface traps.[19] The most straightforward method to directly measure the mobility is the Hall measurement.

The Hall mobility and electron density of the graphene film are characterized at different gate biases and at different temperatures in Fig. 1(c). The room temperature Hall mobility is ~1600 cm^2/V s and decreases slightly with the increase in electron densities. There is also no significant Hall mobility degradation with gate stacks as compared with similar devices without gate dielectrics, indicating that the gate dielectric has reasonable quality without significant bulk traps and interface traps. The Hall mobility increases rapidly as temperature decreases and reaches ~2600 cm^2/V s at 110 K, and ~3600 cm^2/V s at 4.2 K due to the suppression of electron-phonon scattering in epitaxial graphene films. So far the low-temperature mobility in epitaxial graphene is about three orders of magnitude lower than that in modulation-doped GaAs and also about one-two orders of magnitude lower than that in suspended exfoliated graphene. We ascribe it mainly due to the defects, impurities, and domain boundaries induced by the high-temperature sublimation process.

Figure 2 shows the magnetoresistance R_{xx} and the Hall resistance R_{xy} as a function of magnetic field B from −18 to 18 T at 0.8 K. From the Hall slope, the electron density is determined to be 1.04×10^{12}/cm^2 and Hall mobility of 3580 cm^2/V s at 0.8 K. At high magnetic fields, R_{xy} exhibits a plateau, while R_{xx} is vanishing, which is the fingerprint of the QHE and SdH oscillations. One well-defined plateau with value ($h/2e^2$) is observed at $|B|>15.5$ T, while two

higher-order plateaus are developing with values of $(h/6e^2)$ and $(h/10e^2)$, respectively. The pronounced SdH oscillations with at least four distinguishable peaks are also observed at the corresponding magnetic fields. The precision of the plateau is better than 1 part in 10^4 within the instrumental uncertainty. It shows the QHE in epitaxial graphene is also applicable for metrology applications. The R_{xy} quantization in this epitaxial graphene film is in accordance with $[h/(4n+2)e^2]$, where n is the Laudau level index, found in exfoliated graphene as a distinguishing feature of Dirac Fermions. It is significantly different from conventional Fermi electrons with plateaus of (h/ne^2). The observed well-defined QHE reproduces the unique features observed in exfoliated single-layer graphene including a Berry phase of π. The observed QHE on this epitaxial graphene confirms that epitaxial graphene on SiC (0001) and exfoliated single-layer graphene are governed by the same relativistic physics with Dirac Fermions as transport carries.[1–3] Due to the relatively thick graphene films on the C-face of SiC grown under similar conditions, no QHE is observed on C-face fabricated devices.

In conclusion, a high-k gate stack on epitaxial graphene is realized by inserting a fully oxidized nanometer thin aluminum film as a seeding layer followed by an atomic-layer deposition process. The electrical properties of epitaxial graphene films are sustained after gate stack formation without significant degradation. At low temperatures, the QHE is observed in epitaxial graphene on SiC (0001), along with pronounced SdH oscillations. This quantum experiment confirms that epitaxial graphene on SiC (0001) shares the same relativistic physics as the exfoliated graphene. During the preparation and revision of this manuscript we became aware of similar observations of the graphene-like QHE on both Si-face and C-face of SiC substrates.[20–22]

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