Main determinants for III–V metal-oxide-semiconductor field-effect transistors (invited)

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(Received 2 December 2007; accepted 10 March 2008; published 30 June 2008)

Lacking a suitable gate insulator, practical GaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) have remained all but a dream for more than four decades. The physics and chemistry of III–V compound semiconductor surfaces or interfaces are problems so complex that our understanding is still limited even after enormous research efforts. Most research is focused on surface pretreatments, oxide formation, and dielectric materials; less attention is paid to the III–V substrate itself. The purpose of this article is to show that device physics more related to III–V substrates is as important as surface chemistry for realizing high-performance III–V MOSFETs. The history and present status of III–V MOSFET research are briefly reviewed. A model based on the charge neutrality level is proposed to explain all experimental work he performed on III–V MOSFETs using *ex situ* atomic-layer-deposited high-*k* dielectrics. This model can also explain all reported experimental observations on III–V MOSFETs using *in situ* molecular-beam-expitaxy-grown $Ga_2O_3(Gd_2O_3)$ as a gate dielectric. Related perspectives are also discussed to understand III–V MOS capacitance-voltage measurements. © *2008 American Vacuum Society.* [DOI: 10.1116/1.2905246]

I. INTRODUCTION

GaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) have been a subject of study for several decades. The renewed research thrust is for advanced ultralarge-scale-integration digital applications or complementary metal-oxide-semiconductor (CMOS) technology beyond the 22 nm node by using III–V compound semiconductors as conduction channels to replace traditional Si or strained Si, integrating novel high-*k* dielectrics with these high-mobility materials, and heterogeneously incorporating them on Si or silicon on insulator. The main obstacle to realizing a GaAs MOSFET technology with commercial value is the lack of high-quality, thermodynamically stable gate dielectric insulators on GaAs or III–V that can match device criteria similar to SiO_2 on Si. Our understanding of the interface physics and chemistry of III–V's is still quite limited, though enormous research efforts have been invested in this field. The literature on this subject covers the past 40 years and appears in many journals and conference proceedings. Understanding these studies requires considerable effort by seasoned researchers, and even more for those new in the field. The purpose of this article is to (i) provide readers with a brief overview on the history and current status of III–V MOSFET research, (ii) propose the charge-neutrality-level (CNL) based model to explain all experimental work on III–V MOSFETs using *ex situ* atomic-layer-deposited (ALD) high-*k* dielectrics and also *in situ* molecular-beam-expitaxy (MBE) grown $Ga_2O_3(Gd_2O_3)$ gate dielectric, and (iii) provide some guidelines for III–V MOS interface studies.

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II. HISTORY AND CURRENT STATUS

The advantage of GaAs MOSFET over its Si counterpart has long been recognized because the electron mobility in GaAs is five or more times higher than that in Si. The GaAs MOSFET research has its own phenomenal cycles coincidently with the well-known ten-year semiconductor industrial business cycles. The first GaAs MOSFET work was reported by Becke and White by the Radio Corporation of America in 1965.[1,2] Although deposited SiO_2 is used as the gate dielectric with a large amount of interface traps, the devices are successfully operated in the several-hundred-megahertz frequency range showing the feasibility of this approach. It was quickly realized that SiO_2 is not the right gate dielectric for GaAs, which sparked an enormous research effort in the following decades with a search for a low-defect, thermal-dynamically stable gate dielectric for GaAs. The efforts can be divided into two sceneries: deposited oxide and native oxide.

A variety of dielectrics and techniques have been investigated. The well-studied dielectrics on GaAs include pyrolytically deposited silicon dioxide,[1] silicon nitride,[2] silicon oxynitride,[3] and aluminum oxide.[4] All these processes require relatively high temperatures ranging from $\sim$350 to $\sim$600 °C. The chemical reaction between GaAs and oxygen in gas ambient is expected to form Ga oxide, As oxide, and even a large number of vacancies due to the high volatility of As. A low-temperature process is believed to be essential for obtaining a high-quality interface.[5] Plasma-enhanced deposition with the process temperature lower than 200 °C was attempted,[6] though it could potentially induce more defects or fixed charges on the GaAs surface or interface due to the induction of plasma.

In addition to conventional physical vapor deposition and chemical vapor deposition (CVD), MBE approach was also used to form insulating films on GaAs after it began to be widely used to grow III–V compound semiconductor heterostructures at the end of 1970s. For example, high-resistive AlGaAs (Ref. 7) or low-temperature-grown GaAs (Ref. 8) were used as an insulating layer for the GaAs channel. However, relatively high gate leakage current limits the wide application of these approaches. To improve the barrier heights at the heterojunction interface, thermal oxidation of AlAs epilayers grown on GaAs using MBE was also investigated.[9] The difficulty of this approach is to control the oxidation process to terminate at the AlAs–GaAs interface, though the large difference exhibits in the rate of oxide formation of AlAs and GaAs. The research in this direction is still currently active.[10]

Motivated by the success of thermally oxidized SiO_2 on Si, using native oxides on GaAs as gate dielectrics was also intensively studied at the very beginning. Some representative approaches include thermal oxidation,[11] wet-chemical anodization,[12,13] dc and rf plasma oxidation,[14–18] laser-assisted oxidation,[19] vacuum ultraviolet photochemical oxidation,[20] and photowash oxidation.[21] None is optimistic as a feasible approach leading to a commercial GaAs MOSFET technology. One general observation is that the native oxide is not stable, mostly leaky with low dielectric breakdown strength, and cannot be forward biased beyond a few volts. All these studies are essential to enrich our understanding of chemistry and physics properties of III–V interfaces. Although some controversies exist within much experimental data, there is consensus that a significant amount of As_2O_3, As_2O_5, and elemental As in native oxides pin the Fermi level of GaAs and are not favorable for an ideal gate dielectric. The book *Physics and Chemistry of III–V Compound Semiconductor Interfaces*, edited by C.W. Wilmsen and published in 1985, summarizes most of the experimental work of the 1970s and early 1980s.[22]

A variety of models on semiconductor interfaces were also developed at the same time beyond the Mott-Schottky model (1938), Bardeen's surface states model (1947) and Anderson's electron affinity model (1962). Some representative works include Cowley and Sze's interfacial layer model (1965),[23] Heine's metal induced gap state model (1965),[24] Tejedor and Flores' model on line-up at CNL (1978),[25] Spicer's unified defect model (UDM) (1980),[26] Hasegawa and Ohno's disorder-induced gap state (DIGS) model (1986),[27] and Tersoff's dielectric midgap energy model (1984 and 1985).[28,29] All these works strongly influenced semiconductor device research, including III–V MOS. For example, Spicer's extensive experiments, published in 1980, concluded that the Schottky-barrier formation on III–V semiconductors is due to defects formed near the interface by deposition of the metal or any chemisorption of oxygen.[30] This model also applies to the formation of states at III–V oxide interface states. Fermi-level position in GaAs is pinned at the midgap whether or not it is a metal-semiconductor or oxide-semiconductor interface.

Fermi-level pinning in III–V semiconductors dampened the enthusiasm among III–V researchers to compete with Si in large-scale integrated circuits. However, significant progress was made on high-performance microwave GaAs metal-semiconductor field-effect transistors, pioneered by Hooper and Lehrer,[31] using a GaAs Schottky barrier directly. The development of MBE and metal-organic CVD technologies in the 1970s made heterojunctions, quantum wells, and superlattices practical. In Bell Labs, Dingle *et al.* first demonstrated enhanced mobility in the AlGaAs/GaAs modulation-doped superlattice in 1978.[32] Stormer *et al.* subsequently reported a similar effect using a single AlGaAs/GaAs heterojunction,[33] which led to the discovery of the fractional quantum Hall effect in 1981. In 1980, a Japanese group led by Mimura applied a similar concept and invented the high-electron-mobility transistor (HEMT).[34] Similar work was also reported later the same year by Delagebeaudeuf and others.[35] GaAs HEMT eventually became a commercialized technology, finding broad applications in the communication, military, and aerospace industries today. GaAs MOSFET research did not continue on a large scale after the successful introduction of GaAs HEMT.

The search for suitable dielectrics or passivation layers on GaAs continues. In 1987, researchers at Bell Labs discovered that a class of sulfides [e.g., Li_2S, $(NH_4)_2S$, $Na_2S \cdot 9H_2O$] was able to passivate the GaAs surface and provide excellent electronic properties to GaAs surfaces.[36,37] The work generated new interest in GaAs MOSFETs using sulfur passivation before dielectric deposition. Hundreds of papers were published related to GaAs sulfur passivation. However, sulfur passivation did not become a technology because sulfur is an unstable material with very low thermal budget. Nevertheless, it is still very scientifically interesting. Sulfur, as a group VI element next to oxygen, has the same electron number in its outer shell as oxygen, but is less chemically reactive. A few monolayers of sulfur can passivate a pristine GaAs surface in certain conditions and prevent GaAs from oxidation to form As oxides. Sulfur passivation is still used in today's research. Other work on effective passivation of GaAs using hydrogen or nitrogen plasma was also reported by the IBM group.[38] Another interesting approach uses a very thin amorphous or crystalline Si layer as an interfacial control layer (ICL) between GaAs and SiO_2 or Si_3N_4.[39–42] This approach was intensively studied in the 1990s[43–45] and was recently adopted to integrate with high-k HfO_2 gate dielectrics on GaAs.[46–49] The real effect of this Si ICL, in particular, on capacitance-voltage (C-V) characteristics, needs further investigation.

In 1995, Passlack and Hong at Bell Labs reported that *in situ* deposition of $Ga_2O_3(Gd_2O_3)$ dielectric film on a GaAs surface by electron-beam evaporation from single-crystal $Ga_5Gd_3O_{12}$ produced MOS structures on GaAs with a low interface trap density (D_{it}).[50–52] Because the experiment is realized in an ultrahigh-vacuum (UHV) connected multichamber MBE system, it is usually called MBE-grown $Ga_2O_3(Gd_2O_3)$. A series of device work, mainly led by Hong and Ren, was done at Bell Labs after this breakthrough in

materials science. It included GaAs depletion-mode (*D*-mode) and enhancement-mode (*E*-mode) MOSFETs,[53,54] InGaAs enhancement-mode MOSFETs,[55] GaAs complementary MOSFETs,[56] and GaAs power MOSFETs.[57] This $Ga_2O_3(Gd_2O_3)$ dielectric device work continues at Agere Systems,[58] a spin-off from Bell Labs and Lucent Technologies, and National Tsinghwa University in Taiwan. In 2003, Passlack *et al.* at Motorola/Freescale began reporting on series of work modifying the previous $Ga_2O_3(Gd_2O_3)$ dielectric process and using a Ga_2O_3 template in $Gd_xGa_{0.4-x}O_{0.6}/Ga_2O_3$ dielectric stacks on GaAs.[59] An implant-free enhancement-mode device concept was introduced, and good device performance was demonstrated in 2006 to eliminate the difficulty in realizing the inversion operation due to the relative low thermal budget of III–V and gate dielectric stacks.[60] UHV scanning tunneling microscopy reveals that the unpinning of the GaAs Fermi level results from Ga_2O restoring the surface As and Ga atoms to near-bulk charge.[61]

The strong investment in research on deposited high-*k* dielectrics for Si CMOS technologies began in the late 1990s.[62] High-*k* research has since flourished, in particular, the use of ALD method for fabricating Si-based high-*k* MOS devices. At the end of 2001, Ye and Wilk at Bell Labs/Agere Systems started to work on ALD high-*k* Al_2O_3 and HfO_2 on GaAs and other III–V materials. A series of *D*-mode MOSFETs on GaAs, InGaAs, and GaN using ALD Al_2O_3 as gate dielectrics was demonstrated.[63–67] ALD is an *ex situ*, robust, and manufacturable process that attracts wider interest in academia and industry. The work on ALD integration with high-mobility channel materials continues and has been enhanced by Ye's group at Purdue University. Detailed interface studies were carried out to demonstrate the unpinning of the Fermi level in III–V semiconductors using ALD high-*k* dielectrics,[68–73] including the fundamental understanding of the ALD chemical process on GaAs reported by other groups.[74–76] High-performance inversion-mode III–V MOSFETs were demonstrated with unprecedented drain current as high as 1.05 A/mm and transcondcutance as high as 0.35 S/mm.[77–81] This is the first surface-channel device in III–V with drain current beyond 500 mA/mm. In-rich InGaAs is identified as the potential channel material for the future 22 nm technology node or beyond with higher effective mobility and manageable band gap for low drain voltage. The fundamental understanding on this successful demonstration is discussed in Sec. III. Currently, many research groups are working on ALD III–V MOSFETs.[82–85]

The new cycle of interest in III–V MOSFETs was initiated by Intel in 2005. Intel is starting to look seriously for alternative device technologies beyond Si CMOS. III–V is one of its main focuses, with the excellent publications on InSb-based quantum well transistors in collaboration with QinetiQ.[86,87] We are hoping that the current III–V research in the Si CMOS community is at the similar stage as when the high-*k* concept was introduced at the end of 1990s. After collective efforts in academia and industry, we were able to make this long-standing GaAs MOSFET dream become a real commercial technology as the successful story of high-*k* in Si CMOS.

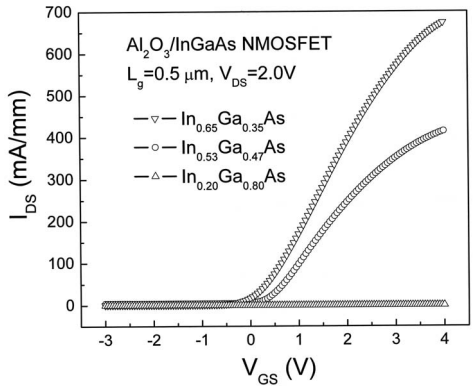

FIG. 1. I_{ds} vs V_{gs} at $V_{ds}=2$ V for $In_{0.20}Ga_{0.80}As$, $In_{0.53}Ga_{0.47}As$, and $In_{0.65}Ga_{0.35}As$ MOSFETs using Al_2O_3 as gate dielectrics.

III. CHARGE-NEUTRALITY-LEVEL MODEL FOR III–V MOSFETS

For the 22 nm technology node or beyond, only the inversion-type enhancement-mode III–V MOSFET is of interest. Inversion-mode surface-channel $In_xGa_{1-x}As$ MOSFETs with In concentrations of 20%, 53%, 65%, and 75% integrated with ALD Al_2O_3, HfO_2, and HfAlO were systematically studied at Purdue University. The details of device fabrication are described in Refs. 77–81. Figure 1 shows the comparison of dc transfer characteristic at $V_{ds}=2$ V on $In_{0.20}Ga_{0.80}As$, $In_{0.53}Ga_{0.47}As$, and $In_{0.65}Ga_{0.35}As$ MOSFETs using Al_2O_3 as the gate dielectric. The device performance has a significant jump to 430 mA/mm drain current on $In_{0.53}Ga_{0.47}As$ MOSFET, compared to 0.2 mA/mm on $In_{0.20}Ga_{0.80}As$ MOSFET, and continues improving to 670 mA/mm drain current on $In_{0.65}Ga_{0.35}As$ MOSFET. The gate length of all three devices is 0.5 μm. The maximum drain current has the potential to increase further by reducing gate length and/or implementing InGaAs channels with more In concentration.[80] Note that most commercial GaAs technology, such as pseudomorphic HEMT (pHEMT), has a maximum drain current around 400 mA/mm at 0.25 μm gate length. For GaAs pHEMT, due to its high low-field mobility, the maximum drain is mainly limited by the saturation velocity, modulation doping concentration, and heterostructure itself. The maximum drain current saturates at 5–10 μm gate length and does not scale with gate length for short gate-length devices. In contrast to GaAs pHEMT, the demonstrated surface-channel InGaAs MOSFET, similar to real Si MOSFET, has gate-length scalability down to the submicron scale.[77–81] Record high maximum drain current of 1.05 A/mm is demonstrated by reducing gate length to 0.4 μm.[81] The maximum inversion current is also related to electrical-field-induced surface potential or band bending. With further improved interface quality and improved het-

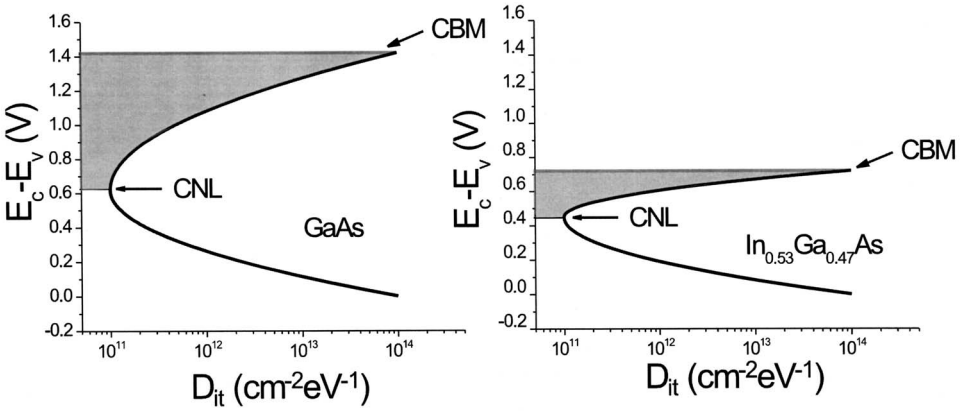

FIG. 2. Schematic for the parabolic D_{it} distribution within energy band of GaAs and $In_{0.53}Ga_{0.47}As$. The CNL is aligned 0.8 eV below CBM for GaAs and 0.27 eV below CBM for $In_{0.53}Ga_{0.47}As$. The shadow area shows the built-up negative charges in interface traps after Fermi level moves from CNL to CBM. All calculated values are listed in Table I.

erostructure design, the maximum drain current could be much higher than the value offered by the doped GaAs pHEMT technology.

We ascribe this improvement to two determinants. First, the ALD dielectric process, in particular, trimethylaluminum-related Al_2O_3, enables unpinning the Fermi levels on III–V semiconductors, in general. The simplified surface preparation for ALD on III–V is as follows.[88] Before surface treatment, all wafers underwent standard degrease process using acetone, methanol, and isopropanol. The NH_4OH treatment is carried out by soaking the samples in NH_4OH (29%) solution for 3 min to remove native oxide and rinsing in flowing de-ionized water followed by gently drying the surface using N_2 blow gun. The NH_4OH etching step removes most of arsenic and gallium oxides from the surface. The further ALD process results on the disappearance of arsenic oxides and self-cleaning of GaAs surface.[64,74–76,89] The interface quality could be further improved sometimes by $(NH_4)_2S$ treatment. The process is to soak the sample in $(NH_4)_2S$ for 10 min in room temperature and dry using N_2 gun. With these appropriate surface pretreatments, the interface trap density in the range of low 10^{11}-low $10^{12}/cm^2$ eV can be realized and the inversion-type enhancement-mode MOSFETs can be demonstrated, as shown in Fig. 1. During the past decades, the research community mainly focused on dielectric materials and III–V surface chemistry study, and paid less attention to device physics of III–V MOSFET. We emphasize that device physics is also extremely important as the second determinant for realizing high inversion current due to the smaller energy-level separation between the CNL of In-rich InGaAs and the conduction-band minimum (CBM), compared to GaAs. The simple CNL-based model below can explain all experimental works on III–V MOSFETs using *ex situ* ALD high-*k* dielectrics and also *in situ* MBE-grown $Ga_2O_3(Gd_2O_3)$ gate dielectric.

A difficult problem with III–V MOSFETs results from the unpassivated dangling bonds on III–V free surfaces. The energy locations of the dangling bonds are directly related to the bulk band structures of different III–V semiconductors. However, in the tight-binding formalism, the conduction and valence bands are formed as bonding and antibonding combinations of the atomic sp^3 hybrids. That is why the dangling-bond energy is typically located in the middle of the band gap.[90] There are many experimental studies that quantitatively measure the midgap energies of various semiconductors. There are also many theoretical studies using sophisticated techniques (such as metal induced gap state model, unified defect model, and disorder-induced gap state model) to quantitatively calculate the electronic energies. To simplify our explanation, we choose one internal reference level called CNL, as illustrated in Fig. 2, to phenomenologically explain all our experimental observations. Presumably, every interface has donor-type and acceptor-type interface traps. A convenient notation is to interpret the sum of these by an equivalent D_{it} distribution, with an energy level called charge-neutrality level E_{CNL}. If Fermi level E_F is above E_{CNL}, the states are of acceptor type and negatively charged if the states are occupied. If Fermi level E_F is below E_{CNL}, the states are of donor type and positively charged if the states are occupied.[91] A recent review on CNL relevant for III–V materials can be found in Ref. 92. CNL concept is also applied to explain the experimental results from Ge MOSFETs.[93]

Figure 2 illustrates the basic idea to qualitatively understand the transistor output characteristic of Fig. 1. The model is extremely simplified to highlight the fundamental point with a few assumptions. First, the D_{it} distribution from valence-band maximum to CBM is parabolic in a logarithm scale. This is a reasonable assumption because the interface traps at III–V interfaces are more significant, compared to the SiO_2/Si interface with a U-shaped distribution. Second, the D_{it} value at CBM is fixed at $10^{14}/cm^2$ eV for simplification. Third, Fermi-level stabilization energy[94] is chosen as CNL energy with values listed in Table I. Assuming the strong electron inversion occurs when the Fermi level reaches CBM, the number of interface-trapped negative charges can easily be calculated by integrating D_{it} from CNL to CBM and are listed in Table I with different D_{it} values at CNL. It is obvious now that the dominant factor is the energy difference between CNL and CBM. For GaAs, with the CNL and CBM difference as large as ~0.8 eV, it builds up 1.02×10^{-6} C/cm^2 negative charges to prevent a strong inversion charge to participate in transport. In contrast, the CNL and CBM potential difference for $In_{0.65}Ga_{0.35}As$ is only 0.15 eV

TABLE I. Calculated built-in negative charges Q_{it} from CNL to CBM on different III-V substrates. In most cases of interest, the Fermi level in the semiconductor is above the CNL, resulting in a large buildup of fixed negative charge (Q_{it}) at the interface due to fillingup of acceptorlike states. $Q_{it}^{(1)}$ is for calculated built-in negative charges from CNL to CBM with $D_{it}=1\times10^{11}/\text{cm}^2\,\text{eV}$ at CNL; $Q_{it}^{(2)}$ is for $D_{it}=2\times10^{11}/\text{cm}^2\,\text{eV}$ at CNL; $Q_{it}^{(3)}$ is for $D_{it}=5\times10^{11}/\text{cm}^2\,\text{eV}$ at CNL; $Q_{it}^{(4)}$ is for $D_{it}=1\times10^{12}/\text{cm}^2\,\text{eV}$ at CNL.

	E_g (eV)	E_{CBM}-E_{CNL} (eV)	$Q_{it}^{(1)}$ (C/cm^2)	$Q_{it}^{(2)}$ (C/cm^2)	$Q_{it}^{(3)}$ (C/cm^2)	$Q_{it}^{(4)}$ (C/cm^2)
GaAs	1.42	0.80	1.02×10^{-6}	1.15×10^{-6}	1.38×10^{-6}	1.63×10^{-6}
$In_{0.53}Ga_{0.47}As$	0.73	0.27	3.44×10^{-7}	3.88×10^{-7}	4.67×10^{-7}	3.44×10^{-7}
$In_{0.65}Ga_{0.35}As$	0.61	0.15	1.91×10^{-7}	2.16×10^{-7}	2.59×10^{-7}	3.06×10^{-7}
$In_{0.75}Ga_{0.25}As$	0.52	0.06	6.37×10^{-8}	7.19×10^{-8}	8.65×10^{-8}	1.02×10^{-7}

assuming a linear extrapolation exhibited in $In_xGa_{1-x}As$ binary and ternary alloys[95] and CNL for InAs is at 0.2 eV above CBM.[96] The built-up negative charge is only 1.91×10^{-7} C/cm^2, a factor of 5 smaller than that in GaAs. That explains why an $Al_2O_3/In_{0.20}Ga_{0.80}As$ MOSFET (Ref. 68) has much less maximum drain current than an $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSFET (Refs. 77–79) and $Al_2O_3/In_{0.65}Ga_{0.35}As$ MOSFET.[80,81] It also explains why $Ga_2O_3(Gd_2O_3)/GaAs$ MOSFETs have only less than 1 mA/mm drain current[53] and $Ga_2O_3(Gd_2O_3)/In_{0.53}Ga_{0.47}As$ MOSFET has 360 mA/mm drain current.[55] InP is another interesting material to double check the applicability of the above model. InP has a band gap of 1.35 eV, which is very similar to 1.42 eV of GaAs. However, the potential difference between CNL and CBM for InP is only ~0.5 eV.[28,29,90] It is much easier to realize an inversion-mode InP MOSFET than a GaAs MOSFET. 100 mA/mm drain current InP MOSFETs have been demonstrated using ALD high-k dielectrics.[97,98] The interface quality of $Al_2O_3/III-V$ is better than that of $HfO_2/III-V$, in general. However, the built-in charge increases less than a factor of 2 from the midgap D_{it} of $10^{11}-10^{12}/\text{cm}^2$ eV, as shown in Table I. That explains why Al_2O_3, HfO_2, HfAlO, and even in situ grown $Ga_2O_3(Gd_2O_3)$ have similar device performance on the same III–V substrate. The ALD process is obviously much more favorable, because it is *ex situ*, robust, manufacturable, and widely used in the Si industry. Compared to Hasegawa DIGS model,[27] Spicer's UDM,[30] and Brillson's work,[99] this phenomenological CNL model is more related to the band structures of III–V substrates. The interface control, which is mainly determined by dielectric materials, surface preparation, and oxide formation, is very important. However, the high-mobility substrate itself plays the most important role here.

A similar conclusion can also be reached by calculating the surface-potential or band-bending condition for strong inversion on different substrates. The strong inversion requires

$$\psi_s \approx 2\psi_B \approx \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right). \tag{1}$$

With N_A of $1\times10^{17}/\text{cm}^3$, n_i (GaAs) of $2\times10^6/\text{cm}^3$, and n_i (InAs) of $1\times10^{15}/\text{cm}^3$, it is clear that it requires much less band-bending or surface-potential movement to realize strong inversion in In-rich InGaAs than in GaAs.

The conclusion is that with decent interface quality as the precondition, the energy difference between CNL and CBM is the most important determinant for high-performance inversion-type E-mode III–V MOSFETs.

IV. ELECTRICAL CHARACTERIZATION METHODOLOGY FOR III–V MOS CAPACITORS

III–V MOS C-V measurement is widely used to characterize III–V MOS structures. It is commonly accepted that the observation of the inversion of minority carriers is conclusive evidence of whether or not the Fermi level is pinned. Most previous studies concentrated on GaAs, so quasistatic C-V was used to evaluate interface properties. Fermi-level pinning was considered the reason for failing to observe inversion features in GaAs MOS capacitors (MOSCAPs). Here, we discuss this concept from a device physics perspective to clarify some controversies.

The determinant for the III-V MOSCAP characteristic is surface recombination velocity S at the MOS interface. Recombination strongly depends on doping type and concentration through the dependence of defect occupation on the Fermi level. The rate of carrier recombination U is given by the Shockley-Hall-Read statistics

$$U = \frac{N_i\sigma_n\sigma_p\upsilon_{th}(np-n_i^2)}{\sigma_n[n+n_i\exp(E_t-E_i/kT)]+\sigma_p[p+n_i\exp(E_i-E_t/kT)]}, \tag{2}$$

where N_t is the number of deep traps at a given energy, σ_n and σ_p are the carrier capture cross sections, υ_{th} is the average thermal velocity, n and p are the carrier concentrations, n_i is the intrinsic concentration, and E_i is the energy level of the deep traps. For p-type GaAs or III-V for n-channel MOSFET, Eq. (2) can be rewritten to give the Stevenson-Keyes expression[100] or the surface recombination velocity S of electrons:

$$S = \frac{U}{\Delta n} = \frac{N_s \sigma_n \sigma_p \upsilon_n \upsilon_p p_0}{\sigma \upsilon N_b \exp(-E_{\min}/kT)}, \quad (3)$$

where N_s is the number of defects per area at the interface at a given energy, p_0 is the hole concentration, Δn is the deviation of electron density from equilibrium, N_b is the effective density of states, and $E_{\min}$ is the smaller of E_c-E_{CNL} or E_{CNL}-E_v.[90] For GaAs, E_{CNL} or E_F are both near midgap and have the highest recombination velocity. For $In_{0.53}Ga_{0.47}As$, E_{CNL} is only 0.27 eV below CBM, whose theoretical S value could be several orders of magnitude lower. It is not surprising that a recent photoluminescence experiment shows that the native oxide on an $In_{0.15}Ga_{0.85}As$ film has one order of magnitude lower surface recombination velocity than the native oxide on a GaAs film.[101] The microscopic structures of different III-V surfaces, dielectrics, and processes play a significant role in surface recombination through the number of surface states N_s. This simple calculation provides only a qualitative trend to understand the general behavior of C-V characteristics.

According to the Shockley-Read-Hall statistics and the low intrinsic carrier concentration (n_i) of $10^6/\mathrm{cm}^3$ in GaAs, the expected ac frequency to observe inversion C-V in the dark and at room temperature is very low ($\sim$0.002 Hz).[102] The condition for reliable quasistatic C-V measurements with leakage current density of less than 10^{-8} A/cm^2 is also difficult to meet on ultrathin high-k dielectrics. After understanding the principle of surface recombination velocity and frequency response of minority carrier to the ac signals by C-V measurements, we recommend three approaches to study inversion C-V on III-V in general: (i) inversion-type MOSFET with implanted source and drain, where minority carriers could be injected into the surface channel at a low drain bias; (ii) photoillumination to increase the minority-carrier concentration; and (iii) elevated temperature to increase the generation and recombination rates of minority carriers in GaAs. All these approaches are used to increase the minority carriers and reduce the recombination velocity, as shown in Eq. (3).

The minority carriers (electrons) in p-type GaAs cannot keep up with the low-frequency C-V measurement even at frequencies as low as 1 Hz in the dark and at room temperature. However, at higher temperatures or under photo- (light) illumination, more carriers are generated and their response time is significantly reduced so that the minority-carrier contribution to the capacitance can be profound. Full inversion could be observed at the Al_2O_3/GaAs interface with increasing light intensity, as shown in Fig. 3, by implementing indium tin oxide (ITO) as metal gate.[73] The conductive and transparent ITO gate enables homogenous photoillumination on the whole MOS capacitor area, such that one can easily observe the low-frequency C-V on GaAs at room temperature. We assume that the interface quality of Al_2O_3/GaAs is similar with or without light. The light-induced minority-carrier concentration and its response time for thermal generation/recombination play a more important role on inversion than the interface trap density. It is not very clear that

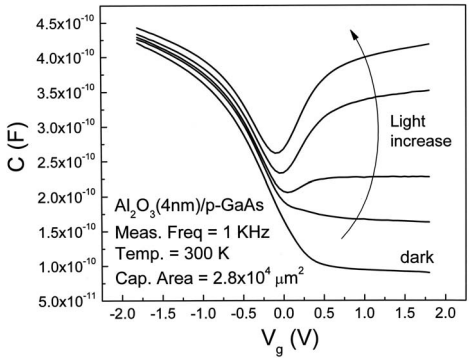

FIG. 3. Capacitance measurement at 1 kHz as a function of gate bias with increased light intensity from the microscope. Indium tin oxide is used as transparent conducting electrodes to improve light illumination on GaAs. The light intensity is simply controlled by the electrical power supplied to the microscope lamp.

the conclusive evidence for Fermi-level unpinning is the inversion or low-frequency feature in C-V measurement, or even in quasistatic C-V measurement in dark and at room temperature.

A good exercise is to integrate low-frequency capacitance and obtain the ψ_s-V relationship, a method first developed by Berglund in 1966.[103] Here, ψ_s is the surface potential and V is the gate bias. The ψ_s-V relationship is very important in interface studies since D_{it} can be directly obtained from it. The change in surface potential due to a change in applied MOS voltage from V_1 to V_2 is

$$\psi_s(V_2) - \psi_s(V_2) = \int_{V_1}^{V_2} \left[1 - \frac{C_{\mathrm{LF}}(V)}{C_{\mathrm{OX}}} \right] dV. \quad (4)$$

Using the Berglund equation, the surface-potential change on GaAs of Fig. 3 is as large as 1.1 eV, which is comparable to the GaAs band gap itself. This is a convincing experimental evidence that the Fermi level at the ALD Al_2O_3/GaAs interface is not pinned. Similar results are also obtained in InGaAs, where the band gap is even smaller. Surface-potential movement or band-bending value could be used to quantitatively study the Fermi-level pinning issue.

Similar to MOSFETs, interface trap density D_{it} or N_s in Eq. (3) is not the only determinant for C-V characteristics. The high-mobility substrate itself also plays an important role here through band gap, intrinsic carrier concentration, doping concentration, and other features. Device physics is also very important in guiding III-V MOS studies and interpreting the experimental data.

V. CONCLUSION

In summary, we briefly reviewed the history over the past 40 years and current status of III-V MOSFET research to help those new in the field to have easy access to the many existing publications. We use a simple CNL-based model to explain all reported experimental observations on inversion-type enhancement-mode ALD high-k/III-V MOSFETs and MBE $Ga_2O_3(Gd_2O_3)$/III-V MOSFETs. Conclusive evidence

on GaAs Fermi-level unpinning using ALD Al_2O_3 is presented by inversion features in *C-V* measurements and surface-potential calculations using the Berglund low-frequency capacitance method.

ACKNOWLEDGMENTS

The author would like to thank Yi Xuan, Tian Yang, and Tian Shen for the experimental results used in this article, and J. M. Woodall, H. Hasegawa, M. Hong, R. M. Wallace, G. D. Wilk, M. S. Lundstrom, and Yanqing Wu for valuable discussions. The work is supported in part by the National Science Foundation (Grant No. ECS-0621949) and the SRC FCRP MSD Focus Center.

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