Depletion-mode InGaAs metal-oxide-semiconductor field-effect transistor with oxide gate dielectric grown by atomic-layer deposition

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Recently, significant progress has been made on GaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) using atomic-layer deposition (ALD)-grown Al_2O_3 as gate dielectric. We show here that further improvement can be achieved by inserting a thin $In_{0.2}Ga_{0.8}As$ layer as part of the channel between Al_2O_3 and GaAs channel. A 1-μm-gate-length, depletion-mode, n-channel $In_{0.2}Ga_{0.8}As$/GaAs MOSFET with an Al_2O_3 gate oxide of 160 Å shows a gate leakage current density less than 10^{-4} A/cm^2, a maximum transconductance ~105 mS/mm, and a strong accumulation current at $V_{gs}>0$ in addition to buried-channel conduction. Together with longer gate-length devices, we deduce electron accumulation surface mobility for $In_{0.2}Ga_{0.8}As$ as high as 660 cm^2/V s at $Al_2O_3/In_{0.2}Ga_{0.8}As$ interface. © *2004 American Institute of Physics.*
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During the past few decades, there has been continued interest in GaAs-based metal-oxide-semiconductor field-effect transistors (MOSFETs).[1–10] GaAs-based devices potentially have great advantages over Si-based devices for high-speed and high-power applications, in part from an electron mobility in GaAs that is ~5× greater than that in Si, the availability of semi-insulating GaAs substrates, and a higher breakdown field. Currently, the GaAs metal-semiconductor field-effect transistor (MESFET) is the dominant device for high-speed and microwave circuits. MESFETs feature gates formed by metal-semiconductor (Schottky barrier) junctions, while MOSFETs have oxide layers (higher barrier) between metals and semiconductors. Compared to GaAs MESFETs, GaAs MOSFETs feature a larger maximum drain current, much lower gate leakage current, a better noise margin, and much greater flexibility in digital integrated circuit design due to large gate voltage range. The main obstacle to GaAs-based MOSFET devices is the lack of high-quality, thermodynamically stable insulators on GaAs as gate dielectric that can match the device criteria similar to SiO_2 on Si. After a decade of effort, much progress has been made recently to form a high-quality oxide on III–V semiconductors;[11–14] for example, atomic-layer deposition (ALD)-grown Al_2O_3 on III–V semiconductors,[15,16] a marriage of Si technology to the III–V compound semiconductor field.

In this letter, we report a GaAs-based MOSFET with an inserted $In_{0.2}Ga_{0.8}As$ layer as part of the channel to explore the potential of better interface quality and surface mobility. The gate dielectric is Al_2O_3 grown by ALD, which is an *ex situ*, robust manufacturing process and commonly used throughout the Si industry.[17] Al_2O_3 is a highly desirable gate dielectric with a high bandgap (~9 eV), a high breakdown field (5–10 MV/cm), a high dielectric constant (8.6–9), high thermal stability (up to at least 1000 °C), and it remains amorphous under typical processing conditions. Depletion-mode, n-channel $In_{0.2}Ga_{0.8}As$/GaAs MOSFETs show a low gate leakage current, good transconductance, and a strong accumulation current at $V_{gs}>0$. We ascribe this strong accumulation current at $V_{gs}>0$ to the improvement of oxide/channel interface or electron accumulation surface mobility by inserting an $In_{0.2}Ga_{0.8}As$ layer. We use MOSFETs of different gate lengths to deduce the series resistance and obtain a high electron accumulation surface mobility of $In_{0.2}Ga_{0.8}As$ at the $Al_2O_3/In_{0.2}Ga_{0.8}As$ interface. A high surface mobility is an indication of interface quality and is critical for realization of enhancement-mode (surface inversion channel) and complementary GaAs MOSFETs.

Figure 1 shows the device structure of the fabricated, depletion-mode, n-channel $Al_2O_3/In_{0.2}Ga_{0.8}As$/GaAs MOSFET. A 1500 Å undoped GaAs buffer layer, a 140 Å Si-doped GaAs layer (2×10^{18}/cm^3), and a 135 Å Si-doped $In_{0.2}Ga_{0.8}As$ layer (1×10^{18}/cm^3) were subsequently grown by molecular-beam epitaxy on a (100)-oriented semi-insulating 2 in. GaAs substrate. After the semiconductor epilayer growth, the wafer was transferred *ex situ* to an ASM Pulsar2000™ ALD module. A 160-Å-thick Al_2O_3 oxide layer was deposited at a substrate temperature of 300 °C. A

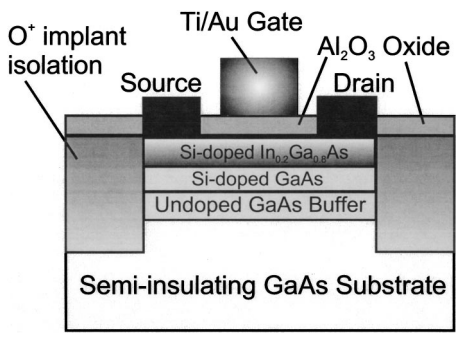

FIG. 1. Schematic view of a depletion-mode, n-channel InGaAs/GaAs MOSFET with ALD-grown Al_2O_3 as gate dielectric.

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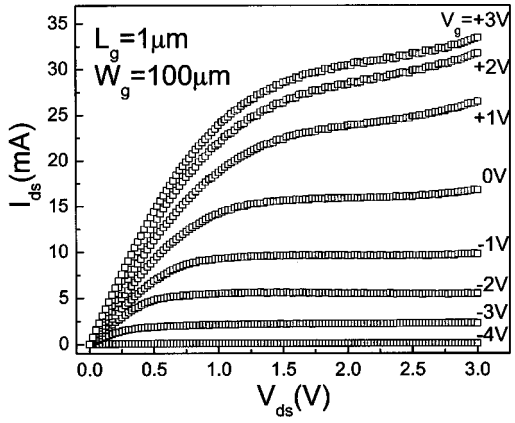

FIG. 2. Drain current vs drain bias as a function of gate bias.

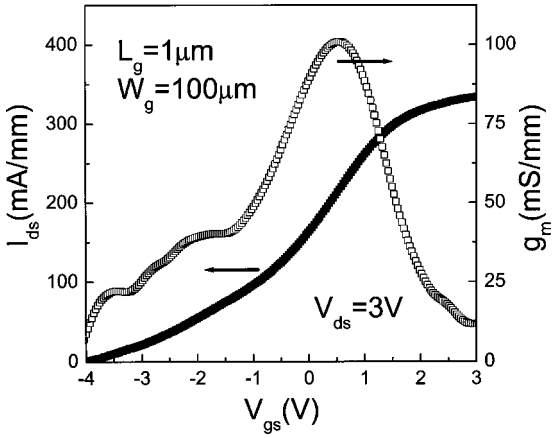

FIG. 3. The filled square line is drain current vs gate bias. The empty square line is transconductance vs gate bias. The device is in the saturation region biased at $V_{ds}=3$ V in both cases.

post-deposition anneal was done at 550 °C for 60 s in an oxygen ambient. Device isolation was achieved by oxygen implantation. Activation annealing was performed at 450 °C in a helium gas ambient. Using a wet etch in diluted HF, the oxide on the source and drain regions was removed while the gate area was protected by photoresist. Ohmic contacts were formed by electron-beam deposition of Au/Ge/Au/Ni/Au and a lift-off process, followed by a 425 °C anneal in a forming-gas ambient. Finally, conventional Ti/Au metals were e-beam evaporated, followed by lift-off to form the gate electrodes. The process requires four levels of lithography (alignment, isolation, ohmic, and gate), all done using a contact printer. The source-to-gate and the drain-to-gate spacings are ~1.0 μm. The sheet resistance of the source/drain region outside the gate and its contact resistance are measured to be 1.5 k$\Omega/\square$ and 2.0 Ω mm. The gate lengths of the measured devices are 0.65, 0.85, 1, 2, 4, 8, 20, and 40 μm. In order to reduce the error in extracting series resistance and mobility, we concentrate on the long-channel devices with gate lengths of 8, 20, and 40 μm to obtain surface mobilities.

Figure 2 shows the dc $I-V$ curve of a MOSFET with a gate length L_g of 1 μm and a gate width W_g of 100 μm. The gate voltage is varied from -4.0 to $+3.0$ V with 1.0 V step. The fabricated device has a pinch-off voltage of -4.0 V. The maximum drain current density I_{dss}, measured at positive bias $V_{gs}=+3.0$ V, is ~330 mA/mm. The knee voltage is ~1.0 V at $V_{gs}=0$ V, due to the relatively high series resistance arising from this non-self-aligned process. Under those conditions, the gate leakage current is less than 100 pA, corresponding to $<10^{-4}$ A/cm^2. The gate leakage current for MOSFETs is more than three orders of magnitude lower than for MESFETs under similar bias. No noticeable $I-V$ hysteresis is observed in the drain current in both forward and reverse gate-voltage sweep directions. This indicates that no significant mobile bulk oxide charge is present and that density of slow interface traps is low.

Figure 3 illustrates the drain current as a function of gate bias in the saturation region. The slope of the drain current shows that the peak extrinsic transconductance (g_m) of the 1 μm gate length device is typically ~105 mS/mm. The theoretical intrinsic g_m in saturation regime can be estimated to be ~235 mS/mm by $g_m=v_{sat}\cdot C_{ox}$, where v_{sat} is $\sim 5\times10^6$ cm/s.[15] Counting on the series resistance of the device $R_s\sim3.5$ Ω mm, the theoretical extrinsic g_m is ~129 mS/mm, which is ~20% off from the measured peak g_m value. We ascribe this reduction of g_m to the existing interface traps and the reduction of mobility and saturation velocity at the interface. The flatband condition in the depletion-mode MOSFET is roughly at the gate bias, where the transconductance g_m appears maximum. The more the gate is biased below the flatband condition, the smaller the g_m is, because the distance from the gate to the channel increases by increasing the depletion width in the semiconductor. On the other hand, when the gate bias is above the flatband condition, additional carriers are confined to the interface and the gate-to-channel distance is fixed to the oxide thickness in this accumulation region. Beyond that gate voltage, the surface mobility is known to decrease with the transverse field (or gate bias), leading to g_m reduction. The flatband condition can be approximately determined to be ~0.3 V from Fig. 3. It is consistent with the theoretical value, which is the difference between the metal work function of Ti (3.95 eV) and the semiconductor work function of $In_{0.2}Ga_{0.8}As$ (4.14 eV). It is also confirmed by the $C-V$ measurement which is usually used to determine the flatband voltage.

A strong accumulation current is observed here from $I_{dss}=19$ mA at $V_{gs}=0.3$ V around the flatband condition to $I_{dss}=33$ mA at $V_{gs}=+3.0$ V, as shown in Fig. 2. This indicates the high quality of $Al_2O_3/In_{0.2}Ga_{0.8}As$ interface, which allows an accumulation current to exist at the interface. The $I-V$ characteristic at $V_{gs}>0$ is significantly improved compared to the previous published data on a GaAs MOSFET without an inserted InGaAs layer.[15] In order to quantitatively characterize this $Al_2O_3/In_{0.2}Ga_{0.8}As$ interface, we study the electron accumulation surface mobility, which is directly related to interface properties. There are at least three different scattering mechanisms that have been proposed to account for the surface mobility: phonon scattering, Coulomb scattering, and surface-roughness scattering. The surface mobility is governed by Coulomb scattering due to charged centers and phonon scattering in the low transverse field region. It is dominated by surface roughness and phonon scattering under strong accumulation. By measuring I_{ds} versus V_{gs} at $V_{ds}=0.1$ V (mobility region) of 8-, 20-, and 40-μm-long channel devices, we are able to extract the series resistance of the devices with a relative error of less than 5%. Therefore, an

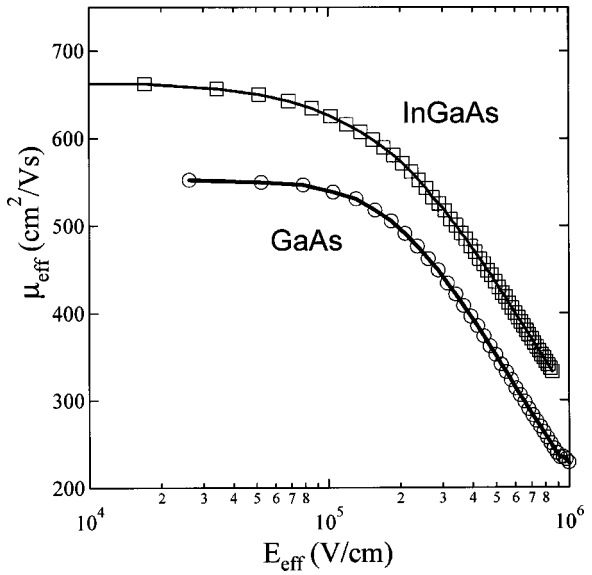

FIG. 4. Effective accumulation electron surface mobility μ_{eff} vs effective electric field E_{eff} on InGaAs (empty squares) and GaAs (empty circles). The data are obtained from 40-μm-gate-length devices.

intrinsic normalized channel resistance R_{ch} at the accumulation region as a function of effective accumulation mobility μ_{eff}, C_{ox}, and V_{gs} can be defined as

$$R_{\text{ch}}=\frac{V_{\text{ds}}}{I_{\text{acc}}}\cdot\frac{W_g}{L_g}=\frac{1}{\mu_{\text{eff}}\cdot C_{\text{ox}}\cdot(V_{\text{gs}}-V_{\text{Gi}})}, \tag{1}$$

where the channel capacitance is the normalized oxide capacitance C_{ox}, V_{Gi} is the voltage at the point of inflection of the I_{ds} versus V_{gs} curve (near the flatband voltage), and I_{acc} is the accumulation current that is taken as zero at $V_{\text{gs}}=V_{\text{Gi}}$.[18,19] Notice that at $V_{\text{gs}}=V_{\text{Gi}}$, the buried-channel conductance is at maximum and remains constant at $V_{\text{gs}}>V_{\text{Gi}}$. Figure 4 is the plot of μ_{eff} versus effective electric field E_{eff} on InGaAs using the formalism expressed in Eq. (1). Unlike the situation for inversion, there is no depletion charge, and E_{eff} on InGaAs is simply

$$E_{\text{eff}}=\frac{\varepsilon_{\text{ox}}\cdot(V_{\text{gs}}-V_{\text{Gi}})}{2\varepsilon_{\text{InGaAs}}\cdot d_{\text{ox}}}, \tag{2}$$

where ε_{ox} (the dielectric constant of Al_2O_3) is 8.6, $\varepsilon_{\text{InGaAs}}$ (the dielectric constant of $In_{0.2}Ga_{0.8}As$) is 13.4, and d_{ox} is the oxide thickness. The accumulation mobility of 660 cm^2/V s at low transverse field is much higher than the reported channel mobility of 470 cm^2/V s at InP-based $Ga_2O_3(Gd_2O_3)/In_{0.53}Ga_{0.47}As$ interface.[12] The value of our surface mobility in the high transverse field region is 20% higher than that of the universal surface mobility of Si MOSFETs at the nearly perfect SiO_2/Si interface.[18,20] The surface mobility on GaAs surface is also plotted in Fig. 4 by performing similar measurements on Al_2O_3/GaAs MOSFETs.[15,16] The higher surface mobility on the InGaAs surface further demonstrates a better interface quality of Al_2O_3/InGaAs and improved device performance for the InGaAs MOSFET compared to the GaAs MOSFET.

We have demonstrated improved GaAs MOSFET with an inserted $In_{0.2}Ga_{0.8}As$ layer as part of the channel using ALD-grown Al_2O_3 as a gate dielectric. A 1-μm-gate-length $In_{0.2}Ga_{0.8}As$/GaAs MOSFET with an Al_2O_3 gate oxide thickness of 160 Å shows a gate leakage current density less than 10^{-4} A/cm^2 and a maximum transconductance above 100 mS/mm. The strong accumulation current at $V_{\text{gs}}>0$ enables us to deduce the electron accumulation surface mobility on $In_{0.2}Ga_{0.8}As$, resulting in as high as 660 cm^2/V s at the $Al_2O_3/In_{0.2}Ga_{0.8}As$ interface. Our findings of high surface mobility of $Al_2O_3/In_{0.2}Ga_{0.8}As$ interface suggest a good Al_2O_3/InGaAs interface and new opportunities in commercializing enhancement-mode (inversion channel) and complementary GaAs MOSFETs.

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