Interface studies of GaAs metal-oxide-semiconductor structures using atomic-layer-deposited HfO_2/Al_2O_3 nanolaminate gate dielectric

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(Received 1 August 2007; accepted 21 September 2007; published online 5 October 2007)

A systematic capacitance-voltage study has been performed on GaAs metal-oxide-semiconductor (MOS) structures with atomic-layer-deposited HfO_2/Al_2O_3 nanolaminates as gate dielectrics. A HfO_2/Al_2O_3 nanolaminate gate dielectric improves the GaAs MOS characteristics such as dielectric constant, breakdown voltage, and frequency dispersion. A possible origin for the widely observed larger frequency dispersion on *n*-type GaAs than *p*-type GaAs is discussed. Further experiments show that the observed hysteresis is mainly from the mobile changes and traps induced by HfO_2 in bulk oxide instead of those at oxide/GaAs interface. © *2007 American Institute of Physics*.
[DOI: 10.1063/1.2798499]

The main obstacle to implement III-V compound semiconductors as novel channel materials for ultimate complementary metal-oxide-semiconductor (CMOS) applications is the lack of high-quality, thermodynamically stable insulators. Although *in situ* molecular beam expitaxy (MBE) $Ga_2O_3(Gd_2O_3)$ and *ex situ* atomic-layer-deposited (ALD) Al_2O_3 show promising results,[1–6] a direct ALD HfO_2, the high-*k* dielectric for Si CMOS at 45 nm node and beyond remains a challenge. Recently, Si (Refs. 7 and 8) or AlN (Ref. 9) surface passivation before HfO_2 deposition has been reported. Though improved *C-V* characteristics have been observed, these methods also have potential limitations. The Si interfacial layer could alter the doping concentration of the GaAs channel after subsequent high-temperature ($T > 750\ ^\circ C$) processing required for dopant activation and degrade the channel mobility. The intrinsic thickness of an AlN layer can increase the effective oxide thickness. In this letter, we present a systematic interface study on ALD HfO_2/Al_2O_3 nanolaminate gate dielectric on *n*- and *p*-type GaAs MOS devices, which combines the advantages of both Al_2O_3 and HfO_2. More importantly, three major issues on compound semiconductor MOS *C-V* characterization, i.e., the "N-dispersion" phenomenon, inversion *C-V*, and the origin of hysteresis, are also insightfully discussed.

MOS capacitors were fabricated on both *n*- and *p*-type GaAs 2-in. substrates with doping concentrations of $(4-6) \times 10^{17}/cm^3$. After NH_4OH based surface pretreatment,[10] 8 nm ALD Al_2O_3/HfO_2 nanolaminate was deposited at 300 °C using an ASM F-120 ALD module. The nanolaminate contains alternate Al_2O_3 (1 cycle) and HfO_2 (2 cycles) with Al_2O_3 as the beginning layer. The Al_2O_3 was deposited using trimethyl aluminum and water, and HfO_2 was deposited using $HfCl_4$ and water. For control samples, 8 nm ALD pure HfO_2 or pure Al_2O_3 was also deposited at the same condition on GaAs substrates. Postdeposition annealing (PDA) was then conducted at 500 °C by rapid thermal annealing in N_2 ambient for 15 s, followed by electron beam evaporated Ni/Au metal as the gate electrodes. The leakage current was measured using an HP4156A semiconductor parameter analyzer, and the capacitance was measured using an HP4284A precision *LCR* meter with frequencies varying from 1 KHz to 1 MHz. Similar experiments with $(NH_4)_2S$ passivation were also performed. Negligible difference was found on *C-V* results, compared to those from NH_4OH passivation.[10] The NH_4OH passivation has certain advantages, viz., well understood chemical handling and a lack of potential sulfur contamination for CMOS manufacture lines. The *C-V* results presented in this letter are all obtained from NH_4OH pretreatment.

Figure 1(a) shows the gate leakage current density of *p*-GaAs MOS capacitors with HfO_2/Al_2O_3 nanolaminate, HfO_2 and Al_2O_3 gate dielectrics both after 500 °C PDA. The HfO_2/Al_2O_3 laminate dielectric films exhibit lower leakage current and higher breakdown voltage than pure HfO_2 films. The gate leakage current density at 3 V gate bias is about 6×10^{-8} A/cm^2 for nanolaminate MOS and 3×10^{-7} A/cm^2 for pure HfO_2 samples. Meanwhile, the breakdown voltage is 6.1 V for nanolaminate samples, 3.8 V for pure HfO_2 samples, and 7.0 V for pure Al_2O_3 samples. This corresponds to maximum electric strength of 7.9 MV/cm for nanolaminates, 5.0 MV/cm for HfO_2, and 9.0 MV/cm for Al_2O_3 after considering the difference between the metal work function and Fermi level of *p*-GaAs. The larger leakage current in HfO_2 devices may be attributed to the creation of more leakage paths around crystallized grains formed from/within the amorphous films after high temperature

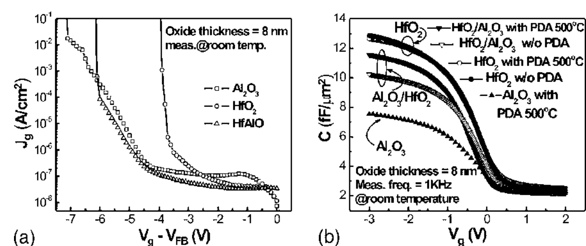

FIG. 1. (a) Leakage current density J_g (A/cm^2) vs gate bias $V_g - V_{FB}$ (V) on HfO_2/Al_2O_3 nanolaminate, pure HfO_2, and pure Al_2O_3 MOS capacitors after postdeposition annealing at 500 °C. (b) *C-V* characteristics of HfO_2/Al_2O_3 nanolaminate, pure HfO_2, and pure Al_2O_3 MOS capacitors before and after PDA process.

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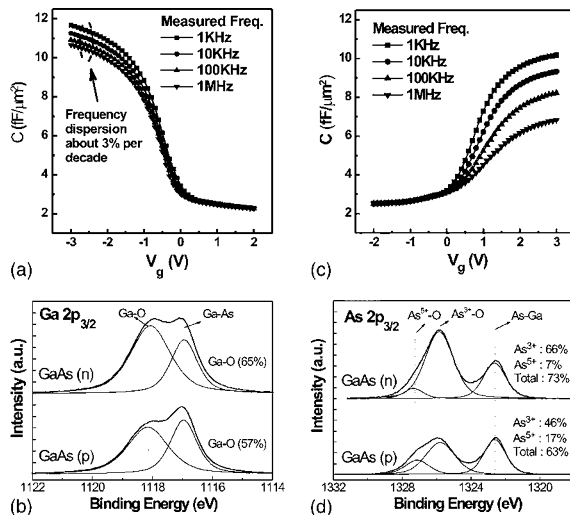

FIG. 2. *C-V* characteristics of HfO_2/Al_2O_3 nanolaminate MOS capacitors measured at different frequencies ranging from 1 KHz to 1 MHz on (a) *p*-type GaAs substrate and (b) *n*-type GaAs substrate. The Ga $2p_{3/2}$ (c) and As $2p_{3/2}$ (d) core level peaks were obtained from *p*-GaAs and *n*-GaAs with native oxides. The contributions of Ga–O, As^{5+}–O, and As^{3+}–O were calculated after curve fitting assuming Gaussian-Lorentzian line shape.

annealing.[11,12] The insertion of intermediate Al_2O_3 layers effectively suppresses further HfO_2 crystallization and reduces the leakage paths in HfO_2. Figure 1(b) shows the *C-V* characteristics of HfO_2/Al_2O_3 and HfO_2 metal-oxide-semiconductor (MOS) capacitor (MOSCAP) before and after PDA, as well as Al_2O_3 MOSCAP after PDA. The nanolaminate *C-V* shows significant enhancement after PDA. It has a sharper transition from the depletion region to the accumulation region than that obtained without annealing, indicating the improved interface quality. Additionally, the accumulation capacitance (C_{max}) value is increased by ~15% after PDA and more than 50% higher than Al_2O_3 with the same thickness. In contrast, HfO_2 MOS samples do not show an obvious difference before and after PDA. Notice that the capacitance value of nanolaminate structure is only about 10% lower than HfO_2, while the breakdown voltage is almost doubled. The dielectric constant of the nanolaminates is ~12.5 deduced from the measured C_{max}, calculated semiconductor capacitance in GaAs, the area of the capacitor, and the film thickness. The midgap interface trap density (D_{it}) is estimated to be around $2\times10^{11}/\text{cm}^2\,\text{eV}$ by the Terman method.

The frequency dispersion on accumulation capacitance is another important issue for high-*k* dielectrics on III-V. This dispersion could be as large as 50% or more on *n*-GaAs in the frequency ranging from 1 kHz to 1 MHz, which implies high interface trap densities at the conduction band edge of GaAs. Figure 2 summarizes the *C-V* characteristic measured on 500 °C annealed nanolaminate samples in the frequency range from 1 KHz up to 1 MHz. The frequency dispersion is about 3% per decade at this frequency range on the *p*-type GaAs substrate. Though the *C-V* curve still shows obvious modulation up to 1 MHz, the frequency dispersion is much more pronounced on the *n*-type GaAs substrate. This N-dispersion phenomenon is widely observed in our experiments with various oxides such as ALD Al_2O_3, HfO_2, ZrO_2, Ga_2O_3, and their combinations. Interestingly, this effect could also be found in literature without any special notice on this phenomenon.[13,14] In many cases, only *C-V* curves on *p*-type GaAs are presented.[10,15,16]

Although GaAs MOS research started as early as in 1965 at the RCA laboratory,[17] there are just a few reports in literature addressing the fundamental surface chemistry and physics on the difficult type of GaAs substrates.[18–21] Pashley *et al.* applied scanning tunnel microscopy to characterize the electronic properties of MBE grown GaAs (001) surfaces with $(2\times4)/c(2\times8)$ reconstructions in high vacuum and found that Fermi level in *p*-GaAs is located near the valence band edge, in contrast to the midgap Fermi-level pinning in *n*-GaAs case due to the high density of acceptorlike kink sites formed at the surface of *n*-GaAs.[20] Other experiments also indicate that *p*-GaAs has reduced surface state density, compared to *n*-GaAs, even after being exposed to air.[21] In order to understand this N-dispersion phenomenon with the current *ex situ* ALD process, we examine the composition of native oxides on *n*-type GaAs and *p*-type GaAs substrates by x-ray photoelectron spectroscopy (XPS), as shown in Figs. 2(c) and 2(d). The native oxide contributions to the Ga $2p_{3/2}$ and As $2p_{3/2}$ peaks, which are marked as Ga–O, As^{5+}–O, and As^{3+}–O, are higher in *n*-GaAs than those in *p*-GaAs. Photochemical reactions on GaAs can explain why *n*-GaAs are oxidized easier than *p*-type GaAs.[21] For illuminated *n*-GaAs, the reaction is $GaAs+6e^+\leftrightarrow Ga^{3+}+As^{3+}$, which leads to photo-oxidation, i.e., Ga and As oxides and elemental As. In illuminated *p*-GaAs, the electron minority carriers result in surface passivation and the reaction is $GaAs+3e^-\leftrightarrow Ga+As^{3-}$ and $As^{3-}+3H^+\leftrightarrow AsH_3\uparrow$, which leads to preferential Ga oxide formation. Preferential Ga–O formation has also been previously reported in the case of O_2 adsorption[22] as well as NH_4OH-treated surfaces.[23] Although unpinning of the Fermi level of GaAs using ALD high-*k* dielectric is mainly due to the appropriate surface pretreatment[3–5,10] and the ALD "self-cleaning" process,[14,24] some may argue that a submonolayer amount of As–O species based on the above surface chemistry might exhibit more on *n*-GaAs than *p*-GaAs during the *ex situ* ALD process. This leads to larger interface density states at the conduction band edge and larger frequency dispersion observed on accumulation capacitance of *n*-GaAs.

According to the Shockley-Read-Hall statistics and the low intrinsic carrier concentration (n_i) of $10^6/\text{cm}^3$ in GaAs, the expected ac frequency to observe inversion *C-V* in dark and at room temperature is very low (~0.002 Hz).[25] Some observed that the "inversion-like" *C-V* curves at a few hundred hertz or up in GaAs could simply be due to the heavy-metal (i.e., Ni, Fe, Zn, etc.) contaminated interface. The inversion feature diminishes after appropriate surface cleaning before dielectric deposition, i.e., HCl and H_2O_2 based cleaning. The condition for reliable quasistatic *C-V* measurements with leakage current density of less than $10^{-8}\ \text{A/cm}^2$ is also hard to fulfill on ultrathin high-*k* dielectrics. Three approaches[26] are recommended to study inversion *C-V* on III-V in general: (i) inversion-type MOS field-effect transistor with implanted source and drain, where minority carriers could be low-injected into the surface channel, (ii) photoillumination to increase the minority carrier concentration, and (iii) elevated temperature to increase the recombination-generation rates of minority carriers in GaAs. Figure 3 shows *C-V* curves on *p*-GaAs and *n*-GaAs taken at temperatures from 300 to 500 K. Depletion capacitances start to increase as temperature goes up to 400 K with full inversion at 500 K. The results demonstrate that Fermi-level unpinning is realized in these ALD nanolaminate GaAs MOS devices.

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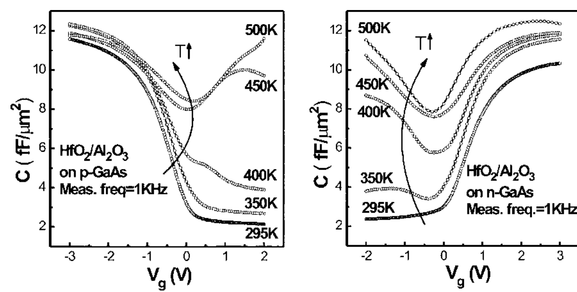

FIG. 3. *C-V* characteristics of HfO_2/Al_2O_3 nanolaminate MOS capacitors measured at different temperatures ranging from room temperature to 500 K on (a) *p*-type GaAs substrate and (b) *n*-type GaAs substrate.

The temperature dependence of accumulation capacitance is explained by the so-called Goswami and Goswami's model.[27] According to this model, the measured series capacitance C_s is given by the relationship of $C_s = C^* + 1/(\omega^2 R^2 C^*)$, where C^* is the intrinsic capacitance. The increase in capacitance with increasing temperature is predicted by this model, providing that the resistance of dielectric R is thermally activated, with $R = R_0 \exp(\Delta E/kT)$. Here, R_0 is a constant and ΔE is the activation energy.

To further explore the influence of the presence of HfO_2 in the gate dielectric stack, experiments with different starting dielectric layers are conducted. The devices were fabricated on the same GaAs substrates with 5 cycles of Al_2O_3 or HfO_2 as the starting layers followed by 8 nm Al_2O_3/HfO_2 as the whole gate dielectric stack. The Al_2O_3-starting and HfO_2-starting nanolaminate MOS devices have the same dielectric thickness, as well as annealing conditions. The *C-V* curves shown in Fig. 4(a) are *surprisingly* similar with negligible dependence on the starting layers. This demonstrates that the significant hysteresis (0.3–0.4 V) observed here are mainly from the mobile charges and traps in bulk oxide induced by HfO_2 instead of those at oxide/GaAs interface. The results are consistent with the general observation that Al_2O_3 films have much smaller hysteresis (~0.1 V) than HfO_2 films (0.5–0.6 V) and are roughly scaled with the film thicknesses. The above conclusion is also confirmed by XPS, as shown in Figs. 4(b) and 4(c). There is no observable difference on Al_2O_3-starting and HfO_2-starting samples, though

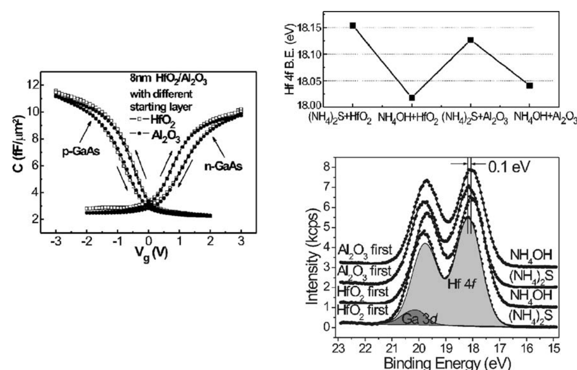

FIG. 4. (a) 1 kHz bidirectional *C-V* characteristics of HfO_2/Al_2O_3 nanolaminate MOS capacitors on both *n*-GaAs and *p*-GaAs with different starting layers. Curves with empty symbols are from HfO_2-starting samples and filled symbols are from Al_2O_3-starting laminate samples. No significant difference can be observed with different starting layers. HfO_2-starting samples have a little bit larger C_{max} as expected. High-resolution XPS analysis of Hf 4*f* peak (b) binding energy and (c) intensity on 3 nm HfO_2/Al_2O_3 with NH_4OH or $(NH_4)_2S$ different surface treatments and 5-cycle HfO_2-starting layer or Al_2O_3-starting layer.

Hf 4*f* and Al 2*p* (not shown) binding energy indicates a consistent (0.1 eV) chemical shift for the NH_4OH treated surface relative to the $(NH_4)_2S$ treated surface. The 2*p* sulfur band is below the detection limit of XPS and may be suppressed due to attenuation of the photoelectron by the overlying layer.

In summary, we have systematically studied interface properties of ALD HfO_2/Al_2O_3 nanolaminate dielectrics on *n*- and *p*-type GaAs-MOS capacitors. A high dielectric constant and electric field strength, as well as inversion *C-V* characteristics at elevated temperatures is achieved by using this nanolaminate gate stack. The observed hysteresis is determined mainly from the mobile charges and traps in the bulk oxide induced by HfO_2 instead of those at oxide/GaAs interface.

The work is supported in part by NSF (Grant No. ECS-0621949) and the SRC MARCO MSD Focus Center.

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