COMPOUND SEMICONDUCTOR

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CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

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GaAs radar adds grunt to Growler

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RF Micro and Sirenza set for merger deal p5

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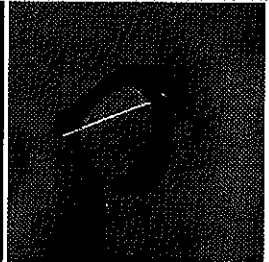

Cubic GaN

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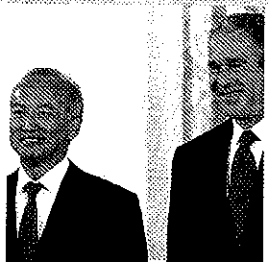
HEADLINE NEWS



Medal winner

Al Cho rewarded for epitaxy work with US National Medal. p5

INTEGRATION

Atomic deposition promises InP logic

A collaboration headed by Peide Ye's team at Purdue University has produced the first InP MOSFETs that feature a high-k dielectric layer grown by atomic layer deposition (ALD).

The Al_2O_3 dielectric MOSFETs, which were produced in partnership with US firm Amberwave Systems, address the weaknesses of their equivalents built with SiO_2, such as low channel-mobility and a high interface trap density.

If these devices can be fully optimized, then the InP MOSFET's channel is calculated to deliver a high-field transconductance 60% greater than that associated with silicon, germanium or GaAs, which would produce a very promising candidate for high-speed logic applications.

The team built its transistors on a pre-treated semi-insulating InP substrate. ALD added a 30 nm layer of Al_2O_3, before source and drain regions were defined by implantation and an electron-beam and lift-off process formed AuGe/Pt/Au gates.

The transistors produced a mobility of 600 $cm^2V^{-1}s^{-1}$. This value is higher than that for InP MOSFETs with a SiO_2 dielectric and standard silicon devices, says Ye, which have typical mobilities of 400 $cm^2V^{-1}s^{-1}$. However, a switch to InP epilayers should bring further substantial improvements in the mobility.

A move away from using the InP substrate for the device should also boost the maximum drain current, which was 70 mA/mm at a gate and drain bias of 8 and 3V, respectively.

The researchers are now developing MBE-grown devices and targeting the 22 nm node, which requires an equivalent oxide thickness of 1 nm. "However, our ultimate goal is to make an ALD high-k InP MOSFET on a silicon substrate," explained Ye. "The work presented in our paper is the first step towards that goal."

Journal reference
YQ Wu *et al.* 2007 *Appl. Phys. Lett.* **91** 022108.

SOLAR CELLS

Layer transfer cuts InP substrate cost

Researchers at Aonex Technologies, the California Institute of Technology and Emcore have developed a technique that promises to cut the cost of four-junction solar cells.

The potential savings would be driven by a switch from a bulk InP substrate to the team's recently fabricated InP-on-silicon composite, which features far less InP material.

"We are now ready to fabricate ultra-high efficiency InGaP/GaAs/InGaAsP/InGaAs four-junction cells on silicon, because we have also developed a technique to make tandems between cells based on InP and GaAs," explained Caltech's Katsuaki Tanabe.

The researchers use a layer-transfer technique that involves bonding InP and silicon, then exfoliating a thin film of InP through ion implantation. Only a few microns of the InP film are consumed in this transfer step, leading to a low materials bill because the donor can be reclaimed and used repeatedly.

The team formed its InP-on-silicon composite by implanting the InP donor with a dose of at least 1×10^{17} cm^{-2} of He^+ ions. Applying a pressure of at least 1 MPa at 150 °C bonded the two materials together, before they were separated to leave a 900 nm thick InP film on the silicon handle. This composite suffered from a high density of lattice defects near the exfoliated surface, so the top part of the InP film was removed to leave 400 nm of higher-quality material.

MOCVD produced single-junction InGaAs solar cells on this composite and a commercial InP substrate. These were compared using illumination from a source mimicking the spectrum that these cells would receive in a multijunction device.

The InP-on-silicon cell produced an energy conversion efficiency of 13.6% at a current density of 24.9 mA/cm^2. This is sufficiently high to current-match to InGaP/GaAs double-junction cells. In comparison, the control device delivered 12.9% efficiency at 21.5 mA/cm^2.

Journal reference
JM Zahler *et al.* 2007 *Appl. Phys. Lett.* **91** 012108.

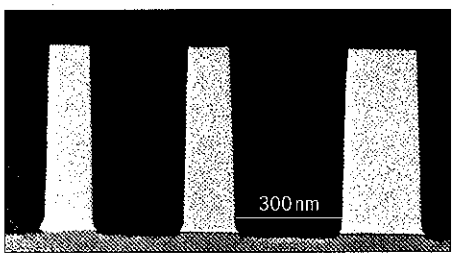
EPITAXY

Narrow trenches unite GaAs with silicon

Engineers from Amberwave Systems and Sarnoff have developed a dislocation trapping technique capable of producing high-quality GaAs-on-silicon epilayers that are compatible with silicon CMOS and GaAs optoelectronic technologies.

"Crucially, this is achieved with only a few hundred nanometers of epitaxial growth, which minimizes the stress arising from the large difference in the thermal expansion coefficients of the materials," explained Jizhong Li from Amberwave.

Li believes that this approach will also work for materials with a larger mismatch, such as InP, and he says that the III-V islands produced by this technique are sufficiently large to accommodate devices such as semiconductor lasers.



Trenches in the SiO_2-on-silicon wafer, with a high trench height-to-width ratio, hold the key to low-defect GaAs epilayers grown by MOCVD.

The researchers produced their GaAs-on-silicon layers using a standard 200 mm silicon CMOS line and commercially available production equipment. Photolithography and reactive ion etching formed trenches in a SiO_2-on-silicon wafer with widths of 0.3–2.5 μm, before a GaAs layer was added using growth temperatures and rates of 430 °C and 7 nm/min for the buffer, and 720 °C and 50 nm/min for the top layer.

The trench height-to-width ratio governs GaAs layer quality. At a ratio of 1.8, cross-sectional and plan-view transmission electron microscopy images reveal that the dislocations formed at the hetero-interface are terminated within 200 nm of GaAs growth.

The team is now characterizing its material with techniques such as etch pit density measurements and starting to investigate the growth of electronic and optolectronic devices on this platform.

Journal reference
JZ Li *et al.* 2007 *Appl. Phys. Lett.* **91** 021114.