ECS Transactions, 19 (2) 605-614 (2009)
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Inversion-mode $In_xGa_{1-x}As$ MOSFETs (x=0.53,0.65,0.75) with atomic-layer-deposited high-k dielectrics

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High-performance *inversion-type* enhancement-mode (E-mode) n-channel MOSFETs on In-rich InGaAs using ALD Al_2O_3 as high-*k* gate dielectrics are demonstrated. The maximum drain current, peak transconductance, and the effective electron velocity of 1.0 A/mm, 0.43 S/mm and $1.0x10^7$ cm/s at drain voltage of 2.0 V are achieved at 0.75-μm gate length devices. The device performance of In-rich InGaAs NMOSFETs with different indium contents, $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$, are systematically studied and compared. Deep submicron inversion-mode $In_{0.75}Ga_{0.25}As$ MOSFETs with ALD high-k Al_2O_3 as gate dielectric are also demonstrated by the full electron beam lithography process. N-channel MOSFETs with 100 nm to 200 nm-long gates have been fabricated. At a supply voltage of 0.8 V, the fabricated devices exhibit drain currents of 260 μA/μm to 801 μA/μm and transconductances of 540 μS/μm to 950 μS/μm. Important scaling metrics, such as on/off current ratio, sub-threshold swing, and drain-induced barrier lowering are presented and their relations to the short-channel effect are discussed. Although on-state performance of InGaAs MOSFETs, such as drain current and trans-conductance, shows great opportunities for III-V MOSFET for future logic applications, great challenges could still exist on off-state performance limited by the implanted junction leakage and donar-type interface traps at high-k/InGaAs interfaces.

Introduction

The continuous device scaling and performance improvements required by the International Technology Roadmap of Semiconductors (ITRS) are facing a grand challenge as conventional Si CMOS scaling comes to its fundamental physical limits. As several new technologies such as high-k metal gate integration, non-planar Si transistors, and strained channel materials have been developed to maintain the Moore's Law, tremendous efforts have been spent to look into those alternative channel materials "beyond Si" such as germanium and III-V compound semiconductors. Benefiting from their high electron mobility and velocity, III-V High Electron Mobility Transistors (HEMTs) or Quantum Well Transistors (QWT) with channels of In-rich InGaAs, InAs and InSb have been demonstrated with superior device metrics such as transconductance, cut-off frequency, and gate delay [1-3]. However, the gate leakage of these transistors limits their application in large scaled integrated circuits.

For more than four decades, the research community has been searching for suitable gate dielectrics or passivation layers on III-V compound semiconductors. There are tremendous efforts and many literatures in this field. The main obstacle is the lack of high-quality, thermodynamically stable insulators on GaAs that can match the device criteria as SiO_2 on Si, e.g., a mid-bandgap interface-trap density (D_{it}) of ~10^{10}/cm^2-eV. Unpinning the III-V surface Fermi level with low D_{it} is the key to the realization of high-performance III-V metal-oxide-semiconductor field-effect-transistors (MOSFETs) with commercial values. In the quest for perfect dielectrics on III-V semiconductors, significant progress has been made recently on inversion-type enhancement-mode InGaAs NMOSFETs, operating under the same mechanism as Si MOSFETs, using high-k gate dielectrics. The promising dielectrics include ALD Al_2O_3 [4-7], HfO_2 [7-9], HfAlO [7,10-11], ZrO_2 [12] and *in-situ* MBE $Ga_2O_3(Gd_2O_3)$ [13-15]. Most recently, record-high inversion current and transconductance have been achieved for surface-channel Al_2O_3/InGaAs MOSFETs [8].

Field-effect transistor (FET) can be divided into two categories: (1) majority carrier device or (2) minority carrier device. Si works perfect as a minority carrier device, i.e., Si MOSFETs, with large inversion current at the perfect SiO_2/Si interface. This minority carrier Si MOSFET is the build-block of our modern microelectronic industry. However, GaAs works only as majority carrier devices such as GaAs HEMTs or InP HEMTs. In the past years, we have succeeded in integrating ALD high-k dielectric Al_2O_3 on GaAs, InGaAs and GaN, and demonstrated high-performance depletion-mode III-V MOSFETs [16-19]. We have also demonstrated GaAs-based enhancement-mode (E-mode) accumulation-type ALD Al_2O_3/InGaAs MOS-HEMTs [20]. Similar works were also reported by Freescale/Glasgow and IBM groups [14,21]. The above two types of devices are majority carrier devices with buried channel design. In this paper, we review the experimental efforts on inversion-mode InGaAs MOSFETs with indium content of 0.53, 0.65, and 0.75. These devices are real minority carrier devices as the traditional Si MOSFETs. We report on the promising on-state performance of these inversion-mode InGaAs MOSFETs with record drain currents. Meanwhile, we also discuss on the existing challenge on the off-state performance of these devices which might be limited by implanted junction leakage in InGaAs and donor-type interface traps.

Experiments

Fig. 1(a) shows the schematic cross section of the device structure. The channel is 15~20 nm thick 1×10^{17}/cm^3 doped p-type $In_{0.53}Ga_{0.47}As$ or $In_{0.65}Ga_{0.35}As$ or $In_{0.75}Ga_{0.25}As$ channel layer, which is MBE epitaxially grown on $In_{0.53}Ga_{0.47}As$/InP substrate. 5~10nm thick ALD Al_2O_3 is used as gate dielectric and Ni or Al is used as gate electrodes. Table 1 show the device fabrication flow. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300^{o}C as an encapsulation layer. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 30 keV and 1×10^{14} cm^{-2} at 80 keV through the 30 nm thick Al_2O_3 layer. Implantation activation was achieved by rapid thermal anneal (RTA) at 700-800 ^{o}C for 10 s in a N_2 ambient. An 5~10 nm Al_2O_3 film was then re-grown by ALD after removing the encapsulation layer by BOE etching and ammonia sulfide surface preparation. After 400-600 ^{o}C Post Deposition Anealing (PDA), the source and drain

ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA at 400 °C for 30 s also in N_2 ambient. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.40 μm to 40 μm and a gate width of 100 μm. Table 1 shows the device fabrication flow. An HP4284 LCR meter was used for the capacitance measurement and a Keithley 4200 was used for MOSFETs output characteristics. Fig. 1(b) shows transmission electron microscopy (TEM) images of the cross section of $Al_2O_3/In_{0.75}Ga_{0.25}As/In_{0.53}Ga_{0.47}As$ on a similarly finished device. No visible interfacial layer between $Al_2O_3/In_{0.75}Ga_{0.25}As$ interface and relaxation of $In_{0.75}Ga_{0.25}As$ on $In_{0.53}Ga_{0.47}As$ are observed from these TEM images. The native oxide of III-V material has been effectively removed by HCl etching, NH_4OH and $(NH_4)_2S$ pretreatment and the ALD "self-cleaning" process. [22-24]

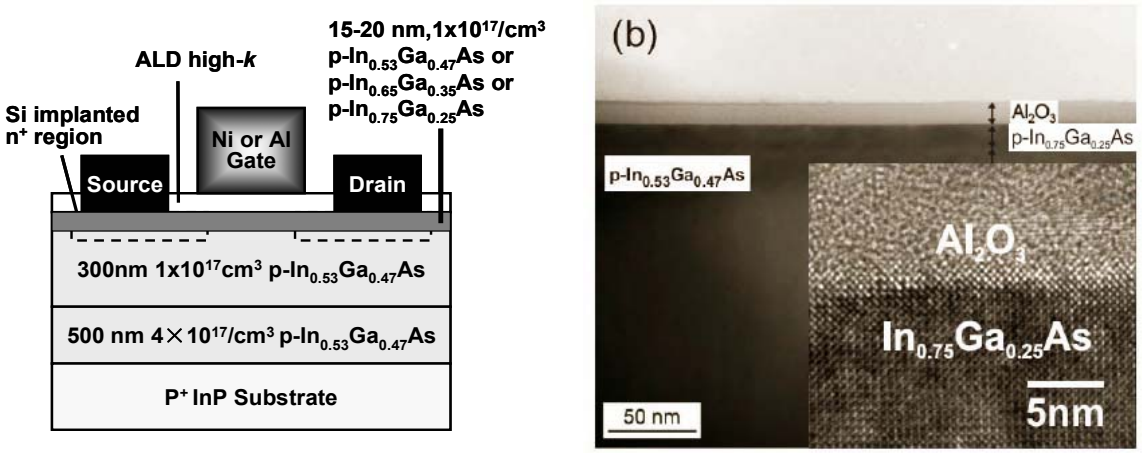

Fig. 1(a) Schematic view of surface channel $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$, and $In_{0.75}Ga_{0.25}As$ NMOSFETs with ALD high-*k* Al_2O_3 as gate dielectrics. (b) TEM image of a similarly fabricated device with 10 nm Al_2O_3. No relaxation of p- $In_{0.75}Ga_{0.25}As$ is observed after 750 °C RTA activation. Inset: high-resolution TEM shows sharp $Al_2O_3/In_{0.75}Ga_{0.25}As$ interface remaining after full device fabrication including 750 °C RTA activation process.

Table 1 Device process flow of surface channel E-mode In-rich InGaAs NMOSFETs

1) NH_4OH surface pretreatment
2) ALD Al_2O_3 30nm as an encapsulation layer
2) S/D patterning and Si implantation (30KeV/1E14 & 80KeV/1E14)
3) S/D activation using RTA (700-800 °C 10s in N_2)
4) ALD re-growth: Al_2O_3
5) PDA: 400-600 °C 30s in N_2
6) S/D contact patterning and Au/Ge/Ni ohmic metal evaporation and 400 °C metallization
7) Gate patterning and Ni/Au or Al/Au evaporation

Results and Discussion

On-state Performance of Al_2O_3/InGaAs MOSFETs With Indium Contents of 0.53, 0.65, And 0.75

Well-behaved I-V characteristic of 0.75-μm gate length inversion-type E-mode $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ NMOSFETs are demonstrated in Fig. 2-4 with the I_{DMAX} of 0.3 A/mm, 0.86 A/mm and 1.0 A/mm, respectively. The gate leakage current (I_G) is less than 10^{-4} A/cm^2 at 4.0 V gate bias (V_G) for all devices. The extrinsic G_m, the intrinsic G_m, and the threshold voltage V_T for $In_{0.75}Ga_{0.25}As$ NMOSFETs are 0.43 S/mm, 052 S/mm, and 0.5 V respectively.

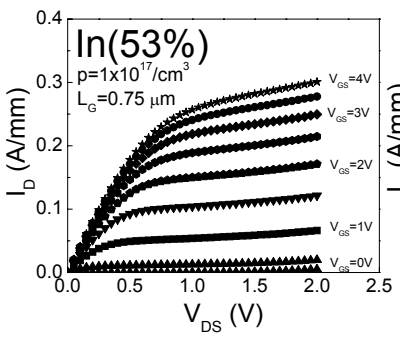

Fig. 2. Drain current (I_D) versus drain bias (V_{DS}) as a function of gate bias (V_{GS}) for Al_2O_3(8nm) / $In_{0.53}Ga_{0.47}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 0.3 A/mm.

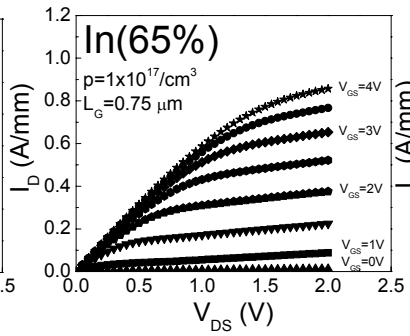

Fig. 3 Drain current versus drain bias as a function of gate bias for Al_2O_3 (10nm) /$In_{0.65}Ga_{0.35}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 0.86 A/mm.

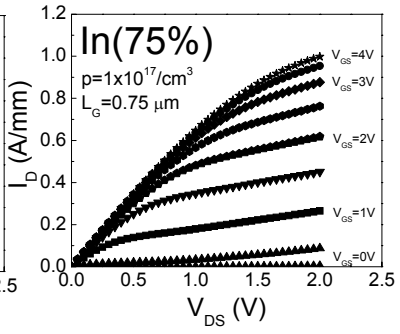

Fig.4 Drain current versus drain bias as a function of gate bias for Al_2O_3(10nm)/$In_{0.75}Ga_{0.25}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 1.0 A/mm.

Fig. 2-4 show I_{DMAX} and G_m versus different indium content InGaAs MOSFETs with 0.75-μm gate length. The I_{DMAX} and G_m increase with increasing indium content in InGaAs due to the increase of mobility and saturation velocity and reduced contact resistance. Fig. 5 is the scaling characteristics of I_{DMAX} and G_m versus different gate length for different indium content devices. $In_{0.75}Ga_{0.25}As$ NMOSFETs show the best device performance due to its narrowest bandgap of 0.52 eV, which is the easiest to realize inversion, and its largest mobility and saturation velocity. The I_D of $In_{0.75}Ga_{0.25}As$ MOSFETs at gate length greater than 10 μm is a little bit smaller than that of $In_{0.65}Ga_{0.35}As$. It could be related to more defects in long gate length devices due to larger lattice mismatch between $In_{0.75}Ga_{0.25}As$ and $In_{0.53}Ga_{0.47}As$. The intrinsic properties of $In_{0.75}Ga_{0.25}As$ are still believed to be superior to those of $In_{0.65}Ga_{0.35}As$. Electron velocity is also studied for all devices with different indium content as in Fig. 6. The effective electron velocity reached $1.0x10^7$ cm/s for $In_{0.65}Ga_{0.35}As$ at 0.4-μm gate length and for $In_{0.75}Ga_{0.25}As$ at 0.75-μm gate length. The effective electron velocity could be significantly above $1.0x10^7$ cm/s (also the value for Si MOSFET) at deep submicron gate length.

Off-state Performance of Al_2O_3/InGaAs MOSFETs And Short Channel Effects

Fig. 7 shows the source current (I_S) versus V_G at different V_{DS}. The I_{on}/I_{off} ratio is 10^6 at V_{DS}=1.0 V, and the subthreshold swing (S.S) is around 190mV/dec. The low I_{on}/I_{off} ratio reported previously [5] is mainly due to the large drain junction leakage current instead of intrinsic limitation from the narrow bandgap InGaAs channel. It could be eliminated by more sophisticated junction engineering.

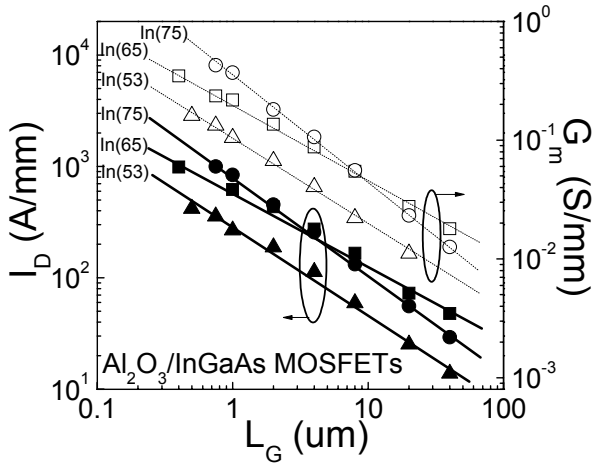

Fig. 5. Comparison of scaling behavior of drain current and transconductance versus gate length with different indium content InGaAs NMOSFETs.

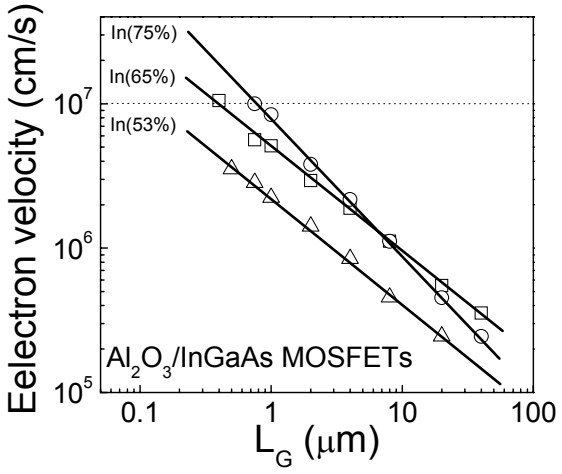

Fig. 6. Effective electron velocity versus gate length with different indium content InGaAs MOSFETs. The effective electron velocity is $1x10^7$cm/s for $In_{0.65}Ga_{0.35}As$ at 0.4-μm gate length and $In_{0.75}Ga_{0.25}As$ at 0.75-μm gate length.

I_D, I_S, I_G and substrate current (I_{SUB}) versus V_{GS} for $In_{0.75}Ga_{0.25}As$ MOSFETs at V_{DS}=2.0 V is studied. It is clear that I_{SUB} determines the leakage floor which constrains I_D at $V_{GS} < 0$. There is no Fermi level pinning at V_{GS} less than 0 V since the gate still controls the channel well as I_S can still be modulated by four orders of magnitude by the gate bias. The analysis on I_S can more accurately reflects the intrinsic properties of devices by avoiding the substrate current. I_{SUB} is mainly from the reverse biased drain-substrate p-n junction. Since III-V semiconductors include elements from relatively volatile V group, activation and/or annealing at high temperature leads to more bulk defects hence produce more junction leakage. In order to reduce junction leakage, development of low temperature activation technique such as spike RTA or laser annealing is critical. The reverse current increases as the activation temperature increases as shown in Fig. 8. The $In_{0.53}Ga_{0.47}As$ MOSFETs show larger reverse current than GaAs MOSFETs due to its narrower bandgap.

Another issue related with off-state performance is so called short-channel effect. This effect becomes so severe that the device cannot be turned off even in linear scale at 100 nm gate length. A full electron beam lithography process was developed for InGaAs MOSFETs. The detailed device fabrication flow is following. After surface cleaning and ammonia passivation, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick Al_2O_3 encapsulation layer was deposited at a substrate temperature of 300 ^oC. All patterns were defined by a Vistec VB-6 UHR electron beam lithography (EBL) system and a lift-off process. The source and drain regions of the MOSFETs were formed by selective implant of 3×10^{13} cm^{-2} at 40 keV Si and annealing at 750°C for 10 s in N_2 for activation. After treated with $(NH_4)_2S$ solution for 10 minutes, another 5 nm Al_2O_3 was also grown by ALD after stripping away the encapsulation oxide layer. The ohmic source and drain contacts were made by electron-beam evaporation of AuGe/Ni/Au and annealing at 400°C for 30 s in N_2. The gate electrode was made by electron-beam evaporation of Ni/Au. The fabricated MOSFETs have a nominal gate length varying from 100, 150, 180 and 200 nm.

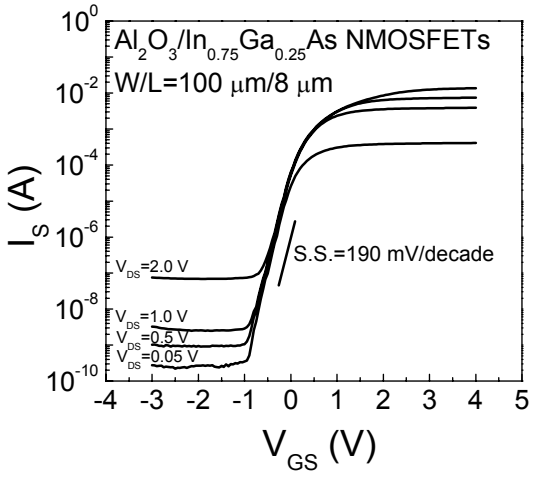

Fig. 7. Source currents versus gate bias as a function of drain voltages for Al_2O_3 /$In_{0.75}Ga_{0.25}As$ NMOSFETs measured at room temperature. The DIBL is 17 mV/V and the subthreshold swing (S.S.) is 190 mV/decade.

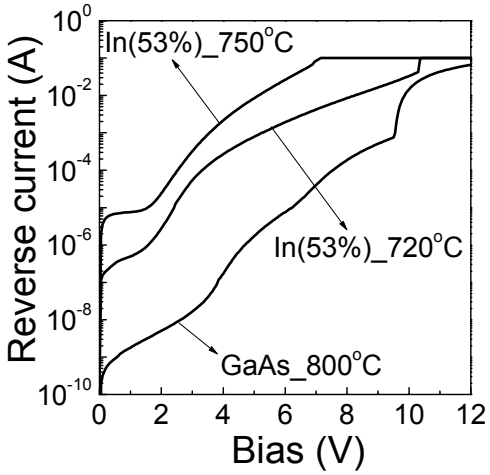

Fig. 8. The reverse biased current of p-n junction with different S/D activation temperature for GaAs and InGaAs MOSFETs. Higher activation temperature leads to more junction leakage.

Fig. 9 shows the well-behaved output characteristics for a 180 nm gate length $In_{0.75}Ga_{0.25}As$ MOSFET under a supply voltage of V_{DD} = 0.8 V. V_T is measured from the transfer characteristics in linear region (Drain-source V_{ds} = 0.05 V). With the gate-source voltage $V_{gs} = V_{ds} = V_{DD}$ = 0.8 V, the measured on-current (I_{on}) is 390 μA/μm, while the gate leakage current is less than 1×10^{-4} A/cm^2 at operating bias. The maximum extrinsic transconductance G_m is 675 μS/μm at V_{gs} = 0.6 V and V_{ds}= 0.8 V. The intrinsic G_m is estimated to be 1 mS/μm, since the measured source/drain resistance is approximately 0.5 Ω·mm. Fig. 10 shows the output characteristics for a 100 nm gate length $In_{0.75}Ga_{0.25}As$ MOSFET under the similar bias condition. The device cannot be turned-off due to the so-called short channel effect. This is mainly due to overly deep implanted source/drain.

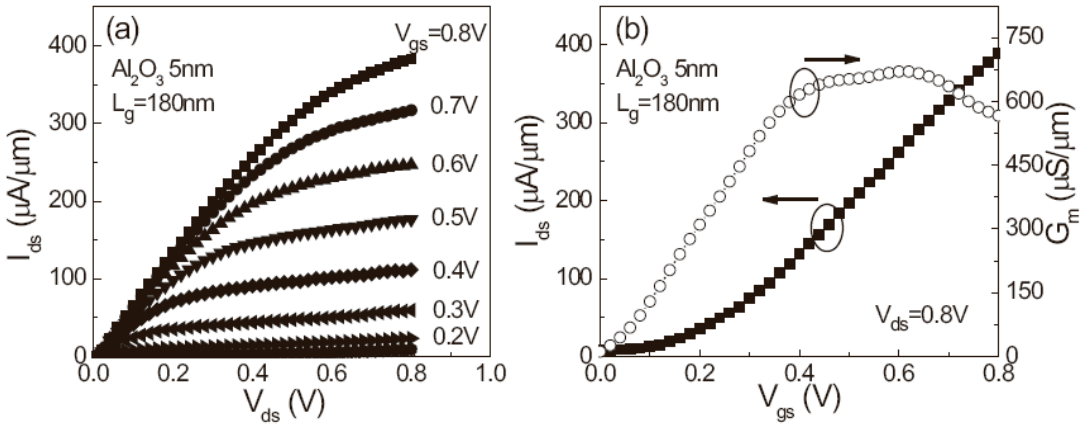

Fig. 9. (a) Drain characteristics of an $In_{0.75}Ga_{0.25}As$ MOSFET with a gate length of 180 nm showing well-behaved on/off currents. (b) Transfer characteristics of an $In_{0.75}Ga_{0.25}As$ MOSFET with a gate length of 180 nm.

Fig. 10 shows the output characteristics for a 100 nm gate length $In_{0.75}Ga_{0.25}As$ MOSFET under the similar bias condition. The device cannot be turned-off due to the so-called short channel effect. This is mainly due to overly deep implanted source/drain. The *p*-type doped channel is punched through by the implanted n^+ source and drain and more sophisticated processing techniques such as halo implantation are needed to fabricate sub-100 nm $In_{0.75}Ga_{0.25}As$ MOSFETs. The 150 nm and 200 nm devices work well because their L_g*'s* are more than twice of the depletion width. With V_{gs} = 0 and 0.8 V, the measured on/off current ratio is 48, 280 and 1530 for L_g = 150, 180, and 200 nm, respectively. Another interest feature is the very low R_{on} for this 100 nm device. It's around 0.6 Ω·mm with the source/drain contact resistance less than 0.3 Ω·mm.

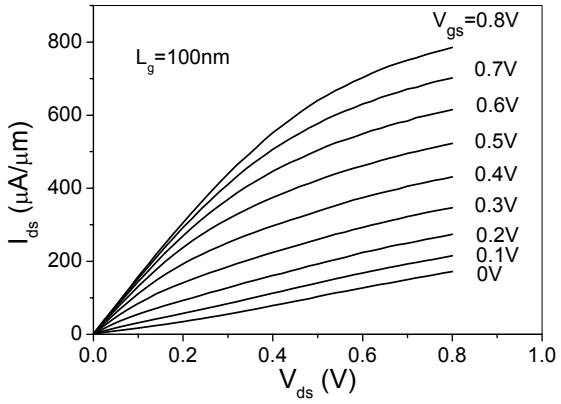

Fig. 10. Drain characteristics of an $In_{0.75}Ga_{0.25}As$ MOSFET with a gate length of 100 nm showing that the device cannot be pinched-off due to the short channel effect.

Fig. 11 shows how I_{on} and peak G_m scale with L_g. Since the 100 nm device cannot be turned off completely, I_{on} in this case is taken to be the difference between the drain current with V_{gs} = 0.8 V and that with V_{gs} = 0. After such adjustment, it can be seen that both I_{on} and G_m scale linearly with L_g down to 100 nm. This adjustment is simply to force the 100 nm data point to align with the scaling line. With L_g = 100 nm, modified I_{on} = 630 μA/μm and G_m = 950 μS/μm. The I_{on} = 801 μA/μm without subtracting off-state current. To our best knowledge, this is the highest G_m ever reported for III-V MOSFETs. The high G_m value can be attributed to ballistic transport and/or velocity overshot in such a short channel device.

To further explore short-channel effects, Fig. 11(b) shows the scaling metrics of subthreshold slope (*SS*) and drain-induced barrier lowering (*DIBL*) as functions of L_g. To quantify the effect of the substrate current on the transfer characteristics in the weak inversion and reverse biased regions [25], *SS* and *DIBL* are evaluated by using either the drain current I_d or the source current I_s. Either way, it can be seen that *SS* and *DIBL* increase with decreasing L_g, indicating more severe short-channel effects. With minimum short-channel effects at L_g = 200 nm, *SS* ~ 100 mV/decade. These scaling metrics could be further improved by non-planar geometry, junction engineering, and better interface quality. Without considering the *SS* degradation by short-channel effects, the upper limit of the interface trap density D_{it} is estimated to be $4\times10^{12}/cm^2$-eV for the present devices. With more demonstrated on-state performance of inversion mode MOSFETs on In-rich InGaAs channels, more work are needed to study the fundamental limitation of narrow

energy gap of In-rich InGaAs, reduction of implanted junction leakage in InGaAs, and the off-state performance related with the exhibiting interface traps. For example, recent works unveil that the interface traps at ALD Al_2O_3/InGaAs interface are mostly donor-type with so far measured lowest D_{it} from 8.0×10^{11}/cm^2-eV to 2.0×10^{12}/cm^2-eV near the conduction band edge and increases continuously to ~10^{13}/ cm^2-eV level at the valence band edge. [26] Further reducing the interface traps to the required device quality level, it is still a big challenge.

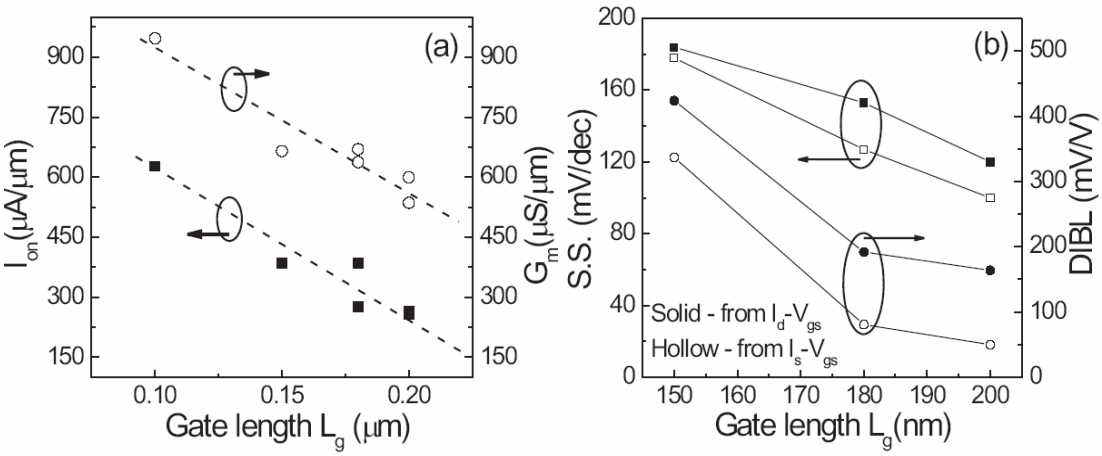

Fig. 11. (a) Maximum drain current I_{on} and peak transconductance G_m showing linear scaling with gate length down to 100 nm. (b) Subthreshold slope *SS* and drain-induced barrier lowering *DIBL* versus gate length L_g., calculated from either the drain current I_d or the source current I_s.

Summary

In summary, we have systematically studied *inversion-type* enhancement-mode (E-mode) n-channel MOSFETs on In-rich $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ using ALD Al_2O_3 as high-*k* gate dielectrics with similar devices. Great on-state performance is demonstrated such as the maximum drain current of 1.0 A/mm at drain voltage of 2.0 V and at 0.75-μm gate length devices and the transconductance of 950 μS/μm at drain voltage of 0.8 V and at 100-nm gate length device. Important scaling metrics, such as on/off current ratio, sub-threshold swing, and drain-induced barrier lowering are presented and their relations to the short-channel effect are discussed. Currently, the overly deep implanted source/drain is the main reason for the short channel effect. However, great challenges could still exist on off-state performance eventually limited by the narrow bandgap of In-rich InGaAs, implanted junction leakage, and existing dominant donor-type interface traps at high-k/InGaAs interfaces.

Acknowledgments

The authors would like to thank T. Shen, K. Xu, D.N. Zakharov, E. Stach, W.K. Wang, O. Kaybashi, J.C.M. Hwang, H. Pal, M.S. Lundstrom, D. Varghese, M.A. Alam, J.A. del Alamo, and D.A. Antoniadis for the valuable discussions and technical assistance. The work is supported in part by NSF (Grant No. ECS-0621949) and the SRC FCRP MSD Focus Center.

References

1. S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, "85nm gate length enhancement and depletion mode InSb quantum well transistors for ultra high speed and very low power logic applications," in *IEDM Tech. Dig.,* 783 (2005).
2. D. H. Kim, J. A. del Alamo, J. H. Lee, and K. S. Seo, "Logic suitability of 50-nm $In_{0.7}Ga_{0.3}As$HEMTs for Beyond-CMOS applications," *IEEE Trans. Electron Devices* **54**, 2606 (2007).
3. D. H. Kim, J. A. del Alamo, "30-nm InAs Pseudomorphic HEMTs on an InP substrate with a current-gain cutoff frequency of 628 GHz," *IEEE Electron Device Lett.* **29**, 830 (2008).
4. P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.-J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, "GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition," *IEEE Electron Device Lett.* **24**, 209 (2003).
5. Y. Xuan, Y. Q. Wu, and P. D. Ye, "High-performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm," *IEEE Electron Devices Lett.* **29**, 294 (2008).
6. J.P. de Souza, E. Kiewra, Y. Sun, A. Callegari, D.K. Sadana, G. Shahidi, D.J. Webb, J. Fompeyrine, R. Germann, C. Rossel, and C. Marchiori, "Inversion mode n-channel GaAs field effect transistor with high-k/metal gate," *Applied Physics Letters* **92**, 153508 (2008).
7. Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, "High performance Submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO as gate dielectrics," in IEDM Tech. Dig., 637 (2007).
8. D. Shahrjerdi, T. Rotter, G. Balakrishnan, D. Huffaker, E. Tutuc, and S. K. Banerjee, "Fabrication of self-aligned enhancement-mode $In_{0.53}Ga_{0.47}As$ MOSFETs with TaN/HfO_2/AlN gate stack," *IEEE Electron Devices Lett.* **29**, 557 (2008).
9. I. Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, D. Garcia, P. Majhi, N. Goel, W. Tsai, C. K. Gaspe, M. B. Santos, and J. C. Lee, "Self-aligned n-channel metal-oxide-semiconductor field effect transistor on high-indium-content $In_{0.53}Ga_{0.47}As$ and InP using physical vapor deposition HfO_2 and silicon interface passivation layer," *Applied Physics Letters* **92**, 202903 (2008).
10. H.C. Chin, M. Zhu, X.H. Tung, G.S. Samudra, and Y.C. Yeo, "In situ surface passivation and CMOS-compatible palladium-germanium contacts for surface-channel gallium arsenide MOSFETs," *IEEE Electron Device Lett.* **29**, 553 (2008).
11. J. Q. Lin, S. J. Lee, H. J. Oh, G. Q. Lo, D. L. Kwong, and D. Z. Chi, "Inversion-mode self-aligned $In_{0.53}Ga_{0.47}As$ n-channel metal-oxide-semiconductor field-effect transistor with HfAlO gate dielectric and TaN metal gate," *IEEE Electron Device Lett.* **29**, 977 (2008).
12. S. Koveshnikov, N. Goel, P. Majhi, H. Wen, M. B. Santos, S. Oktyabrsky, V. Tokranov, R. Kambhampati, R. Moore, F. Zhu, J. Lee, and W. Tsai, "$In_{0.53}Ga_{0.47}As$ based metal oxide semiconductor capacitors with atomic layer deposition ZrO_2 gate oxide demonstrating low gate leakage current and equivalent oxide thickness less than 1 nm," *Appl. Phys. Lett.* **92**, 222904 (2008).

13. F. Ren, J. M. Kuo, M. Hong, W. S. Hobson, J. R. Lothian, J. Lin, H. S. Tsai, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, "$Ga_2O_3(Gd_2O_3)$/InGaAs enhancement-mode n-channel MOSFET's," *IEEE Electron Devices Lett.* **19**, 309 (1998).
14. R. J. W. Hill, D. A. J. Moran, X. Li, H. Zhou, D. Macintyre, S. Thoms, A. Asenov, P. Zurcher, K. Rajagopalan, J. Abrokwah, R. Droopad, M. Passlack, and I. G. Thayne, "Enhancement-mode GaAs MOSFETs with an $In_{0.3}Ga_{0.7}As$ channel, a mobility of over 5000 cm^2/Vs, and transconductance of over 475 μS/μm," *IEEE Electron Devices Lett.* **28**, 1080 (2007).
15. T. D. Lin, H. C. Chiu, P. Chang, L. T. Tung, C. P. Chen, M. Hong, J. Kwo, W. Tsai, and Y. C. Wang, "High-performance self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistor with $Al_2O_3/Ga_2O_3(Gd_2O_3)$ as gate dielectrics," *Applied Physics Letters* **93**, 033516 (2008).
16. P.D. Ye, G.D. Wilk, J. Kwo, B. Yang, H.-J.L. Gossmann, M. Frei, S.N.G. Chu, J.P. Mannaerts, M. Sergent, M. Hong, K. Ng, J. Bude, *IEEE Electron Devices Lett.* **24**, 209 (2003).
17. P.D. Ye, G.D. Wilk, B. Yang, J. Kwo, H.-J.L. Gossmann, S.N.G. Chu, S. Nakahara, H.-J.L. Gossmann, J.P. Mannaerts, M. Sergent, M. Hong, K. Ng, J. Bude, *Appl. Phys. Lett.* **83**, 180 (2003).
18. P.D. Ye, G.D. Wilk, B. Yang, J. Kwo, H.-J.L. Gossmann, M. Hong, K. Ng, J. Bude, *Appl. Phys. Lett.* **84**, 434 (2004).
19. P.D. Ye, B. Yang, K. Ng, J. Bude, G.D. Wilk, S. Halder, J.C.M. Hwang, *Appl. Phys. Lett.* **86**, 063501 (2005).
20. H.C. Lin, T. Yang, H. Sharifi, S.K. Kim, Y. Xuan, T. Shen, S. Mohammadi, and P.D. Ye, *Appl. Phys. Lett.* **91**, 212101 (2007).
21. Y. Sun, E.W. Kiewra, J.P. de Souza, J.J. Bucchignano, K.E. Fogel, D.K. Sadana, and G.G. Shahidi, *IEEE Electron Device Letters* **29**, 5 (2009).
22. M.M. Frank, G.D. Wilk, D. Staodub, T. Gustafsson, E. Garfunkel, Y.J. Chabal, J. Grazul, and D.A. Muller, "HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition," *Appl. Phys. Lett.* **83**, 152904 (2003).
23. M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, "Surface passivation of III-V compound semiconductors using atomic-layer-deposition-grown Al_2O_3," *Applied Physics Letters* **87**, 252104 (2005).
24. C.L. Hinkle, A.M. Sonnet, E.M. Vogel, S. McDonnell, G.J. Hughes, M. Milojevic, B. Lee, F.S. Aguirre-Tostado, K.J. Choi, H.C. Kim, J. Kim, and R.M. Wallace, "GaAs interfacial self-cleaning by atomic layer deposition," *Applied Physics Letters* **92**, 071901 (2008).
25. P. D. Ye, Y. Xuan, Y. Q. Wu, T. Shen, H. Pal, D. Varghese, M. A. Alam, M. S. Lundstrom, W. K. Wang, J. C. M. Hwang, and D. A. Antoniadis, "Subthreshold characteristics of high-performance inversion-type enhancement-mode InGaAs NMOSFETs with ALD Al_2O_3 as gate dielectric," in *Proc. 66th Device Research Conf.*, 93 (2008).
26. D. Varghese, Y. Xuan, Y.Q. Wu, T. Shen, P.D. Ye, and M.A. Alam, "Multi-probe interface characterization of $In_{0.65}Ga_{0.35}As/Al_2O_3$ MOSFET", *in IEDM Tech. Dig.*, 379 (2008); H.C. Lin, Ph.D. Dissertation, Purdue University (2008) with partial work done at IMEC; K. Martens et al., private communication.