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Atomic-Layer-Deposited High-k Dielectric Integration on Epitaxial Graphene

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The scaling of silicon-based MOSFET technology beyond the 22 nm node is challenging. Further progress requires new channel materials such as Ge, III-V semiconductors, carbon nanotubes (CNTs) and graphene. Perfect top-gate dielectric stacks are needed in order to sustain their potential device performance for carbon nanoelectronics. Due to the inert nature of carbon surfaces of CNTs and graphene, the challenges and current work on atomic-layer-deposited (ALD) high-k/CNTs and graphene integration are reviewed. The research work performed at Purdue University on ALD high-k integration on epitaxial graphene on SiC is summarized.

Introduction

The continuous device scaling and performance improvements required by the International Technology Roadmap of Semiconductors (ITRS) are facing a grand challenge as conventional Si CMOS scaling comes to its fundamental physical limits. As several new technologies such as high-k metal gate integration, non-planar Si transistors, and strained channel materials have been developed to maintain Moore's Law, tremendous efforts have been spent to look into those alternative channel materials "beyond Si" such as germanium, III-V, nanowires, carbon nanotubes (CNTs), and graphene as the emerging channel materials. All of these channel materials need device-quality top-gate dielectric stacks in order to sustain their excellent transport properties and provide the potential device performance to benchmark with Si CMOS.

It is interesting to note that the gate stack formation usually combines with a channel surface preparation and a conventional atomic-layer-deposited (ALD) high-k process. For Ge, the channel surface preparation layer is either thermal GeO_2 or amorphous Si layer before the conventional ALD of Al_2O_3, HfO_2 or $LaLuO_3$. The issues related with ALD of gate dielectrics on carbon nanoelectronic materials are quite different from the traditional semiconductors. For Ge and III-V, high-quality gate dielectrics require the efficient passivation of the dangling bonds of the semiconductor interface. In great contrast, CNTs and graphene have a chemically inert surface and cannot initiate the chemical reactions the ALD process requires. The inert carbon surface issue is not a dominant concern for CNTs laid on SiO_2 surface. Due to the super small dimension of CNTs (1~2nm), the ALD process can start from the clean SiO_2 surface and eventually overgrow on top of CNTs; but, it is an issue for suspended CNT and graphene.

There are three main preparation strategies for graphene, resulting in different materials sharing some common physical and electrical properties – mechanically exfoliated graphene from graphite (1-3), CVD of graphene on Ni or Cu (4-7), and high-temperature thermal decomposited graphene on SiC (8-12). The advantage of epitaxial

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graphene on SiC for nanoelectronic applications resides in its planar 2D structure that enables conventional top-down lithography and processing techniques. Since SiC can be obtained as an insulating substrate, this technique does not require transferring the graphene layer onto another substrate, compared to CVD and exfoliation approaches. Except for opening the bandgap by forming graphene nano-ribbons, an additional challenge for graphene based electronics is the formation of high-quality, ultrathin dielectrics with low interface trap density. A perfect graphene surface is chemically inert (13-15), which does not lend itself to conventional ALD high-k dielectrics, which is very different from CNTs. In this paper, we review the majority research work in the past couple of years on ALD/graphene integration and focus on the research work done at Purdue University on ALD/epitaxial graphene integration. The approach we have taken is to insert a fully oxidized nanometer thin aluminum film as a seeding layer followed by an ALD process (16). The electrical properties of epitaxial graphene films are sustained after gate stack formation without significant degradation. At low temperatures, half-integer quantum-Hall effect is observed in epitaxial graphene on SiC (0001), along with pronounced Shubnikov-de Haas oscillations (17).

Review on ALD high-k on CNTs and graphene

Since their discovery in 1991 (18), CNTs have been the focus of extensive research for many potential applications, including sensing, chemistry, biology, and electronics (19-21). CNTs are rolled up sheets of graphite with diameter of 1~3 nm and are available in both single-walled and multi-walled forms. Due to their perfect one-dimensional crystalline structure, CNTs exhibit unusual physical, chemical, mechanical and electrical properties. Single-walled carbon nanotube field effect transistors (SWNT-FETs) were first demonstrated in 1998 (22). It has been demonstrated that these transistors can achieve ballistic transport, can sustain high current densities while dissipating very low DC powers (23-24). Despite the advantages of SWNT-FETs, these devices have not been utilized in industry due to two major hurdles in realization of large area and/or complex circuits based on these transistors. These two issues are: [1] Difficulty in the separation of semiconducting from metallic single-walled carbon nanotubes; [2] Difficulty in alignment and placement of the nanotubes to the device structure in a controlled and reproducible fashion. Up to now, various methods for selective deposition or growth of single walled carbon nanotubes (SWNTs) on two electrodes have been developed (25-26). In the past years, we deposited ALD Al_2O_3 and HfO_2 dielectrics on CNTs with two different aligning techniques and fabricated and characterized high-performance SWNT-FETs. The work is mainly carried out by Sunkook Kim and Saeed Mohammadi at Purdue University and published in Ref. (27-28). In the first method, room temperature device fabrication is achieved based on dielectrophoresis. Individual SWNTs and SWNT bundles suspended in ethanol solution display a positive dielectrophoresis which facilitate their alignment and placement through a very simple processing technology. It was found that the electrical performance of these devices is limited by their high contact resistance of SWNT bundles which is on the order of a few MΩ. In the second technique, alignment of nanotubes to the device's structure is achieved through high temperature CVD synthesis of nanotubes on a quartz wafer (29). Parallel arrays of individual SWNTs with a controlled density are utilized to construct high performance SWNT-FETs. This technology allows implementation of SWNT-FETs with low contact resistance, high mobility, and high saturation current.

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Graphene, a monolayer of carbon atoms tightly packed into a two-dimensional (2D) hexagonal lattice, has recently been shown to be thermodynamically stable and exhibits astonishing transport properties, such as an electron mobility of ~15,000 cm^2/Vs and an electron velocity of ~10^8 cm/s at room temperature. An existing challenge for graphene based electronics is the formation of high quality, ultrathin dielectrics with low interface trap density. A perfect graphene surface is chemically inert, which does not lend itself to conventional ALD high-k dielectrics. (13) Numerous efforts have been carried out in this field using a certain seeding layer or interfacial layer, as done with Ge or III-V. It can be summarized as [1] TMA + NO_2 seeding layer (14) [2] TMA+O_3 seeding layer (30) [3] fully oxidized Al seeding layer (31,17) [4] organic PTCA seeding layer (15) [5] diluted spin-coated polymer NFC 1400-3CP as a buffered dielectric (32). Much more work is needed to characterize the interface quality and optimize the dielectric formation process at device level. Our approach is to form ALD high-k gate stack integration on epitaxial graphene films by inserting a fully oxidized Al film as a seeding layer. The gate stack formation does not degrade the electrical properties of epitaxial graphene films. The quantum Hall effect (QHE) is observed in gated epitaxial graphene films on SiC (0001), along with pronounced Shubnikov-de Haas (SdH) oscillations in magneto-transport. The observation of quantum features demonstrates the reasonable success of integration of ALD high-k on graphene. (17)

Electronic transport study on ALD top-gated epitaxial graphene

The graphene films were grown on semi-insulating 4H-SiC substrates in an Epigress VP508 SiC hot-wall chemical vapor deposition reactor. The off-cut angle of the substrate is nominally 0°. Prior to growth, substrates were subjected to a hydrogen etch at 1500 °C for 10 min, followed by cooling the samples to below 700 °C. After evacuating hydrogen from the system, the growth environment was pumped to an approximate pressure of 2×10^{-7} mbar before temperature ramping at a rate of 10–20 °C/min up to the specified growth temperature. The detailed device structure and fabrication could be found in Ref. 17. The device isolation was achieved by O_2 plasma mesa dry etching. One nanometer of an aluminum or titanium metal film was evaporated onto the sample by electron-beam evaporation at about 10^{-6} Torr and fully oxidized in an oxygen rich ambient for one hour as a seeding layer for ALD growth. Thirty nanometers of Al_2O_3 gate dielectric were deposited at 300 °C using an ASM F-120 reactor with trimethyl aluminum and water vapor as the precursors. The metal contacts and gate electrodes were subsequently patterned and deposited, both using electron-beam evaporated Ti/Au. Four-point magnetotransport measurements were performed in a 1T Abbess Hall system (110–300 K), a variable temperature (0.4–70 K) ^{3}He cryostat, or a variable temperature (1.4-300K) ^{4}He cryostat using standard low frequency lock-in techniques. The external magnetic field (B) was applied normal to the graphene plane. Devices fabricated from various growth conditions were characterized. A summary of the growth conditions is listed in Table 1.

Fig. 1 shows the carrier mobilities and densities for the epitaxial graphene devices. Graphene grown on the Si-face is compared to graphene grown on the C-face of SiC. Looking at conditions #1128 and #1148, both grown on the C-face of the SiC substrates, carrier densities and mobilities are both enhanced as compared to the devices on the Si-face. The growth conditions, film morphology, and electrical properties of the epitaxial

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TABLE I. SUMMARY OF GRAPHENE GROWTH/FABRICATION CONDITIONS

Designation	SiC substrate face	Growth Temperature (°C)	Growth Time (min)	Growth Ambient	Growth Pressure (milibar)	Dielectric Seeding Layer
#1117	Si	1600	10	argon	10	Al
#1118	Si	1600	10	vacuum	1.0×10^{-5}	Al
#1128	C	1600	10	argon	1.0	Al
#1148	C	1600	10	argon	50	Al
#1156	Si	1600	10	vacuum	1.0×10^{-5}	Al
#1162	Si	1600	30	vacuum	1.0×10^{-5}	Al
#1164	Si	1640	30	vacuum	1.0×10^{-5}	Al
#1174	Si	1600	10	vacuum	1.0×10^{-5}	Ti

graphene films differ markedly between films grown on the C-face and films grown on the Si-face. The formation of graphene on C-face is very rapid at the growth temperature of 1500-1650 ^{o}C in vacuum. At growth temperatures ≥ 1550 ^{o}C, several-micron large regions of smooth graphene films are obtained with tens of nanometers high ridges as domain boundaries.(33) Without gate stacks, the multi-layer graphene films on C-face are mostly p-type with a typical Hall mobility of 5000-6000 cm^2/Vs. On Si-face, continuous few-layer graphene only starts to form at 1550 ^{o}C. The growth on Si-face is much slower, making it possible to form single layer graphene with a better controlled process. (34) The morphology of graphene films on the Si-face is quite homogenous compared to those films on the C-face. However, the typical Hall mobility of graphene on Si-face is ~ 1300-1600 cm^2/Vs. The carriers for Si-face are always n-type from Hall measurements without gate dielectrics. It remains at low temperature as shown in Figure 1.

As the second part of the experiment, the growth time and temperature were adjusted. Comparing devices from conditions #1156 and #1162, an increase in growth time from 10 minutes to 30 minutes has only a small effect, slightly increasing mobility and densities. Comparing devices from condition #1164 to conditions #1156 and #1162, one sees that an increase in temperature by 40°C has a much greater effect, reducing mobilities by about 500 cm^2/Vs but increasing carrier densities by a factor of two. Another interesting fact is that mobility does not change dramatically between 77 K down to 1 K.

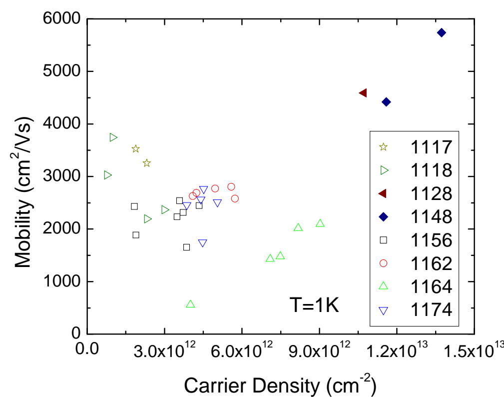

Figure 1. Low temperature Hall mobilities and carrier densities for epitaxial graphene on SiC with high-k Al_2O_3 gate stack. These measurements are taken at a temperature of 1K. Growth conditions are differentiated by symbol type and color. #1128 and #1148 are on C-face with filled symbols. The rest are on Si-face with empty symbols.

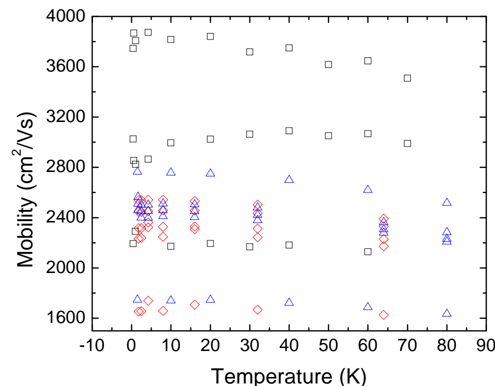

Figure 2. Mobility as a function of temperature for epitaxial graphene on SiC with high-k Al_2O_3 gate stack. Growth/fabrication conditions #1118, #1156, and #1174 are shown by the black squares, red diamonds, and blue triangles respectively.

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In order to study the effect of dielectric/graphene interface on transport properties, Hall bar devices were manufactured using fully oxidized titanium, rather than aluminum, as the seeding layer for the ALD of the Al_2O_3 gate dielectric. Comparing conditions #1156 and #1174, we see that mobility remains unchanged while carrier densities increase only slightly. The difference between Al_2O_3 and TiO_2 has a small effect on the mobility of graphene. However, the gate stack using Ti as the seeding layer produced gates with higher leakage currents, making Al a more favorable seeding layer for the ALD process.

As the fourth part of the experiment, the temperature dependence of the carrier mobility and density is examined. Figure 2 and Figure 3 show that over the temperature range of 1K to 80K, there is little change with temperature in the carrier mobility and carrier density for each device, relative to the differences from device to device. This fact indicates that impurity scattering in the epitaxial graphene film is the dominate mobility limiting mechanism for temperatures below 80 K. However, above 80K, the carrier mobility and density begin to vary more strongly with temperature as phonon scattering begins to dominate and charge carriers are thermally excited, as Fig. 4 shows.

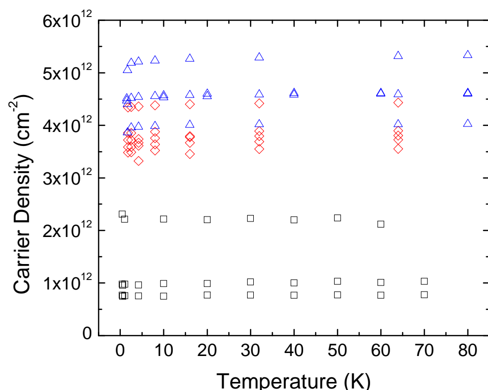

Figure 3. Carrier Density as a function of temperature for epitaxial graphene on SiC with high-k Al_2O_3 gate stack. Growth/fabrication conditions #1118, #1156, and #1174 are shown by the black squares, red diamonds, and blue triangles respectively.

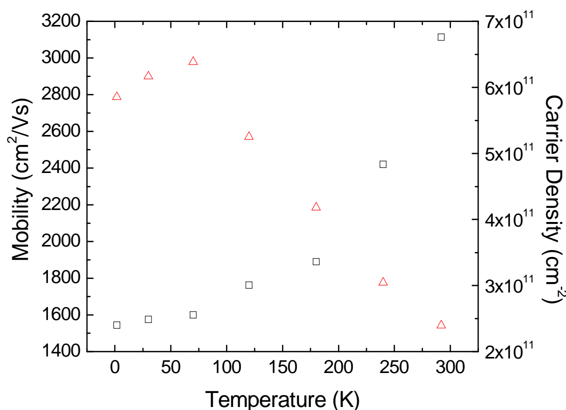

Figure 4. Carrier mobility and density as a function of temperature for a device from growth/fabrication condition #1118 over an extended temperature range. Mobility and carrier density are depicted by red triangles and black squares respectively.

As the final part of the experiment, the top gates are used to examine the mobility as a function of carrier density at a temperature of 1K. These measurements are shown in Fig. 5. The mobility increases with increasing carrier density for devices manufactured from conditions #1162 and #1164, indicating that impurities are the dominant scattering mechanism at low temperature, as is expected. The increase of density has much more screening effects on impurities so that the mobility of carriers increases. However, the two devices from conditions #1156 do not follow this expected trend. This is perhaps related to scattering due to the roughness of the gate stack. The mobility strongly depends on the scattering mechanism and the quality of dielectric/graphene interface and even graphene/SiC interface.

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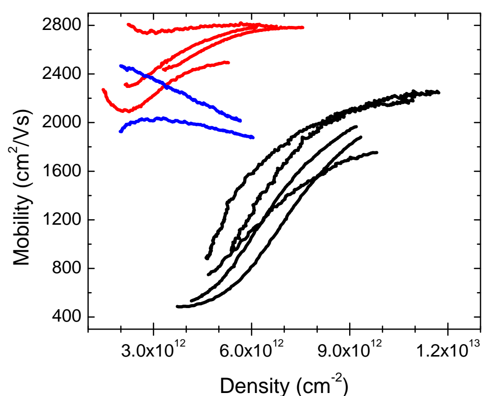

Figure 5. Mobility as a function of carrier density at a temperature of 1K. The carrier density is modulated using the top gate of the graphene Hall bar devices. Growth conditions #1156, #1162, and #1164 are depicted in blue, red and black respectively.

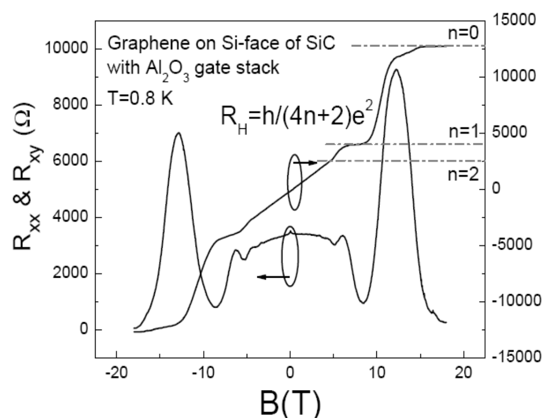

Figure 6. Hall resistance and magneto-resistance measured in the device in Figure 10(a) at T=0.8K and with floating gate bias. The horizontal dashed lines corresponding to $h/(4n+2)e^2$ values. The QHE of the electron gas in epitaxial graphene is shown one quantized plateau and two developing plateau in R_{xy}, with vanishing R_{xx} in the corresponding magnetic field regime.

In a brief summary of mobility study, electronic transport of epitaxial graphene on SiC at low temperature has been extensively studied to gain insight into the optimum growth and processing conditions. Devices manufactured on the C-face of SiC show higher mobilities and carrier densities than those on the Si-face of SiC. Further increases in growth time seem to have little effect on the graphene electronic transport properties, but increases in growth temperature increase carrier densities without significant degradation in the mobility, which is desirable for device applications. The Ti seeding layer does not aversely affect electronic transport in the graphene devices as compared to the Al seeding layer, but gate stacks deposited using the Ti seeding layer showed higher leakage currents. Most of the data show that impurity scattering is dominant below 80K, and at temperatures above 80K phonon scattering begins to dominate as expected.

Figure 6 shows the magneto-resistance R_{xx} and the Hall resistance R_{xy} as a function of magnetic field B from -18T to 18T at 0.8 K. From the Hall slope, the electron density is determined to be 1.04×10^{12}/cm^2 and Hall mobility of 3580 cm^2/Vs at 0.8 K. At high magnetic fields, R_{xy} exhibits a plateau while R_{xx} is vanishing, which is the fingerprint of the QHE and SdH oscillations. One well-defined plateau with value ($h/2e^2$) is observed at |B|>15.5T, while two higher-order plateaus are developing with values of ($h/6e^2$) and ($h/10e^2$), respectively. The pronounced SdH oscillations with at least four distinguishable peaks are also observed at the corresponding magnetic fields. The precision of the plateau is better than 1 part in 10^4 within the instrumental uncertainty. It shows the QHE in epitaxial graphene is also applicable for metrology applications. The R_{xy} quantization in this epitaxial graphene film is in accordance with [$h/(4n+2)e^2$], where n is the Laudau level index, found in exfoliated graphene as a distinguishing feature of Dirac electrons. It is significantly different from conventional Fermi electrons with plateaus of (h/ne^2). The observed well-defined QHE reproduces the unique features observed in exfoliated single-layer graphene including a Berry phase of π. The observed QHE on this epitaxial graphene confirms that epitaxial graphene on SiC (0001) and exfoliated single-layer graphene are governed by the same relativistic physics with Dirac particles as transport

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carriers. Due to the relatively thick graphene films on the C-face of SiC grown under similar conditions, no QHE is observed on C-face fabricated devices.

Summary

In summary, we review the critical issues related with ALD high-k integration on CNTs and graphene and current status in this field. The detailed electronic transport studies on epitaxial graphene integrated with ALD high-k by inserting a nanometer thin fully oxidized metal film are presented. The first observation of half-integer QHE confirms that epitaxial graphene grown on SiC shares the same physical properties of exfoliated graphene and also verifies the good quality of top-gated dielectric stack on graphene.

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