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ALD High-k as a Common Gate Stack Solution for Nano-electronics

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The scaling of silicon-based MOSFET technology beyond the 22 nm node is challenging. Further progress requires new materials, innovative structures, and even novel device concepts. All the emergent channel materials need perfect top-gate dielectric stacks in order to sustain their potential device performance. ALD high-k as a common gate stack solution finds itself very successfully integrated with these novel channel materials such as Ge, III-V, different nanowires, carbon nanotubes (CNTs), graphene and newly discovered all oxide electronic materials.

Introduction

The continuous device scaling and performance improvements required by the International Technology Roadmap of Semiconductors (ITRS) are facing a grand challenge as conventional Si CMOS scaling comes to its fundamental physical limits. As several new technologies such as high-k metal gate integration, non-planar Si transistors, and strained channel materials have been developed to maintain the Moore's Law, tremendous efforts have been spent to look into those alternative channel materials "beyond Si" such as germanium, III-V, nanowires, carbon nanotubes (CNTs), and graphene as the emerging channel materials. All these channel materials need device-quality top-gate dielectric stacks in order to sustain their excellent transport properties and provide the potential device performance to benchmark with Si CMOS.

One of the major reasons for the success of Si is that the SiO_2/Si interface is of high quality with a mid-bandgap interface-trap density (D_{it}) of ~10^{10}/cm^2-eV for thermal grown SiO_2 on H-terminated Si face. The situation for any other oxide on any other semiconductors is quite different. For example, the research community has been searching for suitable gate dielectrics or passivation layers on III-V compound semiconductors for more than four decades with very limited success. Atomic-layer deposition (ALD) is based on the self-limiting chemical reactions to form ultra-thin, uniform, conformal, and pin-hole free films. ALD or Atomic-layer epitaxy (ALE) concept was invented in 70s. Strong interest in non-native oxides for Si CMOSFETs began in the late 1990s. High-*k* dielectric research, especially the development of ALD high-*k* dielectrics for Si MOSFETs, has since flourished. (1) In 2007, Intel claimed its successful integration of ALD high-*k* dielectric and metal gate process into its 45 nm node technology as one of the biggest technical leaps in Si CMOS development, after the introduction of poly-silicon gate in the 1960s. (2) The success of ALD high-*k* dielectrics on Si has created much more research on ALD itself and other applications beyond Si CMOS.

It is interesting to note that the gate stack formation usually combines with a channel surface preparation and a conventional ALD high-k process. For Ge, the channel surface preparation layer is either thermal GeO_2 or amorphous Si layer before the conventional ALD of Al_2O_3, HfO_2 or $LaLuO_3$. For III-V compound semiconductors, HF/HCl, NH_4OH and $(NH_4)_2S$ are applied before ALD high-k. The successful integrations performed in our research group include GaAs, InGaAs, InAs, InSb, InP, GaN, and GaSb. In collaborations with other Purdue device groups, we also demonstrated ALD as a common solution for various nanowire systems such as ZnO and In_2O_3 and CNTs. For semiconductor nanowires, the critical issue is the interface trap density between ALD high-k and nanowires, similar to Ge and III-V planar structures. The situation is even challenge because more surface area involved and complication of different facets on one single nanowire. One interesting result is the first experimental demonstration of InGaAs finFET down to 40 nm dimension. InGaAs finFET can be evaluated as a new type of III-V nanowires FET using top-down approaches. The inert carbon surface issue is not a dominant issue for CNTs laid on SiO_2 surface. Due to super small dimension of CNTs (1~2nm), ALD process can start from the clean SiO_2 surface and eventually overgrown on top of CNTs. The advantage of epitaxial graphene for nanoelectronic applications resides in its planar 2D structure that enables conventional top-down lithography and processing techniques. Except for opening the bandgap by forming graphene nano-ribbons, an additional challenge for graphene based electronics is the formation of high-quality, ultrathin dielectrics with low interface trap density. A perfect graphene surface is chemically inert, which does not lend itself to conventional ALD high-k dielectrics, which is very different from CNTs. One successful high-*k* gate stack on epitaxial graphene is realized by inserting a fully oxidized nanometer thin aluminum film as a seeding layer followed by an ALD process. The electrical properties of epitaxial graphene films are sustained after gate stack formation without significant degradation. At low temperatures, quantum-Hall effect is observed in epitaxial graphene on SiC (0001), along with pronounced Shubnikov-de Haas oscillations. This quantum experiment confirms that the reasonable quality of dielectric/graphene interface exhibits. Using ALD $LaAlO_3$ on $SrTiO_3$ substrate to form a novel all oxide conducting channel is also briefly summarized in this paper.

Experiments in Ge

As device scaling of silicon complementary metal-oxide-semiconductor (CMOS) is approaching its fundamental physical limits, innovative device structure such as FinFET and Gate-all-around FET has been proposed and demonstrated for superior electrostatic control. An alternative approach to continue the trend of scaling is to implement novel channel materials with better transport properties than silicon. Extensive research progress has been made on using III-V materials as n-channel substrates and germanium as p-channel substrate, mainly due to their high electron and hole mobility, respectively. In both cases, one challenging task is on how to form high-quality gate stack with low interface trap density and low equivalent oxide thickness (EOT). Among all the Ge passivation technique, thermally grown GeO_2 is a natural choice and has been proven to be effective in passivating Ge surface (3-9), even better than SiO_2 on Si. On the other hand, high-*k* dielectric having a dielectric constant larger than 20 is favorable to achieve aggressive EOT scaling. Ternary rare earth oxides such as $LaLuO_3$ have been considered promising candidate as "higher-*k*" gate dielectric (8). Recently, superior $LaLuO_3$/Ge

MOS capacitance-voltage (CV) characteristics have been demonstrated with high pressure oxygen annealing (9). However, for device applications, a much thinner GeO_2 layer is required for EOT consideration. We systematically study the effect of thin thermal GeO_2 passivation layer on $LaLuO_3$/Ge gate stack at transistor level, with Smart Cut GeOI as starting substrate. Well-behaved transistor performance is achieved. The effectiveness of thin GeO_2 thermal oxide as passivation layer is demonstrated from both transistor current-voltage and effective hole mobility characterization. The high interface quality is also indicated from the phonon scattering dominated behavior obtained with low temperature MOSFET characterization from room temperature down to 10K. ALD high-k dielectrics can be successfully integrated on Ge with GeO_2 as an interfacial layer.

MOSFET fabrication starts with a 100mm GeOI wafer from SOITEC. The Germanium layer is about 100nm thick, with (100) orientation and an n-type Sb doping lower then $4\times10^{15}cm^{-3}$. The Ge film is separated from the Si substrate by 400nm SiO_2 layer and is produced by layer transfer from bulk Ge. The Si handling wafer has a p-type doping with a resistivity around 14 to 22 ohm·cm. From the substrate parameter, the maximum depletion width is calculated to be around 350nm. Since the maximum depletion width is larger than the Ge film thickness, the fabricated devices operate in fully-depleted (FD) GeOI regime. The GeOI wafer is first treated with cyclic 2% hydrofluoric (HF) acid and de-ionized (DI) water rinse to remove any native oxide present. The rinse is stopped at HF to maintain a hydrophobic surface. Then the wafer is transferred to an oxidation furnace immediately. A ~1.5nm GeO_2 oxide is thermally grown at 450 ^oC in dry oxygen ambient. 5nm $LaLuO_3$ is grown at 350 ^oC in a horizontal gas flow ALD chamber, with $La(amd)_3$ and $Lu(amd)_3$ as precursors. The procedure is one layer of La_2O_3 deposition followed by one layer of Lu_2O_3 deposition and then repeats alternatively. Therefore the final ration of La_2O_3:Lu_2O_3 is 1:1. The ALD $LaLuO_3$ process is done by Yiqun Liu and Roy G. Gordon at Harvard University. Since $LaLuO_3$ is water soluble, another 5nm Al_2O_3 capping layer is deposited in an ASM F-120 ALD reactor at a substrate temperature of 300 ^oC to protect the gate stack throughout the fabrication process. After gate stack formation, BF_2 is implanted at 10 keV with dose of $1\times10^{15}cm^{-2}$ as p-type dopants. The dopant activation is carried out in a N_2 furnace at 450C for 30 minutes. Contact window is opened by BCl_3 dry etching to protect the gate stack from water exposure. After a short 10% HCl dip, 10nm Ti and 70 nm Al is electron beam evaporated as contact metal, followed by contact annealing at 440 ^oC in N_2. Finally, 30nm Ni and 80nm Au is deposited as gate metal.

Figure 1(a) shows the schematic cross section of the device structure of an ALD $LaLuO_3$/GeOI MOSFET with thermal GeO_2 passivation and Al_2O_3 protection layer. The fabricated MOSFETs have a gate width of 100μm and nominal channel length ranging from 2 to 40μm. A Keithley 4200 was used for MOSFET output characteristics. The capacitance measurement was carried out using an HP4284A precision LCR meter with frequencies varying from 1 kHz to 1 MHz. The contact resistance and sheet resistance is determined to be 0.87 Ω·mm and 260.4Ω/□ respectively, both using transfer length (TLM) method. The dielectric constant of the ALD $LaLuO_3$ oxide is determined to be 24 from previous MOS capacitor measurements. Since GeO_2 has a dielectric constant of about 6, the total EOT is estimated to be around 1.14, not counting the capping layer. Figure 1(b) shows the output characteristics of a typical 2μm device with gate voltage from 0 to -5V. The maximum drain current reach 125μA/μm at drain bias of -3V and the transistor is completely pinched off at zero gate bias. Transfer characteristics show an on-

off current ratio of 2300 at V_{ds}=-2V. The threshold voltage (V_T) of devices with GeO_2 passivation is found to be around -0.53V from I_d-V_{gs} curve at low drain bias. However, devices with direct $LaLuO_3$ deposition at same gate length show a threshold voltage of around -0.03V. This means that there exists a ~0.5V positive V_T shift for devices without GeO_2 passivation. Positive V_T shift is indirect evidence that the samples without passivation have a significant higher interface density (10). The charge neutrality level (CNL) in Ge lies close to valence band. The unpassivated n-type surface gives a larger negative interface trap from acceptor states, which tend to facilitate inversion. As a result, the measured threshold voltage for unpassivated surface is shifted to positive gate voltage.

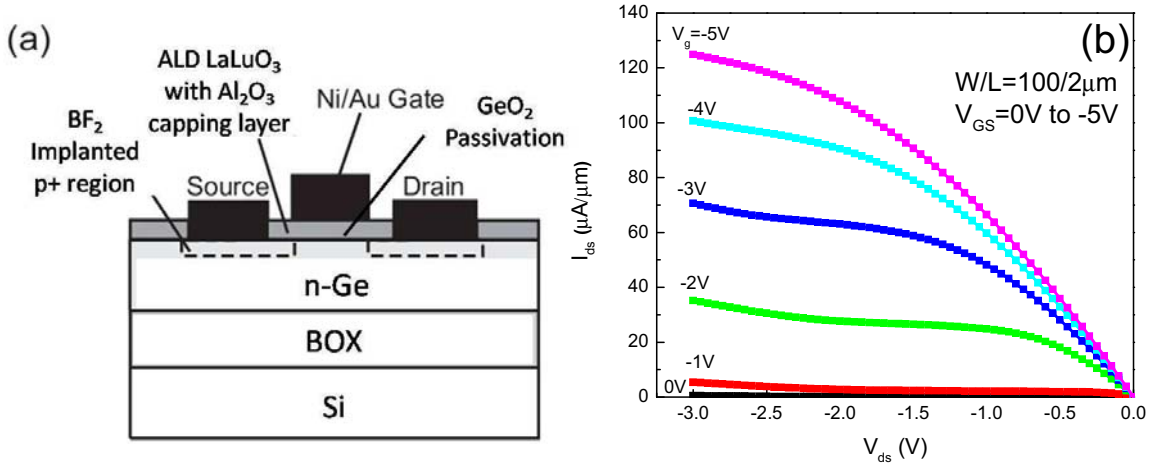

Fig. 1(a) Schematic view of a surface channel GeOI PMOSFET with ALD high-*k* $LaLuO_3$ as gate dielectric. (b) Output characteristics of such a Ge PMOSFET.

Experiments in III-V

In the past 5 years, Purdue group has been intensively studying the ALD integration on III-V compound semiconductors which include GaAs, InGaAs, InAs, InSb, InP, GaN, and GaSb, along with other groups worldwide. (11-30) In general, the integration process can also divided into two steps: surface passivation and ALD high-k deposition. Here In-rich InGaAs is used as an example to address the issues related with ALD/III-V integration.

Fig. 2(a) shows the schematic cross section of the device structure. The channel is 15~20 nm thick $1\times10^{17}/cm^3$ doped p-type $In_{0.53}Ga_{0.47}As$ or $In_{0.65}Ga_{0.35}As$ or $In_{0.75}Ga_{0.25}As$ channel layer, which is MBE epitaxially grown on $In_{0.53}Ga_{0.47}As$/InP substrate. 5~10nm thick ALD Al_2O_3 is used as gate dielectric and Ni or Al is used as gate electrodes. Table 1 show the device fabrication flow. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300°C as an encapsulation layer. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 30 keV and 1×10^{14} cm^{-2} at 80 keV through the 30 nm thick Al_2O_3 layer. Implantation activation was achieved by rapid thermal anneal (RTA) at 700-800 °C for 10 s in a N_2 ambient. An 5~10 nm Al_2O_3 film was then re-grown by ALD after removing the encapsulation layer by BOE etching and ammonia sulfide surface preparation. After 400-600 °C Post Deposition Anealing (PDA), the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA at 400 °C for 30 s also in N_2

ambient. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.40 μm to 40 μm and a gate width of 100 μm. Table 1 shows the device fabrication flow. An HP4284 LCR meter was used for the capacitance measurement and a Keithley 4200 was used for MOSFETs output characteristics. Fig. 2(b) shows transmission electron microscopy (TEM) images of the cross section of $Al_2O_3/In_{0.75}Ga_{0.25}As/In_{0.53}Ga_{0.47}As$ on a similarly finished device. No visible interfacial layer between $Al_2O_3/In_{0.75}Ga_{0.25}As$ interface and relaxation of $In_{0.75}Ga_{0.25}As$ on $In_{0.53}Ga_{0.47}As$ are observed from these TEM images. The native oxide of III-V material has been effectively removed by HCl etching, NH_4OH and $(NH_4)_2S$ pretreatment and the ALD "self-cleaning" process. (31-33)

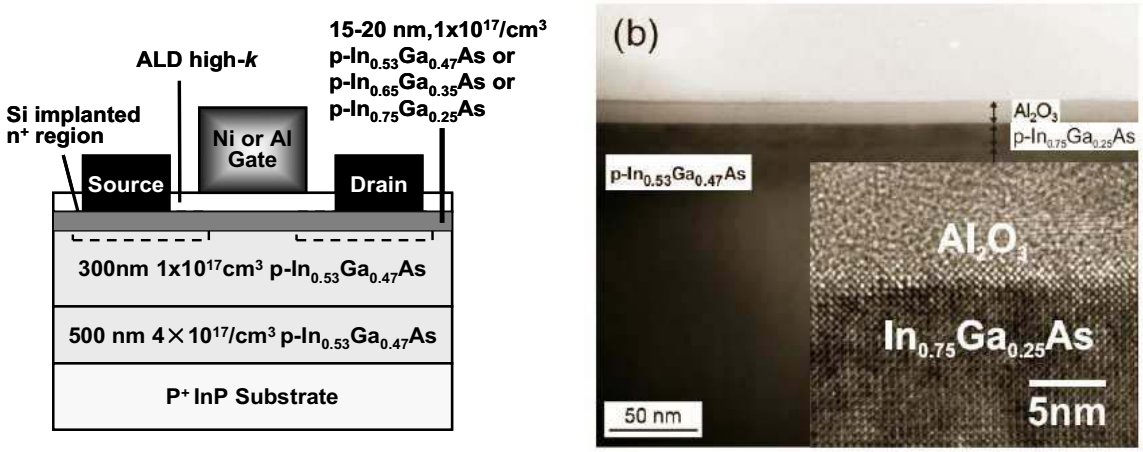

Fig. 2(a) Schematic view of surface channel $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$, and $In_{0.75}Ga_{0.25}As$ NMOSFETs with ALD high-*k* Al_2O_3 as gate dielectrics. (b) TEM image of a similarly fabricated device with 10 nm Al_2O_3. No relaxation of p- $In_{0.75}Ga_{0.25}As$ is observed after 750 °C RTA activation. Inset: high-resolution TEM shows sharp $Al_2O_3/In_{0.75}Ga_{0.25}As$ interface remaining after full device fabrication including 750 °C RTA activation process.

1) NH_4OH surface pretreatment
2) ALD Al_2O_3 30nm as an encapsulation layer
2) S/D patterning and Si implantation (30KeV/1E14 & 80KeV/1E14)
3) S/D activation using RTA (700-800°C 10s in N_2)
4) ALD re-growth: Al_2O_3
5) PDA: 400-600°C 30s in N_2
6) S/D contact patterning and Au/Ge/Ni ohmic metal evaporation and 400°C metallization
7) Gate patterning and Ni/Au or Al/Au evaporation

Table 1. Device process flow of surface channel E-mode In-rich InGaAs NMOSFETs with Ni or Al used as gate electrodes.

Figure 3-5 show the on-state performance of Al_2O_3/InGaAs MOSFETs with indium contents of 0.53, 0.65, and 0.75. Well-behaved I-V characteristic of 0.75-μm gate length inversion-type E-mode $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ NMOSFETs are demonstrated in Fig. 2-4 with the I_{DMAX} of 0.3 A/mm, 0.86 A/mm and 1.0 A/mm, respectively. The gate leakage current (I_G) is less than 10^{-4} A/cm^2 at 4.0 V gate bias (V_G) for all devices. The extrinsic G_m, the intrinsic G_m, and the threshold

voltage V_T for $In_{0.75}Ga_{0.25}As$ NMOSFETs are 0.43 S/mm, 052 S/mm, and 0.5 V respectively.

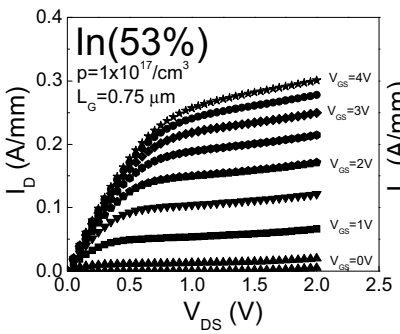

Fig. 3. Drain current (I_D) versus drain bias (V_{DS}) as a function of gate bias (V_{GS}) for Al_2O_3(8nm) / $In_{0.53}Ga_{0.47}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 0.3 A/mm.

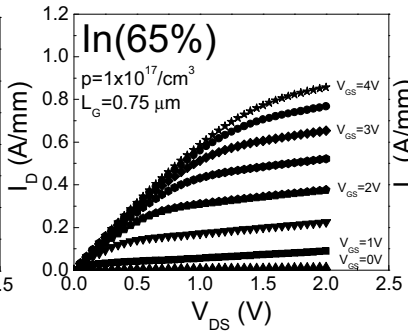

Fig. 4 Drain current versus drain bias as a function of gate bias for Al_2O_3 (10nm) /$In_{0.65}Ga_{0.35}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 0.86 A/mm.

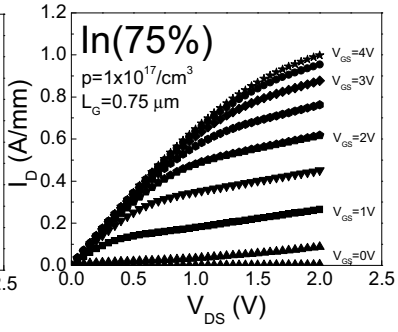

Fig. 5 Drain current versus drain bias as a function of gate bias for Al_2O_3(10nm)/$In_{0.75}Ga_{0.25}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 1.0 A/mm.

Fig. 3-5 show I_{DMAX} and G_m versus different indium content InGaAs MOSFETs with 0.75-μm gate length. The I_{DMAX} and G_m increase with increasing indium content in InGaAs due to the increase of mobility and saturation velocity and reduced contact resistance. Fig. 5 is the scaling characteristics of I_{DMAX} and G_m versus different gate length for different indium content devices. $In_{0.75}Ga_{0.25}As$ NMOSFETs show the best device performance due to its narrowest bandgap of 0.52 eV, which is the easiest to realize inversion, and its largest mobility and saturation velocity. Electron velocity is also studied for all devices with different indium content. The effective electron velocity reached $1.0x10^7$ cm/s for $In_{0.65}Ga_{0.35}As$ at 0.4-μm gate length and for $In_{0.75}Ga_{0.25}As$ at 0.75-μm gate length. The effective electron velocity could be significantly above $1.0x10^7$ cm/s (also the value for Si MOSFET) at deep submicron gate length. Al_2O_3/InGaAs MOSFETs are currently limited with off-state performance and suffer from the severe short-channel effects with gate length down to 150 nm. (34) How to address the short-channel effects by further improving interface quality, implementing retro-grade structure and halo-implantation, and introducing 3D structures such as FinFETs, nanowires FETs or gate-all-around FETs is presented in the recent two IEDM papers (35-36).

Experiments in Nanowires

In the past years, there are enormous efforts to investigate the potential to use bottom-up grown semiconductor nanowires as the future building blocks for nano-electronics. ALD is a natural choice due to its ultra-thin, conformal, and pin-hole free features. Here we just choose one of examples on fully transparent ZnO and In_2O_3 nanowires transistors. The experiment was mainly carried out by Sanghyun Ju and David Janes at Purdue University with the formation of ALD dielectrics from our group. (37)

Development of optically transparent and mechanically flexible electronic circuitry represents an enabling step toward next-generation display technologies,

including "see-through" and conformable products. Nanowire transistors (NWTs) are of particular interest for future display devices because of their high carrier mobilities compared with bulk or thin film transistors using the same materials, the prospect of processing at low temperatures compatible with plastic substrates, as well as their optical transparency and inherent mechanical flexibility. Ref. [37] reports fully transparent NWTs fabricated using all-transparent In_2O_3 and ZnO nanowire active channels, ALD Al_2O_3 gate insulators, ITO source/drain electrodes, and IZO gate electrodes. The representative In_2O_3 NWTs on glass substrates exhibit n-type transistor characteristics with ~90% visible transparency and μ_{eff} varies from ~ 514 to 300 cm^2/V-sec as the gate bias is increased from 0 V to 2 V. The representative ZnO NWTs on glass substrates exhibit ~91% visible transparency with μ_{eff} varying from ~ 96 to 70 cm^2/V-sec over the gate bias range of 0 V to 3 V. Fully transparent and mechanically flexible In_2O_3 NWTs with optical transmission of ~81% are also fabricated on PET plastic substrates with μ_{eff} = 120 ~ 167 cm^2/V-sec over the reported gate bias range. We show here that the excellent transparency and semiconducting properties of In_2O_3 and ZnO nanowires combined with Al_2O_3 as the gate insulator, and ITO and IZO contacts affords high-performance NWTs that are attractive candidates for future flexible transparent display applications.

Except for all nanowires FETs work from bottom-up approach, top-down approach is attracted also more attentions recently. Here we use the first III-V FinFET demonstrated in our group as an example of III-V nanowires FETs from top-down approach. [36] From structure point of view, FinFETs are nanowires FETs are very similar. In order to achieve better gate control capability, new structure design like FinFET demonstrated successfully in Si devices (38-42) is strongly needed for short-channel III-V MOSFETs. However, unlike Si, the dry etching of III-V semiconductor surface has been believed to be difficult and uncontrollable (39), especially related with surface damage and integration with high-k dielectrics. Here, we review the recent work on the first experimental demonstration of inversion-mode $In_{0.53}Ga_{0.37}As$ tri-gate FinFET using damage-free etching and ALD Al_2O_3 as gate dielectric. The short-channel effect (SCE) is greatly suppressed in terms of SS, DIBL and V_T roll-off. Detailed analysis and comparison are performed on the FinFETs with channel length (L_{ch}) from 200 nm to 100 nm, fin width (W_{Fin}) from 100 nm to 40 nm, and fixed fin height (H_{Fin}) of 40 nm. The reduction in the SCE shows the great promise for InGaAs transistors to continue scale into the sub-100nm regime. Fig. 6 and Fig.7 show the schematic cross section of the uniform device structure and the device fabrication flow. A 500 nm p-doped 2×10^{18} cm^{-3} InP layer, a 300 nm p-doped 2×10^{16} cm^{-3} and a 40 nm 2×10^{16} cm^{-3} $In_{0.53}Ga_{0.47}As$ channel layer were sequentially grown by MBE on a 2-inch InP p+ substrate. The heavily doped InP layer beneath the channel was chosen to prevent punch through and reduce substrate leakage because of its higher bandgap.

Due to the non-optimized source/drain junctions, the heavily doped InP layer resulted in worsen junction leakage. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor.. A 10 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300^oC as an encapsulation layer. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 20 keV through the 10 nm thick Al_2O_3 layer. The implantation condition was chosen carefully to achieve the desired junction depth and S/D doping concentration. Implantation activation was achieved by RTA at 600 ^oC for 15 s in a

nitrogen ambient. The reduction of activation temperature from 750 °C to 600 °C resulted in much improved S/D junction leakage while achieving similar activation efficiency.

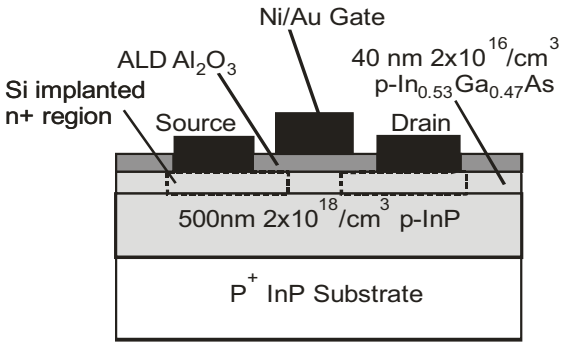

Fig. 6 Cross-section schematic view of the InGaAs FinFET.

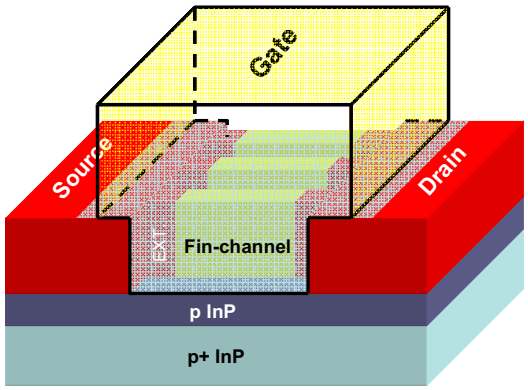

Fig. 7 Three-dimensional schematic view of the $In_{0.53}Ga_{0.47}As$ FinFET

A combined dry and wet etching was used to pattern the fin structures. High-density plasma etcher (HDPE) BCl_3/Ar was used for dry etching at the chamber pressure of 2 mTorr. The gas flow of BCl_3/Ar is 15 sccm/ 60 sccm and the RF source power and bias power is 100 w and 50 w, respectively. The achieved etching rate for InGaAs under this condition is estimated to be 20nm / min. The positive E-beam resist ZEP-520A was used as an etching mask in this case. To achieve the desired small feature of 40nm, the original ZEP 520A resist was diluted with A-thinner (anisole) at the ratio of 1:0.7. The resist thickness of the diluted ZEP 520A is around 200nm at a spinning speed of 2000 rpm. A short dip of 3 seconds in diluted H_2SO_4:H_2O_2:H_2O (1:8:400) solution was carried out immediately after the dry etching to remove the damaged surface layer.

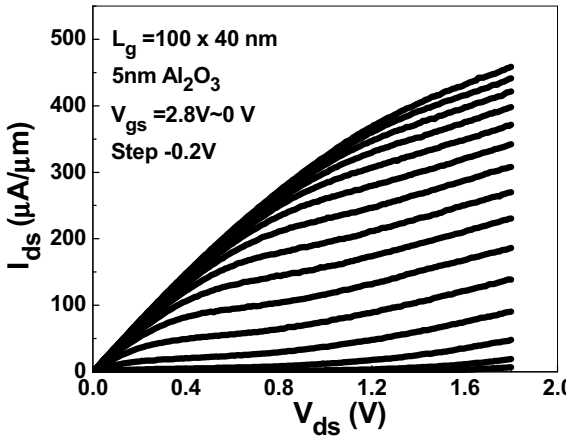

Fig. 8 I_{ds} vs V_{ds} of a FinFET with L_{ch}=100 nm and W_{Fin}=40nm

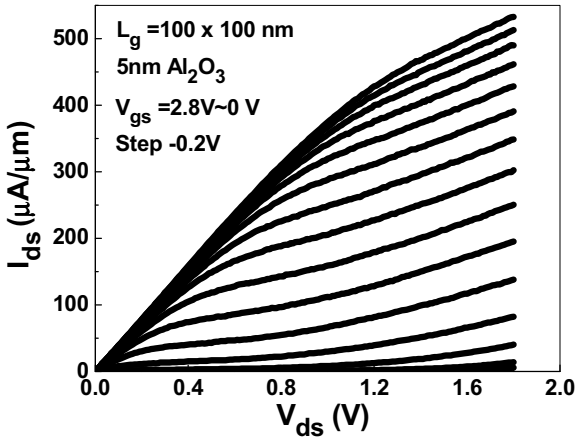

Fig. 9 I_{ds} vs V_{ds} of a FinFET with L_{ch}=100 nm and W_{Fin}=100nm

More sophisticated process is needed to make the fin side-walls perfectly vertical. A 5 nm Al_2O_3 film was regrown by ALD after removing the encapsulation layer by BOE solution and $(NH_4)_2S$ surface preparation. After 400-500 °C PDA process, the source and drain ohmic contacts were made by an electron-beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA process at 320 °C for 30 s also in a N_2 ambient. The gate electrode was deposited by electron- beam evaporation of Ni/Au

and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 100 nm to 150 nm and fin widths from 40 nm to 100 nm. The gate metal covers uniformly on the parallel multi-fin channels. The combined dry and wet etching for the formation of fin channels results in damage-free sidewalls. It is verified by the carrier transport through the fin channels without any significant degradation, compared to the planar devices. Fig. 8 and Fig. 9 depict the well-behaved output characteristic of a FinFET with 40 nm and 100nm W_{Fin} at same channel length of 100nm. There is no significant reduction of drain current even when the fin width is reduced down to 40 nm dimension. Note the current density is scaled by the fin width plus 2 x fin heights. The FinFETs have much better behaved output characteristics in terms of off-state due to the better electro-static control of the channel while maintaining the on-state performance compared to the planar device. It is expected to have even better off-state performance with smaller dimensions (nanowires) and gare-all-around (GAA) FET structures.

Experiments in CNTs and graphene

Since their discovery in 1991 (43), carbon nanotubes (CNTs) have been the focus of extensive research for many potential applications, including sensing, chemistry, biology, and electronics (44-46). Single walled carbon nanotubes (SWNTs) are rolled up sheets of graphite with diameter of 1~3 nm and are available in both single-walled and multi-walled forms. Due to perfect one-dimensional crystalline structure, SWNTs exhibit unusual physical, chemical, mechanical and electrical properties. Single-walled carbon nanotube field effect transistors (SWNT-FETs) were first demonstrated in 1998 (47). It has been demonstrated that these transistors can achieve ballistic transport, can sustain high current densities while dissipating very low DC powers (48-49). Despite the advantages of SWNT-FETs, these devices have not been utilized in industry due to two major hurdles in realization of large area and/or complex circuits based on these transistors. These two issues are: *(1)* Difficulty in the separation of semiconducting from metallic single-walled carbon nanotubes; *(2)* Difficulty in alignment and placement of the nanotubes to the device structure in a controlled and reproducible fashion. Up to now, various methods for selective deposition or growth of single walled carbon nanotubes (SWNTs) on two electrodes have been developed (50-51). In the past years, we deposited ALD Al_2O_3 and HfO_2 dielectrics on CNTs with two different aligning techniques and fabricated and characterized high-performance SWNT-FETs. The work is mainly carried out by Sunkook Kim and Saeed Mohammadi at Purdue University and published in Ref. (52-53). In the first method, room temperature device fabrication is achieved based on dielectrophoresis. Individual SWNTs and SWNT bundles suspended in ethanol solution display a positive dielectrophoresis which facilitate their alignment and placement through a very simple processing technology. It was found that the electrical performance of these devices is limited by their high contact resistance of SWNT bundles which is in the order of a few MΩ. In the second technique, alignment of nanotubes to the devices structure is achieved through high temperature CVD synthesis of nanotubes on a quartz wafer (54). Parallel arrays of individual SWNTs with a controlled density are utilized to construct high performance SWNT-FETs. This technology allows implementation of SWNT-FETs with low contact resistance, high mobility, and high saturation current.

Graphene, a monolayer of carbon atoms tightly packed into a two-dimensional (2D) hexagonal lattice, has recently been shown to be thermodynamically stable and exhibits astonishing transport properties, such as an electron mobility of ~15,000 cm^2/Vs

and an electron velocity of ~10^8 cm/s at room temperature. (55) High-quality monolayer graphene has been obtained in small (tens of microns) areas by exfoliation of highly-ordered pyrolytic graphite (HOPG) and transferred onto SiO_2 substrates for further device fabrication (56,57). However, this exfoliation process cannot form the basis for a large-scale manufacturing process. Recent reports of large-area epitaxial graphene by thermal decomposition of SiC wafers have provided the missing pathway to a viable electronics technology (58-65). The advantage of epitaxial graphene for nanoelectronic applications resides in its planar 2D structure that enables conventional top-down lithography and processing techniques. Except for opening the bandgap by forming graphene nano-ribbons, an additional challenge for graphene based electronics is the formation of high-quality, ultrathin dielectrics with low interface trap density. A perfect graphene surface is chemically inert, which does not lend itself to conventional ALD high-k dielectrics. (66) Numerous efforts (67-71) were carried out in this field using certain seeding layer or interfacial layer as Ge or III-V. It can be summarized as (1) TMA + NO_2 seeding layer (67) (2) TMA+O_3 seeding layer (68) (3) fully oxidized Al seeding layer (69,70) (4) organic PTCA seeding layer (71). Much more work is needed to characterize the interface quality and optimize the dielectric formation process at device level. Our approach is to form ALD high-k gate stack integration on epitaxial graphene films by inserting a fully oxidized aluminum film as a seeding layer. The gate stack formation does not degrade the electrical properties of epitaxial graphene films. The quantum Hall effect (QHE) is observed in gated epitaxial graphene films on SiC (0001), along with pronounced Shubnikov-de Haas (SdH) oscillations in magneto-transport. The observation of quantum features demonstrates the reasonable success of integration of ALD high-k on graphene. (70)

The graphene films were grown on semi-insulating 4H-SiC substrates in an Epigress VP508 SiC hot-wall chemical vapor deposition (CVD) reactor. The graphene synthesis work is carried out by Mike Bolen and Michael Capano at Purdue University. The off-cut angle of the substrate is nominally zero degrees. Prior to growth, substrates are subjected to a hydrogen etch at 1600 ^oC for 5 minutes, followed by cooling the samples to below 700 ^oC. After evacuating hydrogen from the system, the growth environment is pumped to an approximate pressure of 2×10^{-7} mbar before temperature ramping at a rate of 10-20 ^oC/min and up to a specified growth temperature. The growth conditions, film morphology, and electrical properties of the epitaxial graphene films differ markedly between films grown on the C-face and films grown on the Si-face. The formation of graphene on C-face is very rapid at the growth temperature of 1500-1650 ^oC in vacuum. At growth temperatures $\geq$ 1550 ^oC, several-micron large regions of smooth graphene films are obtained with tens of nanometers high ridges as domain boundaries.[16] Without gate stacks, the multi-layer graphene films on C-face are mostly p-type with a typical Hall mobility of 5000-6000 cm^2/Vs. On Si face, continuous few-layer graphene only starts to form at 1550 ^oC. The growth on Si-face is much slower, making it possible to form single layer graphene with a better controlled process. (72-73) The morphology of graphene films on the Si-face is quite homogenous compared to those films on the C-face. However, the typical Hall mobility of graphene on Si-face is ~ 1300-1600 cm^2/Vs. The carriers are always n-type from Hall measurements without gate dielectrics. The particular graphene films shown in this work were grown at 1600 ^oC for 10 minutes in vacuum.

The detailed device structure is shown in Fig. 10(a). The device isolation was achieved by O_2 plasma mesa dry etching. 1 nm of aluminum metal film was evaporated onto the sample by electron-beam evaporation at ~ 10^{-6} Torr, and fully oxidized in an oxygen rich ambient for 1 hour as a seeding layer for ALD growth. 30 nm Al_2O_3 as gate dielectric was deposited at 300 ^oC using an ASM F-120 reactor with tri-methyl aluminum and water vapor as the precursors. The metal contacts and gate electrodes were subsequently patterned and deposited, both using electron-beam evaporated Ti/Au. The active device area for magneto-transport has a width of 10 μm and a length of 22 μm.

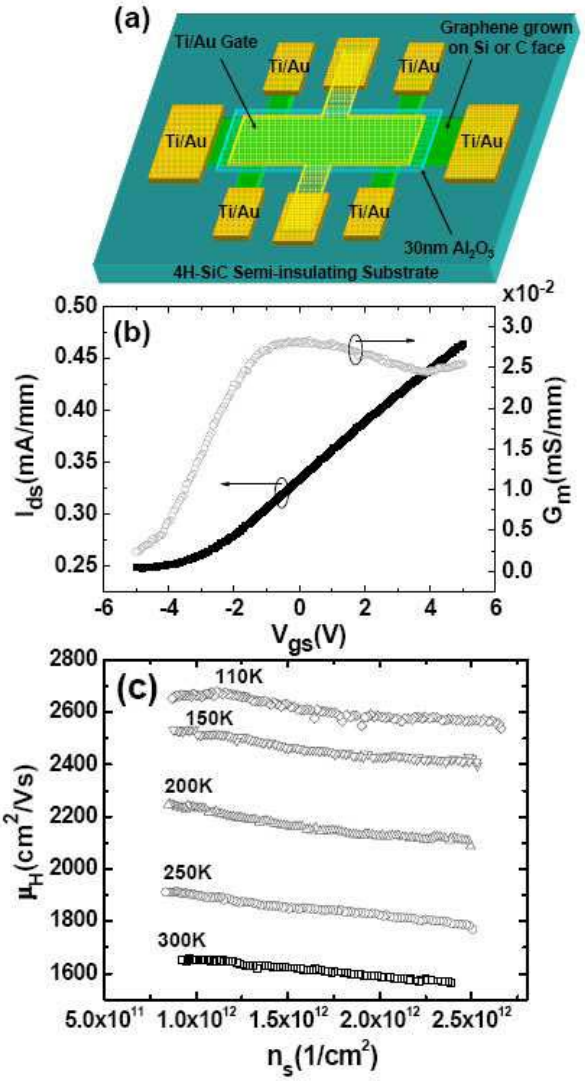

Figure 10 (a) Schematic view of the graphene Hall-bar device structure on SiC (0001) with ALD Al_2O_3 as gate dielectric. (b) Drain current (left) and trans-conductance (right) versus gate bias at drain voltage of 50 mV for the fabricated graphene FET as shown in (a). (c) Hall mobility of the epitaxial graphene on SiC (0001) versus carrier density at various measurement temperatures.

Figure 10(b) shows the dc I_{ds}–V_{gs} and G_m–V_{gs} characteristics with a gate bias from -5.0 to 5.0 V and V_{ds}=50 mV on a Hall-bar device with a partially-covered gate, as shown in Fig. 1(a). The left and right terminals of the Hall-bar serve as source and drain. The measured graphene field-effect transistor (FET) has a designed gate length (L_g) of 30 μm

and a gate width (L_w) of 10 μm. The drain current can be modulated by ~46% with a few volts gate bias, similar to the previous work with SiO_2 as gate dielectric.[5] The device cannot be turned off due to the zero-bandgap of graphene films. The monotonic reduction in drain current with negative gate bias also confirms that the carriers in graphene films on SiC (0001) are n-type. The slope of the drain current shows that the peak extrinsic transconductance (G_m) is ~ 2.8×10^{-2} mS/mm, due to its extraordinarily large gate length and low drain bias. The Hall mobility and electron density of the graphene film are characterized at different gate biases and at different temperatures in Figure 10(c). The room temperature Hall mobility is ~ 1600 cm^2/Vs and decreases slightly with the increase of electron densities. There is also no significant Hall mobility degradation with gate stacks as compared to similar devices without gate dielectrics, indicating that the gate dielectric has reasonable quality without significant bulk traps and interface traps. The Hall mobility increases rapidly as temperature decreases and reaches ~2600 cm^2/Vs at 110K, and ~3600 cm^2/Vs at 4.2K due to the suppression of electron-phonon scattering in epitaxial graphene films. In magneto-transport measurements, pronounced QHE and SdH are observed on this epitaxial graphene, as shown in Figure 11, confirms that epitaxial graphene on SiC (0001) and exfoliated single-layer graphene are governed by the same relativistic physics with Dirac particles as transport carries.

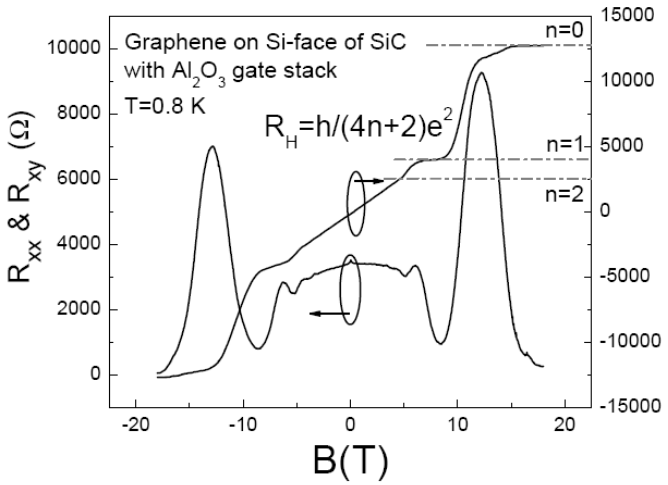

Figure 11 Hall resistance and magneto-resistance measured in the device in Figure 10(a) at T=0.8K and with floating gate bias. The horizontal dashed lines corresponding to $h/(4n+2)e^2$ values. The QHE of the electron gas in epitaxial graphene is shown one quantized plateau and two developing plateau in R_{xy}, with vanishing R_{xx} in the corresponding magnetic field regime.

Experiments in all oxide electronics

The class of transition metal oxide compounds exhibit a broad range of functional properties, such as high dielectric permittivity, piezoelectricity and ferroelectricity, superconductivity, spin polarized current, colossal magnetoresistance and ferromagnetism. Almost all this phenomenology results from strongly correlated electronic behavior and turned out to be very sensitive to external parameters such as electric and magnetic fields, internal or external pressure and so on. Polarity discontinuities at the interfaces between two different crystalline materials or called hetero-interfaces are believed to the key to lead to non-trivial effects. In 2004, Ohtomo and Hwang reported a high-mobility electron gas could be formed at the crystalline

$LaAlO_3/SrTiO_3$ hetero-interface with the materials grown at ultra-high vacuum and pulsed laser deposition technique. (74) It is widely believed that that conducting oxide/oxide interface needs to be atomically engineered oxide heteroepitaxy in order to achieve conducting channels.

Here we brief report for the first time that the conducting channel can be formed at amorphous $LaAlO_3$/crystalline $SrTiO_3$ interface by simply ALD of $LaAlO_3$. The ALD LaAlO3 film is deposited by Yiqun Liu and Roy G. Gordon at Harvard University and the device fabrication and characterization is carried out at Purdue University. Figure 12 shows the output characteristics a FET formed on $LaAlO_3/SrTiO_3$ interface with gate length of 20 µm. An interesting point is that ALD $LaAlO_3$ not only provides the hetero-oxide-interface to induce the channel, it also serves as high-k gate dielectric for top metal gate to electro-statically control the conduction channel. More investigation on this novel all oxide electronic material is on-going.

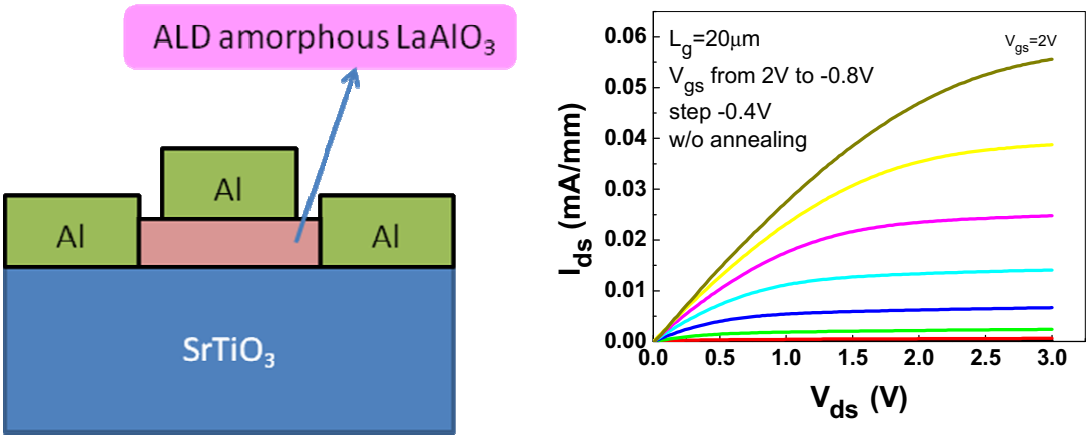

Fig. 12 Schematic view of a surface channel ALD $LaAlO_3/SrTiO_3$ FET. (b) Output characteristics of such a surface channel ALD $LaAlO_3/SrTiO_3$ FET.

Summary

In summary, we have systematically studied the different ALD gate dielectrics on different channel materials with the focus for future nanoelectronics applications. The ALD gate dielectrics include Al_2O_3, HfO_2, ZrO_2, $LaAlO_3$ and $LaLuO_3$. The channel materials include Ge, GaAs, InGaAs, InAs, InSb, InP, GaN, GaSb, CNT, graphene, and all oxide conducting hetero-interface $LaAlO_3/SrTiO_3$. Our conclusion is all these results show that ALD high-k can be used as a common gate stack solution for novel channel materials such as Ge, III-V, semiconductor nanowires, CNTs, graphene and all oxide electronic materials. The interfacial control layer is the key to the successful integration. Different channel materials require specific passivation or interfacial control layer, based on channel physical, chemical and electronic properties, before ALD high-k dielectric formation.

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