High-Performance Inversion-Type Enhancement-Mode InGaAs MOSFET With Maximum Drain Current Exceeding 1 A/mm

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***Abstract*—High-performance inversion-type enhancement-mode (E-mode) n-channel $In_{0.65}Ga_{0.35}As$ MOSFETs with atomic-layer-deposited Al_2O_3 as gate dielectric are demonstrated. A 0.4-μm gate-length MOSFET with an Al_2O_3 gate oxide thickness of 10 nm shows a gate leakage current that is less than 5×10^{-6} A/cm^2 at 4.0-V gate bias, a threshold voltage of 0.4 V, a maximum drain current of 1.05 A/mm, and a transconductance of 350 mS/mm at drain voltage of 2.0 V. The maximum drain current and transconductance scale linearly from 40 μm to 0.7 μm. The peak effective mobility is $\sim$1550 cm^2/V $\cdot$ s at 0.3 MV/cm and decreases to $\sim$650 cm^2/V $\cdot$ s at 0.9 MV/cm. The obtained maximum drain current and transconductance are all record-high values in 40 years of E-mode III–V MOSFET research.**

***Index Terms*—Atomic layer deposited (ALD), compound semiconductor, enhancement mode (E-mode), inversion, MOSFETs.**

I. Introduction

IN THE PAST four decades, great efforts have been made to produce "perfect" insulators for III–V MOSFETs. The literature testifies enormous efforts in this field [1]–[16]. The new cycle of interest in III–V MOSFETs is motivated to look for alternative device technologies beyond Si CMOS, whereas silicon technology is going to reach its physical limit next decade [17]. III–V is one of its main focuses due to its high electron mobility. For future high-speed low-power logic applications, only inversion-type enhancement-mode (E-mode) III–V MOSFET is of interest.

Inversion-mode surface-channel $In_xGa_{1-x}As$ MOSFETs with In concentrations of 20%, 53%, and 65% integrated with conventional atomic-layer-deposited (ALD) Al_2O_3, HfO_2, and HfAlO are systematically studied [8], [13], [14], [16]. In this letter, we report high-performance inversion-type E-mode $In_{0.65}Ga_{0.35}As$ MOSFETs using ALD Al_2O_3 as gate dielectric. The maximum drain current of 1.05 A/mm and extrinsic transconductance of 350 mS/mm for a 0.4-μm gate-length MOSFET are achieved, which are the record-high values in 40 years of III–V MOSFET research. Al_2O_3, which is formed by trimethylaluminum and water vapor, is an ideal ALD process. It has a high bandgap ($\sim$9 eV), a high-breakdown electric field (5–30 MV/cm), a high permittivity (8.6–10), and high thermal stability (up to at least 1000 °C) and remains amorphous under typical processing conditions. The similar ALD process of HfO_2 and HfAlO or other high-κ dielectrics could also be applied to this device structure and significantly reduce the equivalent oxide thickness down to 1–3 nm [14], [18].

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II. Device Structure and Fabrication

Fig. 1(a) shows the cross-sectional schematic of the device structure of an ALD $Al_2O_3/In_{0.65}Ga_{0.35}As$ MOSFET. A 500-nm p-doped 4×10^{17} cm^{-3} buffer layer, a 300-nm p-doped 1×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$ layer, and a 20-nm strained p-doped 1×10^{17} cm^{-3} $In_{0.65}Ga_{0.35}As$ channel layer were sequentially grown by MBE on a 2-in InP p+ substrate. After surface degreasing and ammonia-based native oxide etching [19], the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30-nm-thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C as an encapsulation layer.

For device fabrication, source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 30 keV and 1×10^{14} cm^{-2} at 80 keV through the 30-nm-thick Al_2O_3 layer. Implantation activation was achieved by rapid thermal anneal (RTA) at 750 °C for 10 s in a nitrogen ambient. A 10-nm Al_2O_3 film was regrown by ALD after removing the encapsulation layer by buffered-oxide-etch solution and soaking in ammonia sulfide for 10 min for surface preparation. After 500-°C post-deposition-annealing in N_2 ambient, the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a liftoff process, followed by an RTA process at 400 °C for 30 s also in a N_2 ambient. The gate electrode was defined by electron beam evaporation of Ni/Au and a liftoff process. The fabricated MOSFETs have a nominal gate length varying from 0.4 to 40 μm and a gate width of 100 μm. An HP4284 LCR meter was used for the capacitance measurement, and a Keithley 4200 was used for MOSFET output characteristics. The conducting substrate was connected with the source by all measurements.

III. Results and Discussion

Fig. 1(b) shows the dc $I_{ds}-V_{ds}$ characteristics with a gate bias from 0 to 4.5 V in steps of +0.5 V. The measured MOSFET has a gate length L_g of 0.4 μm and gate width of 100 μm. A 0.4-μm gate length was achieved by a controllable overdevelop process with a 0.5-μm gate length designed from photo mask. A maximum drain current of 1.05 A/mm is obtained at a gate bias of 4.5 V and a drain bias of 2.0 V. The device performance improved in drain current by a factor of three

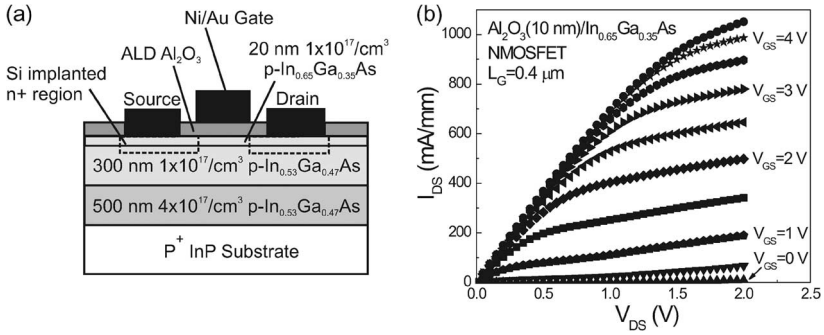

Fig. 1. (a) Cross section of an inversion-type E-mode $Al_2O_3/In_{0.65}Ga_{0.35}As$ MOSFET. (b) I–V characteristic of a 0.4-μm gate-length $In_{0.65}Ga_{0.35}As$ MOSFET with a 10-nm ALD Al_2O_3 as gate dielectric.

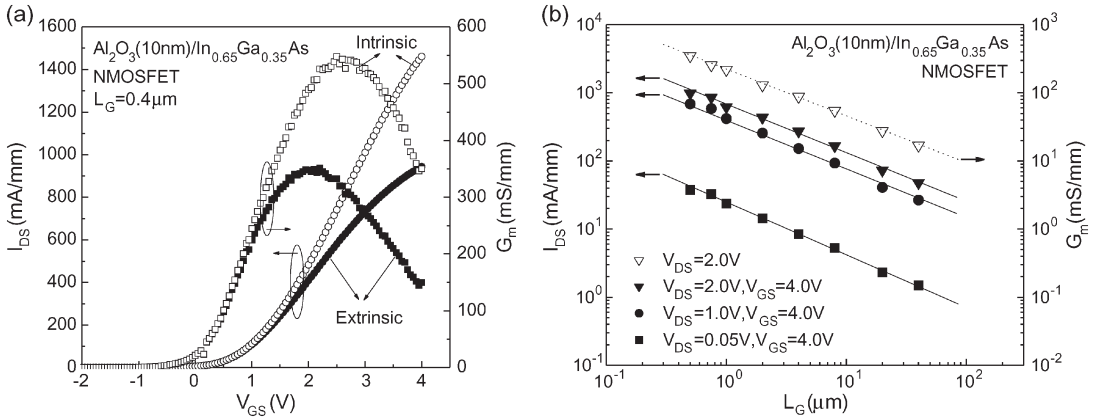

Fig. 2. (a) Extrinsic and intrinsic drain current and transconductance versus gate bias at $V_{\rm DS} = 2.0$ V. (b) Extrinsic drain current at $V_{\rm GS} = 4.0$ V and $V_{\rm DS} = 2.0$ V, $V_{\rm DS} = 1.0$ V, or $V_{\rm DS} = 0.05$ V versus L_G and the extrinsic peak G_m at $V_{\rm DS} = 2.0$ V versus L_G. The solid and dotted lines are guided by eyes.

compared to our previous results on $In_{0.53}Ga_{0.47}As$ MOSFETs [13], [14]. We ascribe this improvement to the following facts. First, $In_{0.65}Ga_{0.35}As$ has higher electron mobility and saturation velocity than $In_{0.53}Ga_{0.67}As$. Second, In-rich InGaAs has much higher intrinsic carrier concentrations. The required surface potential movement to realize strong inversion for In-rich InGaAs is much smaller than that required for GaAs. Most importantly, the charge neutrality level of $In_{0.65}Ga_{0.35}As$ is only $\sim$0.15 eV below the conduction band minimum as compared to $\sim$0.27 eV for $In_{0.53}Ga_{0.47}As$ and $\sim$0.80 eV for GaAs [16]. It does not build up a large amount of negative trapped charges at the interface to prevent further introducing inversion carriers by field effect.

The gate leakage current is below 5×10^{-6} A/cm^2 at 4.0-V gate bias, which is more than eight orders of magnitude smaller than the drain on-current. A series resistance $(R_{\rm SD})$ is extracted to be 1.5 $\Omega \cdot$ mm by transmission line method. A maximum extrinsic transconductance G_m is $\sim$350 mS/mm at $V_{\rm DS} =$ 2.0 V. The extrinsic G_m could be further improved by reducing the equivalent oxide thickness of the dielectric. To evaluate the output characteristics more accurately, the intrinsic transfer characteristics are calculated by substracting the half of $R_{\rm SD}$ and are compared with extrinsic ones in Fig. 2(a). The resulting intrinsic maximum drain current and transconductance for 0.4 μm device are 1.5 A/mm and 550 mS/mm, respectively. By the conventional linear region extrapolation method or second derivative method, the extrinsic threshold voltage is determined around 0.4 V. The source–drain leakage current is another issue for narrow-bandgap semiconductor devices caused mainly by drain-induced barrier-lowering (DIBL) effect. The DIBL is 330 mV/V for a 0.4-μm gate-length device. On/Off ratio is $\sim$150 at $V_{\rm GS} = 4.0$ V (on) and $V_{\rm GS} = 0$ V (off), and $V_{\rm DS} = 2.0$ V on these devices. The subthreshold swing (SS) is 330 mV/decade. The DIBL, On/Off ratio, and SS need to be improved by further optimizing the fabrication process. DC "Split-CV" method is used to measure the effective mobility $\mu_{\rm eff}$. $\mu_{\rm eff}$ has a peak value of 1550 cm^2/V $\cdot$ s around a normal electric field $E_{\rm eff}$ of 0.30 MV/cm, and 650 cm^2/V $\cdot$ s at 0.9 MV/cm, which is about two to three times higher than Si universal mobility [20].

Fig. 2(b) summarizes all the measured drain current $I_{\rm DS}$ versus $1/L_G$ under $V_{\rm GS} = 4.0$ V and $V_{\rm DS} = 2.0$ V, $V_{\rm DS} = 1.0$ V, or $V_{\rm DS} = 0.05$ V. The drain current or transconductance is linearly inversely proportional to L_G as expected and does not saturate at submicrometer gate length. For a simple linear extrapolation, we expect to have the maximum drain current of 2.5 A/mm at $V_{\rm DS} = 1.0$ V and 4.0 A/mm at $V_{\rm DS} = 2.0$ V for 0.1-μm gate-length devices not considering parasitic resistance and short-channel effect. Note that most of commercial GaAs technology, such as pseudomorphic high-electron-mobility transistor (pHEMT), has a maximum drain current around 400 mA/mm at 0.25-μm gate length. For GaAs pHEMT, due to its high low-field mobility, the maximum drain current is mainly limited by the saturation velocity, modulation doping concentration, and heterostructure itself. The maximum drain current saturates at 5–10-μm gate length and does not scale with gate length for short gate-length devices. In contrast to GaAs pHEMT, the demonstrated surface-channel InGaAs MOSFET,

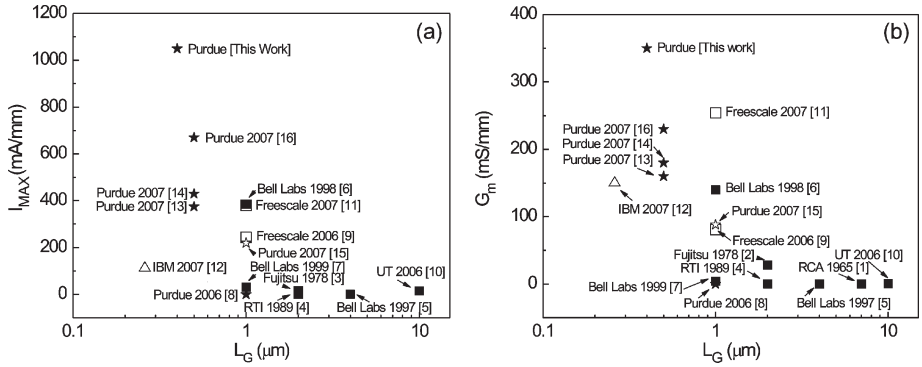

Fig. 3. Historical comparison of published dc (a) maximum drain current I_{MAX} and (b) transconductance G_m of n-channel E-mode III–V MOSFETs from 1965 until today.

which is more or less like real Si MOSFET, has the gate-length scalability down to submicrometer, as shown in Fig. 2(b). It might be related with the exhibiting interface states.

Fig. 3(a) and (b) shows a comparison of maximum drain current (I_{MAX}) and peak transconductance (G_m) of the most representative III–V E-mode MOSFETs reported over the last 40 years. Depletion-mode devices and p-channel devices are not included since they are not the focus of this letter. Implant-free [9], [11], buried-channel [12], or MOS-HEMT [15]-type E-mode III–V devices are still included, although the channels of these devices are located at III–V semiconductor heterojunctions instead of oxide–III–V semiconductor interfaces. Empty signs are used to distinguish these works from the true inversion-type surface-channel devices, whose data are presented by the solid signs. The data in [21] are not included since it is not an E-mode device with $V_T \sim -0.5$ V. The device performance reported in this letter has the highest values in I_{MAX} and G_m over all prior E-mode III–V MOSFETs.

IV. Conclusion

In summary, we have demonstrated unprecedented high-performance inversion-type E-mode $In_{0.65}Ga_{0.35}As$ MOSFETs using ALD high-κ gate dielectrics with record-high values in I_{MAX} and G_m. These results suggest that In-rich InGaAs could be an ideal channel material, which has higher electron effective mobility, higher saturation velocity, is able to introduce large inversion carriers or inversion current, and still has wide enough bandgap for high-speed low-power logic applications.

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