Effects of Positive and Negative Stresses on III–V MOSFETs With Al_2O_3 Gate Dielectric

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***Abstract*—We subjected III–V InGaAs MOSFETs to positive and negative gate stresses. The stress polarity strongly affects the degradation kinetics of the gate current. Positive stress features a remarkable increase of the gate current, a net negative trapped charge, a large telegraphic noise, and soft breakdown, before the occurrence of the final catastrophic breakdown. Negative stress features only positive trapped charge until the hard breakdown.**

***Index Terms*—III–V MOSFET, stress, reliability.**

I. Introduction

HIGH-SPEED low-power digital applications require high-transconductance devices to achieve low propagation delays at reduced power supply voltages [1]. The decrease of the power supply voltage strongly reduces the dynamic power dissipation, but, unluckily, it also increases propagation delays. Hence, strong efforts are being invested to find new materials and structures to achieve high-transconductance values, such as high-k gate dielectrics and strain techniques [2].

A bottleneck for the CMOS technology is the low silicon mobility, whose values (even with strained Si) are much smaller than those of III–V semiconductors (see, for instance, [3] and [4]), which have been therefore evaluated [4]–[6] as possible replacement to silicon for high-speed MOSFETs.

Nowadays, several works on III–V MOSFETs are currently being published on new record-breaking transconductance and mobility values [4], [5], but very little is known about their reliability. In this paper, we show for the first time, to our knowledge, the effects of positive and negative gate ramp stresses, focusing on the evolution of the gate current during stress and the interface and bulk trapped charge build up.

II. Experiment and Devices

We carried out positive and negative gate ramp stresses on inversion-type enhancement-mode InGaAs MOSFETs with a 5-nm Al_2O_3 gate dielectric, Ni–Au metal gate, and a 5-μm channel width. A 500-nm $4 \times 10^{17}/\text{cm}^3$-p-type doped buffer layer, a 300-nm $1 \times 10^{17}/\text{cm}^3$-p-type $In_{0.53}Ga_{0.47}As$ layer, and a 12-nm strained $1 \times 10^{17}/\text{cm}^3$-p-type $In_{0.75}Ga_{0.25}As$ channel were sequentially grown by molecular beam epitaxy over a p^+-InP substrate. The interested reader may refer to [6] for details on device structure and electrical characteristics. The gate lengths (L) considered in this paper were 150, 200, and 250 nm.

We subjected the devices to several stress-characterization steps, until the oxide breakdown was reached. Each step starts with a 100-s constant voltage stress (CVS) at the gate with the other terminal grounded. Then, to neutralize any unstable trapped charge, which may affect the characterizations, a 200-s relax phase (-0.5- or 0.5-V gate bias for the positive stress or negative stress, respectively) is applied after each CVS with the other terminals grounded. After that, the transcharacteristics are measured, and a new stress step is performed increasing the absolute value of the stress voltage ($|V_{\text{STRESS}}|$) by 0.1 V.

III. Results and Discussions

A. Gate Current Stress Kinetics

In Fig. 1, we show the absolute gate current value ($|I_G|$) evolution measured during each CVS step (omitting the relax phase for clarity) for the positive and negative stresses. For clarity, we plotted only one representative curve for each stress polarity. $|V_{\text{STRESS}}|$ is also shown in Fig. 1 (see right axis).

Noticeably, positive and negative stresses behave much differently. For instance, during each CVS step with negative polarity, $|I_G|$ slowly decreases after current spike, suggesting the presence of bulk and border traps in the Al_2O_3, as also found in [7] and [8]. Since the trap density is finite, $|I_G|$ diminishes with time in a saturating behavior. The charging of the gate and cable parasitic capacitances (less than 100 pF) are not responsible for this evolution because the charging transient expires in a time as short as few nanoseconds, much shorter than the sampling time (1 s).

This kinetic is observed until the hard breakdown suddenly occurs at V_{STRESS} between -4.1 and -4.3 V, which corresponds to an Al_2O_3 field of $\sim$8 MV/cm, in agreement with other works on Al_2O_3 [9]. During positive stress, instead, the degradation kinetics can be divided in three distinct regions which will be discussed as follows. Fig. 1(b)–(d) shows one representative of the $|I_G|$ versus time plot during a single step for each region.

The decreasing $|I_G|$ evolution of each stress step in Region 1 ($V_{\text{STRESS}} < 2.9$ V) is very similar to that observed in negative stress, and it can be ascribed to the bulk/border Al_2O_3 traps.

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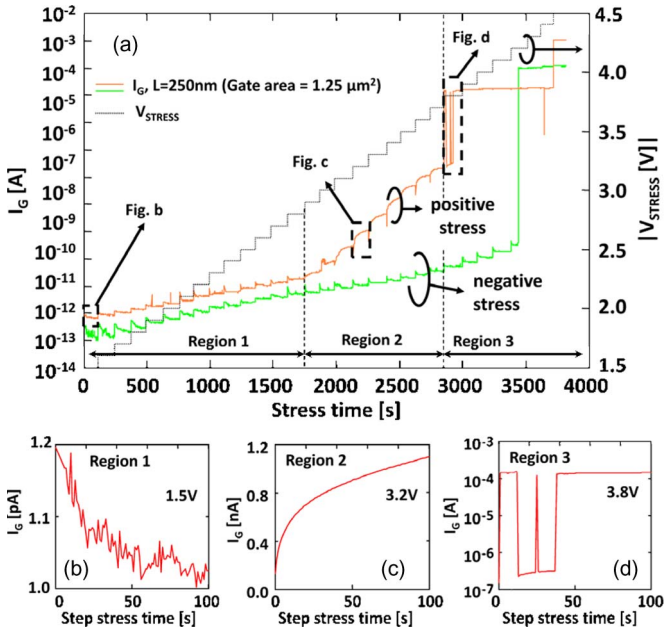

Fig. 1. (a) Gate current during the positive and negative stresses. (Right axis) The dotted line is the absolute value of the stress voltage. The positive stress shows three regions with peculiar behaviors. Zooms of the gate current in one step of Regions 1 (b), 2 (c), and 3 (d).

When the stress voltage is between 2.9 and 3.8 V (Region 2), $|I_G|$ increases during each stress step [Fig. 1(c)], suggesting that the stress is generating new traps, and the increase of $|I_G|$ due to availability of new leakage paths dominates over the current relaxation of Region 1. Noticeably, despite each CVS step being performed with a stress voltage that is 0.1 V higher than the previous one, $|I_G|$ starts with a value smaller than that reached at the end of the previous CVS step. This suggests that the relax phase or even the characterization, which is performed at gate voltages much lower than the stress, induces some sort of recovery on the gate dielectric, as observed also in [10].

We believe that injected electrons release hydrogen atoms (H) at the anode, generating interface traps near it. The hydrogen atoms, in turn, might move toward the cathode, generating here an interface trap. The nature of this degradation mechanism is similar to what happens in conventional Si MOSFETs with SiO_2 gate dielectrics [11]. Furthermore, hydrogen might also generate bulk oxide traps [11], which enhance the gate leakage current by trap-assisted tunneling, similarly to the mechanisms observed in thin SiO_2 oxides. One might expect a similar $|I_G|$ evolution during positive and negative stresses because both stress polarities generate interface and bulk traps. This strongly asymmetric behavior suggests that traps are generated at positions energetically much less favorable to the trap-assisted tunneling conduction when electrons are injected from the metal gate. Furthermore, the negative flatband voltage and the smaller substrate/Al_2O_3 electron barrier height enhance electron injection from the substrate during positive stress.

Region 3 starts at $V_{\mathrm{STRESS}} > 3.8$ V with the onset of a soft breakdown, and it features a very low-frequency random telegraph noise (RTN)-like evolution at current levels much higher than in Region 2 [Fig. 1(d)]. It is well known [12], [13] that stressed oxides may feature gate leakage currents, which may exhibit RTN. Still, in the literature, the RTN is observed at current values within the 1 pA–100 nA range, which are several orders of magnitude below the 100-μA range shown in Fig. 1(d). Furthermore, it has been observed that the stronger the electric field, the higher is the RTN frequency [13], due to the onset of multilevel fluctuations induced by several separated leakage paths, while the third region in Fig. 1 has timescales in the 10–100-s range and very high electric fields (exceeding 6–7 MV/cm). Consequently, we tentatively attribute these low-frequency high-current fluctuations to the formation/rupture of a filament due to the high electric field during the stress, similarly to what happens in resistive random access memories, which exploits the ability of some oxides (also Al_2O_3) [14] to reversibly switch their conductivity.

Finally, hard breakdown during positive stress occurs at $V_{\mathrm{STRESS}} \geq 4.4$ V, which, taking into account the flatband voltage and the InGaAs band bending, yields a ~8 MV/cm Al_2O_3 field, i.e., the same value reached during negative stress.

B. Stress-Induced Interface Traps and Bulk Dielectric Charge

The stress induces a threshold voltage shift and an increase of the subthreshold swing on the I_D–V_{GS} curve (not shown), due to interface trap and charge trapping in the bulk of the gate dielectric. Using the well-known subthreshold-midgap method [15], from the I_D–V_{GS} taken after each stress step, we calculated the stress-induced bulk average trapped charge density (Q_{OT}) [Fig. 2(a)], and the stress-induced interface trap density variation $\Delta \mathrm{N_{IT}}$ [Fig. 2(b)]. The trapped charge density has been calculated as if it were uniformly distributed in the bulk of the dielectric as in [16] and [17]. This is just a first-order approximation, as we expect that the charges near the interfaces are quickly neutralized by tunneling. Still, the obtained values represent the average oxide trapped charge density. As in [15], for the sake of simplicity, we assumed, both for the fresh and the stressed devices, that the interface traps are acceptors and donors, in the upper and lower half of the bandgap, respectively. In this way, at the midgap voltage (V_{mg}), the traps are neutrally charged, and the variation on V_{mg} depends only on Q_{OT}. Of course, this is just a first-order approximation, because in [18], it has been observed that the majority of the interface traps are donors-like. Still, the donor trap density is higher below the intrinsic level, and the donor traps above it can be neglected as a first approximation.

We expect the InGaAs/Al_2O_3 interface to be more H-rich than Al_2O_3/gate interface, since the substrate is treated using ammonia passivation. This could explain the different trapped charge polarity observed in Fig. 2(a). During negative stress, many H atoms are released at the H-rich substrate/dielectric interface, and some of them might be trapped in the bulk of the oxide, acting as a positive charge [19]. Conversely, during the positive stress, much less H is released, and the negative charge trapping due to the injection of electrons dominates.

Noticeably, before breakdown, we can identify two distinct growth rates [see dotted lines of Fig. 2(a)] for the positive stress, roughly corresponding to the first two regions of Fig. 1. This suggests that a second degradation mechanism is being activated at electric fields higher than 6 MV/cm, such as Fowler–Nordheim injection of electrons. Conversely, negative stress features a gradual increase of the bulk trap growth rate, and we cannot identify any region before breakdown. The obtained Q_{OT}/q before breakdown reaches the 10^{19} cm^{-3} value, which falls within the trap density range of Al_2O_3 and

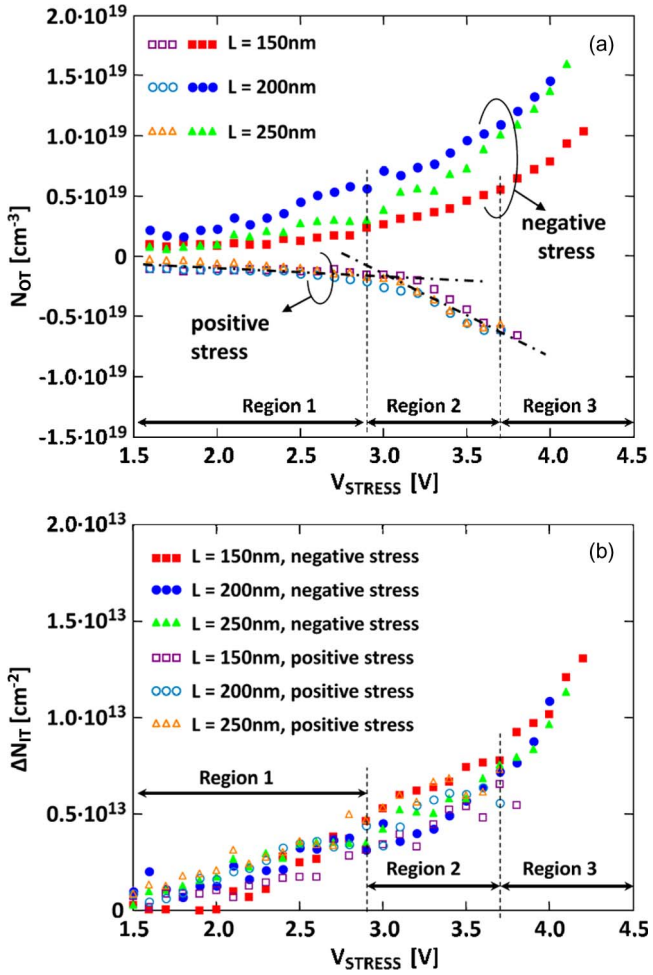

Fig. 2. (a) Trapped charge density versus stress voltage, before the soft/hard breakdown. The dash-dotted line indicates the different Q_{OT} growth rate during positive stress. (b) Variation of the interface trap density versus stress voltage for six devices with different gate lengths.

other high-k oxides [16], [17]. However, because we expect that the charge near the interface is quickly neutralized, the peak of the Q_{OT}/q profile may reach, in the center of the gate dielectric, a value larger than 10^{19} cm^{-3} but still within the $10^{19}-10^{20}$ cm^{-3} range found in many high-k oxides [16], [17].

Finally, in Fig. 2(b), we plot the estimated variation of the interface trap density. The similar trend, regardless of the gate length and stress voltage polarity, might be explained by the action of two distinct degradation mechanisms. During negative stress, electrons are injected from the metal gate toward the Al_2O_3/InGaAs interface, directly inducing interface degradation. On the contrary, during positive stress, electrons are injected toward the metal gate/Al_2O_3 interface. Here, they could release H atoms from a passivated dangling bond, which might move toward the substrate generating interface traps.

IV. Conclusion

For the first time, to our knowledge, we have showed the results of gate stress on III–V MOSFETs. Stress induces charge trapping and subthreshold slope degradation. Positive stress has three distinct stress regions with different gate current kinetics. Soft breakdowns with very low-frequency RTN are always observed prior to hard breakdown. Positive stress induces negative charge trapping in the bulk of Al_2O_3. Negative stress, instead, features only a sudden hard breakdown, at the same electric field at which it is reached during positive stress, and it induces positive charge trapping.

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