Charge Trapping in Al_2O_3/β-Ga_2O_3-Based MOS Capacitors

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***Abstract*—Trapping characteristics of MOS structures with β-Ga_2O_3 substrates and Al_2O_3 gate dielectrics are evaluated via constant-voltage stress and X-ray irradiation. Traps that affect bias-induced charging are located primarily in the Al_2O_3 dielectric layer, and are distributed broadly in time and/or energy. Stress-induced flatband voltage shifts are reduced by N_2 annealing. Trap-assisted tunneling is shown to be responsible for the observed gate leakage. Hole trapping in the Al_2O_3 dielectric layer dominates device radiation response. The relatively modest radiation-induced charge trapping observed in these devices is promising for the potential future use of Al_2O_3/β-Ga_2O_3 devices in a space environment.**

***Index Terms*—β-Ga_2O_3, Al_2O_3, MOS capacitors, oxide traps, radiation.**

I. Introduction

GALLIUM Oxide (Ga_2O_3) is quite promising for next generation power electronics due to its 4.8 eV band gap, high theoretical breakdown electric field of 8 MV/cm, and potentially high performance relative to competing technologies [1], [2]. Improvements have been reported in breakdown voltage [3]–[5], quality of crystal growth [6]–[9], device performance [10]–[15], gate dielectric, interface quality [16]–[18] and deep defect levels in Ga_2O_3 [19].

Gate stack quality is crucial to the performance, reliability, and radiation tolerance of Ga_2O_3-based MOS devices. Trapping of carriers in the gate dielectric affects critical device parameters such as gate leakage, mobility, etc. Similar to GaN [20], Ga_2O_3-based devices may also be promising for applications in high-radiation environments, including space or high-energy particle accelerators. Al_2O_3, has a relatively high dielectric constant and favorable band offset [21], [22], making it a potentially suitable gate dielectric for β-Ga_2O_3-based devices.

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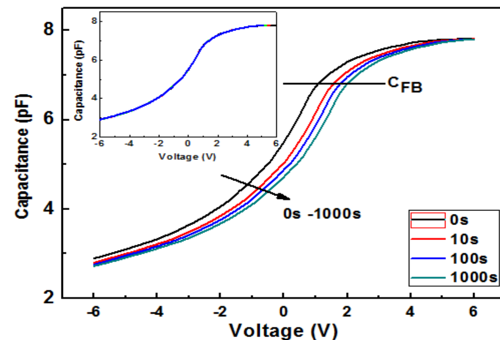

Fig. 1. High-frequency (1 MHz) *C-V* curves vs. stress time for Al_2O_3/β-Ga_2O_3 MOS capacitors biased at 4 V. The inset shows curves translated negatively by amounts equal and opposite in magnitude to measured values of ΔV_{fb}.

In this work, the responses to constant voltage stress (CVS) of β-Ga_2O_3-based MOS devices with Al_2O_3 gate dielectrics are evaluated via capacitance-voltage *C-V* and current-voltage *I-V* methods. Increasing electron-trap densities are observed for increasingly positive stress voltages, and hole traps are observed for devices irradiated with 10-keV X-rays under grounded bias conditions. Stress-induced traps are found to be located primarily in the Al_2O_3 gate dielectric layer, and are found to be distributed broadly in time and/or energy.

II. Devices and Experiments

Al_2O_3/β-Ga_2O_3 MOS capacitors were built on Sn-doped β-Ga_2O_3 (−201) substrates. Samples are cleaned with organic solvent and piranha solution before depositing 15 nm of Al_2O_3 at 250 °C by atomic layer deposition. MOS capacitors are photolithographically defined via Ti (30 nm)/Au (70 nm) deposition and lift-off. Devices were exposed to constant voltage stress at 295 K. Some devices were irradiated at 295 K with 10-keV X-rays at a dose rate of 31.5 krad(SiO_2)/min. All measurements were performed at 295 K.

III. Results and Discussion

A. Voltage Stress

Fig. 1 shows high-frequency (1 MHz) *C-V* curves as a function of stress time for Al_2O_3/β-Ga_2O_3 MOS capacitors biased at 4 V. Positive shifts are observed, consistent with net negative charge trapping in the Al_2O_3 gate dielectric layer. The inset shows curves translated negatively by amounts equal and opposite in magnitude to the measured flatband voltage

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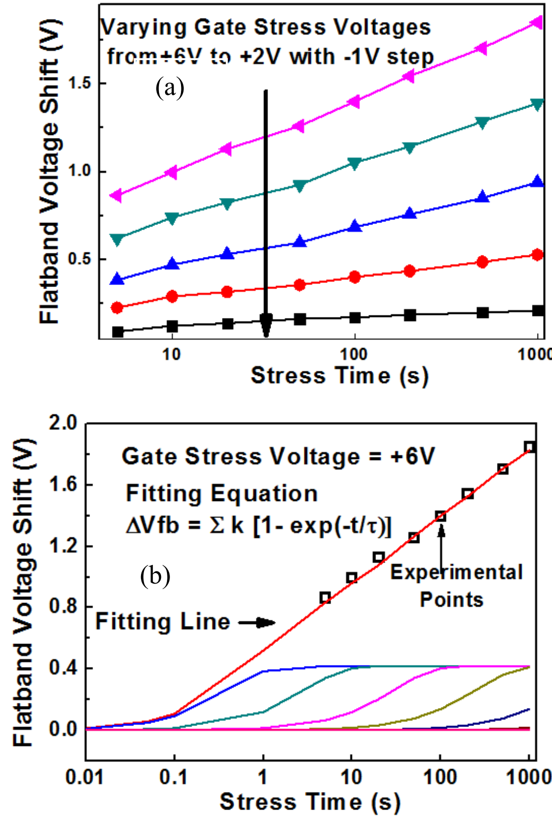

Fig. 2. (a): ΔV_{fb} vs. stress voltage and time. (b) Fitting of the ΔV_{fb} vs. stress and time curve at 6 V using a summation of exponential components.

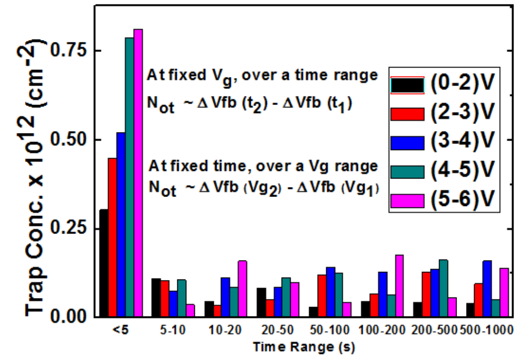

Fig. 3. Trap concentrations as a function of stressing time and voltage range.

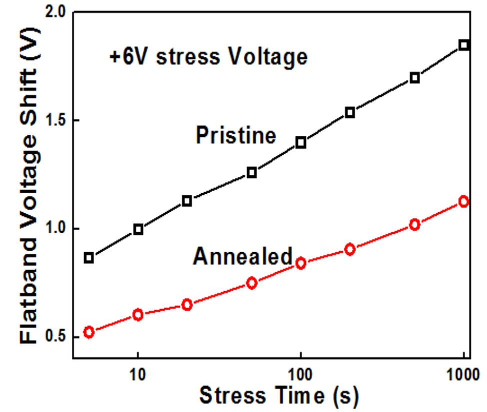

Fig. 4. ΔV_{fb} vs. stress time for as-processed (pristine) and devices annealed for 30 s in N_2 after dielectric deposition.

shifts ΔV_{fb}, showing parallel shifts. This means that neither border traps nor fast interface traps contribute significantly to the observed charge trapping [23], [24]. Hence, the observed positive shifts are primarily due to electron trapping in the Al_2O_3 dielectric layer and/or associated with deep traps at the Ga_2O_3/Al_2O_3 interface [25]–[27].

Fig. 2 shows (a) variations in ΔV_{fb} as a function of applied positive voltage during stress, and (b) extracted ΔV_{fb} line from exponential curve fits to the data, each as a function of stressing time. For all gate voltages, monotonic positive shifts of V_{fb} with stress time are observed in Fig. 2(a); increasing shifts are observed for larger stress voltages [25]–[27]. Fig. 2(b) shows that multiple exponential components with logarithmically varying time constants are required to fit these curves, suggesting that traps with a wide range of time constants participate in the bias-induced charging. These characteristics are consistent with a typically broad distribution [28], [29] of capture cross sections and tunneling distances between the β-Ga_2O_3 and traps in the Al_2O_3 gate dielectric.

Because we observe no contributions from border traps or fast interface traps in these measurements, the total-effective density of stress-induced traps (ΔN_t) with time constants between t_2 and t_1 may be estimated at a fixed bias voltage (equivalent to a fixed trap energy level) via [23]–[25], [28]:

$$\Delta N_t = \{\Delta V_{fb}(t_2) - \Delta V_{fb}(t_1)\} \times (C_{ox}/\mathrm{q}) \tag{1}$$

Similarly for these devices, for a fixed stress time t_1, ΔN_t between two different energy levels or gate stress voltages (V_2 and V_1) can be estimated via:

$$\Delta N_t = \{\Delta V_{fb}(V_2) - \Delta V_{fb}(V_1)\} \times (C_{ox}/\mathrm{q}) \tag{2}$$

Fig. 3 shows a mapping of the characteristic voltages and charging times derived from the analysis of the data of Fig. 2 via Eqs. (1) and (2). A relatively high effective trap density is observed for short stressing times, because many decades of response times are compressed into this interval. For traps within the Al_2O_3 dielectric layer that are distributed evenly in space and energy, one would expect the resulting trap distributions to be approximately linear with logarithmic time for each voltage [28]. The small deviations from precise linearity with logarithmic time in Fig. 2 are evidence that trap distributions are not precisely uniform [30].

Fig. 4 shows that annealing these Al_2O_3/β-Ga_2O_3 MOS capacitors at 500 °C for 30 s in N_2 decreases the observed ΔV_{fb} for devices stressed at 6 V. The similarity in time dependence suggests that the energy dependence of the traps has not been modified significantly, but the overall trap density has been reduced. Similar results are observed for other stress voltages.

B. Gate Leakage

Fig. 5 shows the gate leakage current density J for un-annealed devices as a function of inverse electric field. The observed linear dependence is consistent with trap-assisted tunneling (TAT), per the expression [22]:

$$J \,\alpha\, \exp\,(k \times \phi^{1.5}/E_{ox}). \tag{3}$$

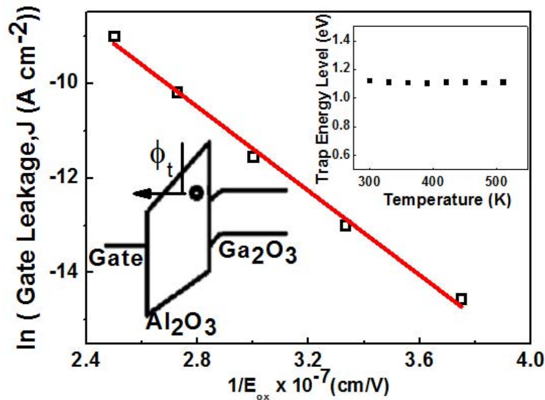

Fig. 5. The observed linear relation between ln (leakage current) vs. inverse of electric field across the oxide ($1/E_{OX}$) is consistent with trap assisted tunneling for positive gate voltage. The effective trap energy level for the rate-limiting step in the process is ~1.1 eV for temperatures from 300 K to 500 K (inset).

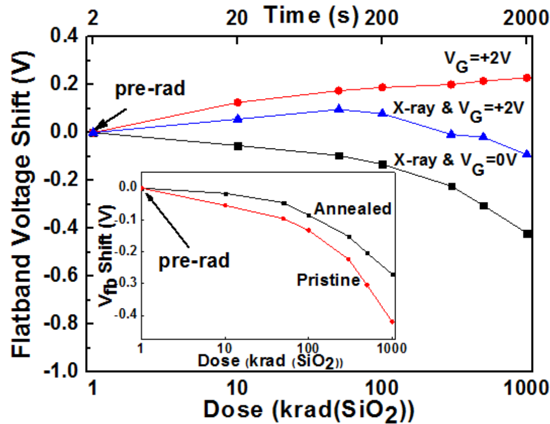

Fig. 6. Flatband voltage shift as a function of 10-keV X-ray irradiation and/or voltage stress. The inset compares irradiation results under 0 V bias for as-processed (unannealed) and N_2 annealed devices.

Here E_{ox} is the oxide electric field, ϕ is the effective energy level of the trap that is rate-limiting for the process, and k is a constant. The inset shows that, for temperatures between 300 K and 500 K, the extracted value of ϕ is ~1.1 eV below the conduction band, similar to what is found at 300 K by Hung *et al*. [22]. Vacancies in amorphous Al_2O_3 are known to have negative charge states at similar energies [31]; hence, an O vacancy center is a logical candidate for the responsible defect.

C. Radiation Effects

Fig. 6 compares the responses of devices irradiated with 10-keV X-rays and/or exposed to voltage stress at 2 V. Net negative charge trapping in the Al_2O_3 gate dielectric is observed for voltage stress. Net positive charge trapping is observed for irradiation with 0 V bias. When devices are irradiated with +2 V bias, the observed flatband voltage shifts show intermediate values. When devices are irradiated, X-rays create electron-hole pairs in the gate dielectric that are separated by the internal electric field. Holes, having lower mobility than electrons, are more likely to become trapped [32], leading to net positive charge trapping, as commonly observed for Al_2O_3 on a wide variety of semiconducting materials [33], [34].

When positive bias is applied during irradiation, radiation-induced hole trapping first reduces the magnitude of the voltage-stress induced charge trapping, and eventually becomes the dominant defect at higher doses. The inset of Fig. 6 shows that N_2 annealing reduces the net radiation-induced charge trapping. O vacancies in Al_2O_3 also have a prominent hole trapping level [31], and are therefore likely to be responsible for both radiation- and bias-induced charging effects, with the polarity of the observed shift determined by the type of carrier that is most in excess within the dielectric layer.

The radiation-induced voltage shifts for these development stage Al_2O_3/β-Ga_2O_3 MOS devices are comparable to or less than those of β-Ga_2O_3 MOSFETs with 20 nm Al_2O_3 dielectrics evaluated by Wong *et al.* [35] at similar doses. Not surprisingly, these shifts are significantly larger than those observed in industrial quality Si-based MOS capacitors with Al_2O_3 dielectrics [33], [36]. For example, Zhou *et al.* observe ~ −10 mV shifts when Si MOS capacitors with 5 nm Al_2O_3/1 nm Si oxynitride gate dielectrics are irradiated to 1 Mrad(SiO_2) at 0 V bias. However, these shifts are significantly smaller than those observed for Ge-based MOSFETs with much thinner gate dielectrics irradiated to similar doses by Ren *et al.* [34], reinforcing the comparatively higher radiation tolerance of Al_2O_3/β-Ga_2O_3 MOS devices to other developmental stage technologies with Al_2O_3 gate dielectrics. These results are promising for the potential future use of Al_2O_3/β-Ga_2O_3 devices in a space radiation environment, and indicate that further improvements in radiation tolerance should be expected as the technology matures.

IV. Conclusion

Al_2O_3/β-Ga_2O_3 MOS capacitors trap predominantly negative charge in their gate dielectrics during positive voltage stress, and predominantly positive charge during 10-keV X-ray irradiation. Oxygen vacancies in Al_2O_3 are strong candidates for the defect leading to each type of shift. The magnitude of the stress-induced charge trapping increases with increasing bias. The resulting defect distribution within the Al_2O_3 dielectric layer is distributed relatively uniformly in space and energy. However, the defect that contributes most significantly to trap-assisted tunneling is found to have an energy level that is ~ 1.1 eV below the Al_2O_3 conduction band over a wide range of temperatures. These results illustrate the strong role of oxygen vacancies in Al_2O_3 on the observed charge trapping in Al_2O_3/β-Ga_2O_3 MOS devices, and indicate that N_2 annealing may be effective in reducing the defect density and improving device reliability and radiation response.

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