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"Zero" Drain-Current Drift of Inversion-Mode NMOSFET on InP(111)A Surface

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Inversion-mode n-channel metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al_2O_3 as gate dielectric were fabricated on two crystalline surfaces: InP (100) and InP (111)A. A record high drain current of 600 μA/μm is obtained on InP (111)A surface at $V_{ds} = V_{gs} = 3$ V with a gate length of 1 μm and Al_2O_3 dielectric thickness of 8 nm. The maximum drain current is greater by a factor of 3.5 on the InP (111)A surface compared to devices fabricated on the InP (100) surface at the same bias conductions. During room temperature positive gate stress, "zero" drain current drift is observed for InP (111)A devices, in great contrast to InP(100) devices. The greater maximum drain current and the "zero" drain current drift on InP (111)A can be explained by oxide band bending caused by trap neutral level shifts and low border trap density.
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Si-based complementary-metal-oxide-semiconductor (CMOS) devices have been scaled close to their physical limit. To further increase device performance, III-V semiconductor materials have attracted lots of interest because of their higher electron mobility and velocity at low field which allow faster device operation and lower power consumption. Among these III-V materials, high-performance n-channel metal-oxide-semiconductor field-effect transistors (NMOSFETs) have been achieved on In-rich $In_xGa_{1-x}As$ with high on-state current I_{on},[1,2] and high transconductance g_m.[3,4] Nevertheless, their off-state performance is limited by oxide-semiconductor interface quality and the narrow band gap of In-rich $In_xGa_{1-x}As$. InP is a commonly used compound semiconductor with many applications in electronic, optoelectronic, and photonic devices. It has a bandgap of 1.34 eV, much larger than that of In-rich $In_xGa_{1-x}As$. Compared to GaAs, InP is widely believed to be a more forgiving material with respect to Fermi level pinning and has a higher electron saturation velocity (2.5×10^7 cm/s) as well. It would be a viable channel material for high-speed logic applications if a high-quality, thermodynamically stable high-k dielectric could be found.[5,6] The understanding of high-k/InP interfaces is also of great importance since InP is used as a transition layer for atomic-layer-deposited (ALD) high-k/InGaAs quantum well transistors which show outstanding device performance at low drain voltage.[7] Motivated by surface orientation studies of GaAs[8] and InGaAs[9], we have systematically studied NMOSFETs, metal-oxide-semiconductor capacitors (MOSCAPs), and interfacial chemistry on two different crystalline surfaces: InP (100) and (111)A (In-terminated polar surface).[10] In this paper, we report a record high drain current of 600 μA/μm and "zero" drain-current drift on InP (111)A MOSFETs at $V_{ds} = V_{gs} = 3$ V. Drain-current drift is a major issue that prevented the commercialization of InP MOSFET technology on (100) surface in 1980s.[11–15] "Zero" drain current drift and superior reliability properties of InP MOSFETs on (111)A verifies the high-quality Al_2O_3/InP (111)A interface.

Figure 1a shows the schematic cross section of the device structure of the ALD Al_2O_3/InP (100) and ALD Al_2O_3/InP (111)A NMOSFETs fabricated on semi-insulating substrates. Processing begins with removing the native oxide from InP(100) and InP(111)A wafers with dilute HCl solution and then a $(NH_4)_2S$-based pretreatment. The wafers were then transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300°C, using alternately pulsed chemical precursors of $Al(CH_3)_3$ (the Al precursor) and H_2O (the oxygen precursor) in a carrier N_2 gas flow. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 30 keV and 1×10^{14} cm^{-2} at 80 keV through the 30 nm thick Al_2O_3 layer. Implantation activation was achieved by rapid thermal annealing (RTA) at 750°C for 15 s in a N_2 ambient. An 8 nm Al_2O_3 film was then re-grown by ALD after removing the encapsulation layer via a buffered oxide etch (BOE) followed by an ammonia sulfide surface preparation. After 500°C post deposition annealing (PDA), the source and drain ohmic contacts were made by an electron beam evaporation of a combination of Ni/Ge/Au using a lift off process, followed by a RTA at 400°C for 30 s also in N_2 ambient. The gate electrodes were electron beam evaporated Ti/Au also defined using a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.40 μm to 40 μm and a gate width of 100 μm. A Keithley 4200 was used to measure the MOSFET output characteristics.

Transmission Electron Microscopy (TEM) images of Al_2O_3/InP(100) and Al_2O_3/InP(111)A stacks are shown in Figure 1b and Figure 1c, demonstrating the equal thickness of 8 nm Al_2O_3 for these two types of NMOSFETs. The flatter and smoother interface of Al_2O_3/InP(111)A is clearly visible in Figure 1c, compared to the Al_2O_3/InP(100) interface shown in Figure 1b. Previous study of $Al_2O_3/In_xGa_{1-x}As$ interfaces confirm that interface roughness is the main limiting factor for the electron mobility of surface-channel III-V MOSFETs.[16] The TEM images suggest the potential to achieve higher electron mobility and thus higher drain current on the InP(111)A surface compared to InP (100). This hypothesis is confirmed by the electrical characteristics of these devices as shown in Figure 2a. A well-behaved I_{ds}-V_{ds} characteristic of a 1 μm-gate-length inversion-mode InP NMOSFET on (111)A is shown with a maximum drain current of 600 μA/μm, *3.5 times larger* than that on (100). To our best knowledge, this is the record high drain current among all inversion-mode InP NMOSFETs reported in literature.

Typically, a slow drain current drift is always observed on InP NMOSFETs due to electron trapping in the so-called border traps (near-interface traps in the oxide).[11,14] The drain current drift behavior is studied in this letter by sampling the drain current after a gate bias step (3 V) is applied to device at t = 0. Figure 2b illustrates that "zero" drain current drift or significantly suppressed drain current drift is obtained from the InP(111)A MOSFET at $V_{gs} = 3$ V and $V_{ds} = 3$ V, in great contrast to the InP(100) MOSFET which shows a 6.9% drain current reduction in 1400 s. The data are normalized with respect to their initial current I_{ds} ($t = 0$). The observed small bumps on the InP (111)A curve might be caused by random telegraph noise (RTN) induced by the capture and emission of electrons by the

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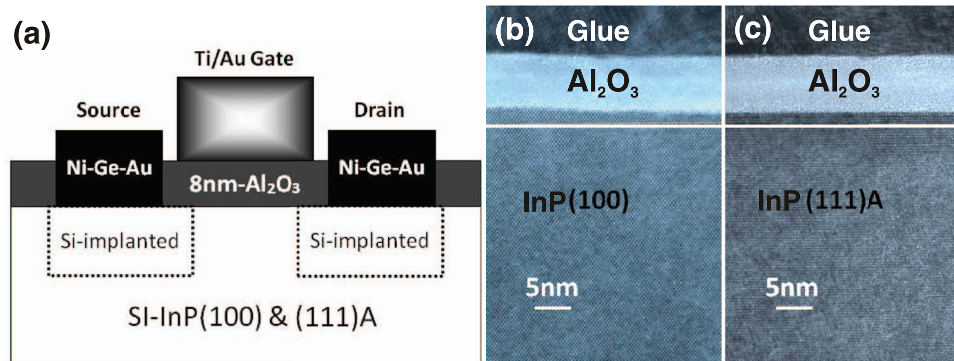

Figure 1. (a) Schematic cross-section of an inversion-mode InP NMOSFET and TEM images of 8 nm Al_2O_3 on semi-insulating (b) InP (100) and (c) InP (111)A substrates. A smoother interface for Al_2O_3/InP(111)A is observed, indicating the higher electron mobility, predicting higher drain current on ALD Al_2O_3/InP(111)A. The horizontal white lines are drawn as guide for the eye.

border traps in the gate oxide.[17] This result provides a pathway to solve the long-standing issue of drain current drift in InP MOSFETs. It also indicates that there are fewer border traps inside the oxide for the Al_2O_3/InP (111)A interface than the Al_2O_3/InP (100) interface.

Combined with the concept of trap neutral levels (TNL),[18,19] the record high drain current and the immunity to drain current drift of the (111)A surface devices can be explained qualitatively through band diagrams. As illustrated in Figure 3, the TNL at the (111)A surface shifts toward the conduction band minimum (CBM) and thus less acceptor traps are filled than in the (100) interface, similar to what observed in GaAs (111)A versus GaAs (100).[20] Detailed interface trap density mapping of InP (111)A versus (100) via the conductance method on MOSCAPs also confirms this model.[10] The (111)A interface allows the creation of more inversion charges and also has higher mobility due to the lower roughness. Thus, a larger drain current is obtained with the (111)A interface at the same gate and drain biases. Assuming both (111)A and (100) surfaces are in strong inversion with similar inversion charge density per area unit, more net negative charges from acceptor interface states would be at the (100) surface, creating a stronger electrical field in the oxide layer. Greater band bending on gate oxide would increase the possibility of electron tunneling from the inversion layer to border traps in gate oxide. This tunneling mechanism is often believed to be the main cause of drain current drift.[14,15] Furthermore, more negative charges trapped in interface states also enhance the possibility of electrons tunneling from interface traps to the border traps such as near the (100) interface.

In order to further understand the drain current drift mechanism in InP NMOSFETs, similar measurements were carried out at elevated temperatures, ranging from 25 to 175°C. The temperature dependent $I_{ds} \sim \log t$ curves measured on InP (100) and InP (111)A MOSFETs at $V_{ds} = 3$ V and $V_{gs} = 3$ V are shown in Figure 4a and Figure 4b, respectively. Figure 4a shows the strong temperature dependent drain current drift observed on an InP (100) MOSFET. At 150°C or higher, the $I_{ds} \sim \log t$ curve starts to bend down at an earlier stage than those at 100°C or lower. The dependence of drain current drift on temperature is found to be faster than linear. At 175°C, drain current decreases more than 20% after 1400 s of stress. The drain current drift is less temperature sensitive in the InP (111)A NMOSFET. Even at 175°C, less than 10% of current decrease is observed after the same stress duration. These results further verify the superior interface properties and high-quality of ALD Al_2O_3 on InP (111)A.

In order to quantitatively describe the temperature dependent I_{ds} drift in InP NMOSFETs, we use Okamura's two-trap-level model[14] to obtain the border trap energy level and density. Inside the ALD Al_2O_3 gate oxide, two border trap centers, TR-L for low energy level border traps and TR-H for high energy level border traps, are defined. Border trap state TR-L lies near but above conduction band minimum (CBM)

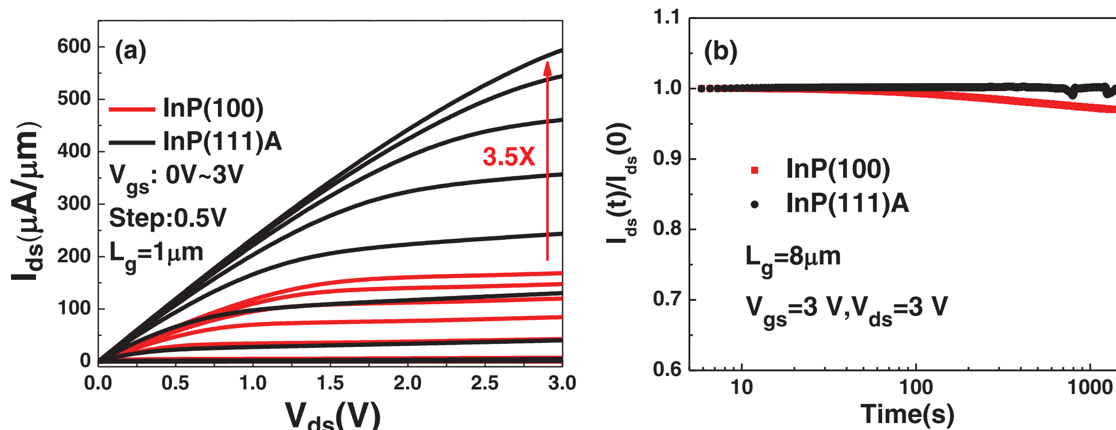

Figure 2. (a) Output characteristics ($I_{ds} \sim V_{ds}$) of InP(100) and InP(111)A NMOSFETs with a gate length of 1 μm. The drain current of InP(111)A is 600 μA/μm, which is ~3.5 times that of InP(100). (b) Comparison of drain current drift of InP(100) and InP(111)A NMOSFETs with $L_g = 8$ μm. V_{gs} and V_{ds} are 3 V, and the stress duration was 1400 s. Currents are normalized with respect to their initial current I_{ds} (t = 0). The drain current drift is significantly suppressed on InP(111)A compared to InP(100), indicating a robust Al_2O_3/InP(111)A interface. No significant current drift is observed on InP(111)A after 1400 s of stress.

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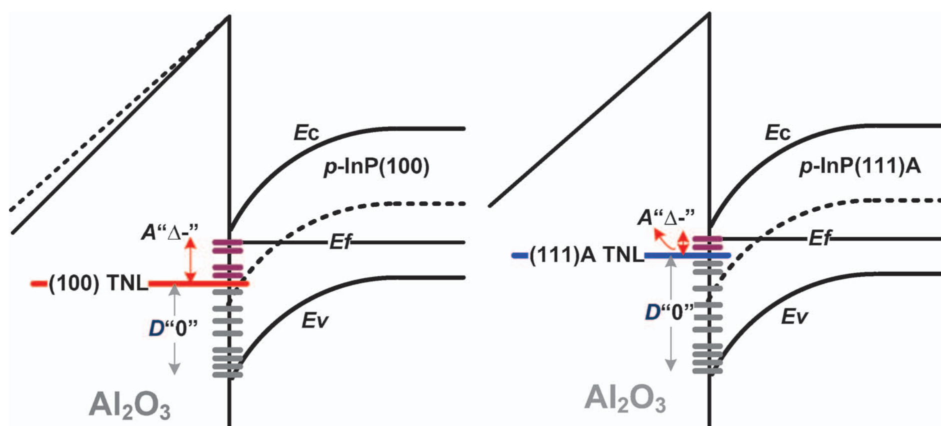

Figure 3. Band diagrams for the Al_2O_3/InP(100) (left) and (111)A (right) interfaces. In strong inversion, less net negative charge in Al_2O_3/(111)A interface results in less oxide band bending and thus less electron tunneling from interface traps to border traps.

while TR-H is at a higher energy level above CBM with the same depth in oxide as TR-L. During strong inversion of the MOSFET, a high density of electrons accumulates at the interface. In this case, these electrons can tunnel into the TR-L by phonon assistance or by direct tunneling from the inversion layer or interface states. With thermal excitations, electrons at TR-L can be excited into TR-H. Supposing that the TR-H density is much higher than that of TR-L, TR-H would play a major role for the temperature dependent current drift. With this model in mind, the drain current I_{ds} can be calculated as:

$$I_d(t)/I_d(t_0) = 1 - [N_{TR-L} + N_{TR-H} \times e^{-2\beta E_{TR-H}}] \cdot \ln(t - t_0 + 1)/(N_0 a) \qquad [1]$$

where N_{TR-L} is the trap density of TR-L, N_{TR-H} is the trap density of TR-H with an energy level E_{TR-H} above CBM, N_0 is the initial electron concentration at InP surface per unit area. The tunneling coefficient $1/a = 3.3$ Å was experimentally determined for Al_2O_3.[21] β is $1/kT$, where k is the Boltzmann constant. In equation 1, the drain current drift is exponentially dependent on temperature and E_{TR-H}. One parameter, $A = (N_{TR-L} + N_{TR-H} \cdot e^{-2\beta E_{TR-H}})/(N_0 a)$, of the function $I_d(t)/I_d(t_0) = 1 - A \cdot \ln(t - t_0 + 1)$ is used to fit the measured $I_{ds} \sim t$ curves for each temperature. These fits are plotted as empty circles in Figure 4a and Figure 4b. These excellent fits verify the validity of this two-trap level model.

Figure 5 plots the fit parameter A obtained from Figure 4 versus β = $1/kT$. Note that the generation of new trap centers due to the drain voltage is not considered in this physical model. During the fitting shown in Figure 5, we find N_{TR-L} can be set to be zero or the value of N_{TR-L} is negligible when compared to $N_{TR-H} \cdot e^{-2\beta E_{TR-H}}$. N_{TR-H} on (111)A is found to be 4.6 times smaller than N_{TR-H} on (100) with E_{TR-H} ~68 meV above the CBM. Using $N_0 = 1.0 \times 10^{13}$ cm^{-2} from Ref. 10 and $1/a = 3.3$ Å, N_{TR-H} is estimated to be 1.7×10^{20} cm^{-3} for InP (111)A, which is a reasonable number of border traps in a

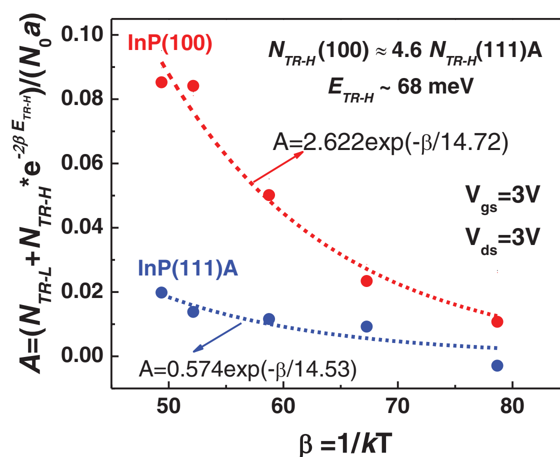

Figure 5. The parameter A, obtained from fitting the experiment curves in Figure 4, versus β = $1/kT$. By fitting A(β) curves, N_{TR-H} (111)A, N_{TR-H} (100), E_{TR-H} (111)A, and E_{TR-H} (100) are obtained experimentally.

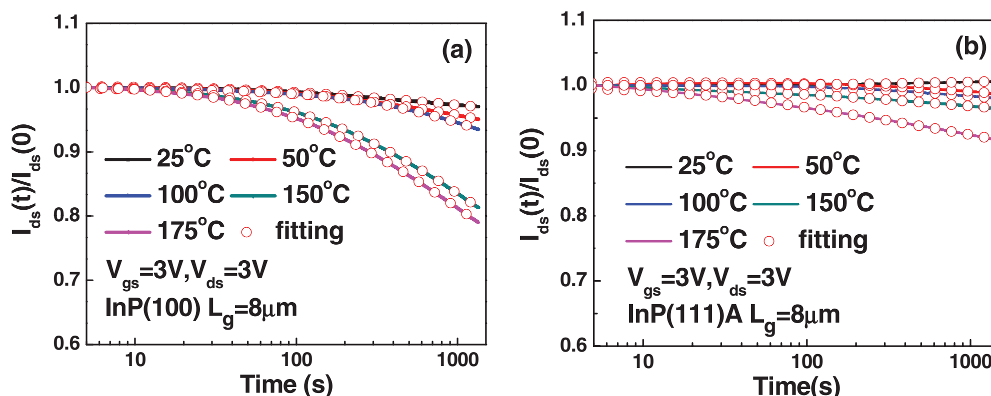

Figure 4. The temperature dependent drain current drift of (a) InP (100) and (b) InP (111)A NMOSFETs with L_g = 8 μm. The measurement was done at 25, 50, 100, 150 and 175°C, respectively. V_{gs} and V_{ds} are 3 V, Stress duration was 1400 s. Currents are normalized with respect to their initial current I_{ds} (t = 0). Using equation $I_{ds}(t)/I_{ds}(t_0) = 1 - A \cdot \ln(t - t_0 + 1)$ with the appropriate A values, the measured drain current drift (in colored lines) is fitted (empty circles) at each different temperatures. Drain current drift is less temperature sensitive on InP(111)A than InP (100).

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deposited high-k dielectric on III-V.[22–24] The 4.6 times larger N_{TR-H} on (100) explains the large drain current drift that is widely observed in InP (100) NMOSFETs.

In conclusion, inversion-mode InP NMOSFETs with ALD Al_2O_3 gate dielectric were fabricated on both (100) and (111)A semi-insulating substrates. Record high drain current of 600 μA/μm with "zero" drain current drift at room temperature is achieved on the (111)A surface. The border trap energy level and concentration in ALD Al_2O_3 on the InP (111)A surface are determined to be ~68 meV above the CBM and 1.7×10^{20} cm^{-3}, respectively. The much lower border trap density on (111)A interface explains the immunity of drain current drift, compared to (100) interface.

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