High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO as gate dielectrics

Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye

School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906, U.S.A.
Tel: 1-765-494-7611, Fax: 1-765-496-7443, Email: yep@purdue.edu

Abstract

High-performance inversion-type enhancement-mod n-channel $In_{0.53}Ga_{0.47}As$ MOSFETs with atomic layer deposited (ALD) Al_2O_3, HfO_2, and HfAlO as gate dielectrics are demonstrated. The ALD process on III-V compound semiconductors enables the formation of high-quality gate oxides and unpinning of Fermi level on III-V in general. A 0.5-μm gate-length MOSFET with an Al_2O_3 gate oxide thickness of 8 nm shows a maximum drain current of 430 mA/mm and a transconductance of 160 mA/mm at drain voltage of 2 V. The transconductance is improved to 180 mA/mm by implementing HfO_2 or HfAlO as gate dielectrics with the same oxide thickness. The peak effective mobility is ~1200 cm^2/Vs from dc measurement, ~ 4000 cm^2/Vs after interface trap correction for $HfO_2/In_{0.53}Ga_{0.47}As$ NMOSFETs.

Introduction

After implementation of ALD high-k gate dielectrics and metal gates in high-volume manufacturing for upcoming CMOS integrated circuits by Intel and IBM, the hope is growing that the ALD high-k dielectrics developed for Si may also be applicable to compound semiconductors. Although *in-situ* MBE grown $Ga_2O_3(Gd_2O_3)$ shows promising results as a good gate dielectric on III-V compound semiconductors [1-2], the current research is mainly focused on *ex-situ* ALD or PVD Al_2O_3 and HfO_2 due to its potential manufacturability [3-6]. In this paper, we report, for the first time, a complete study of submicron *inversion-type* E-mode n-channel MOSFETs on $In_{0.53}Ga_{0.47}As$ using ALD Al_2O_3, HfO_2 and HfAlO as high-k gate dielectrics with more than 430 mA/mm maximum drain current and 180 mS/mm transconductance. The device performance has a significant leap with *4000 times increase* of the maximum drain current, compared to our previous results on $In_{0.2}Ga_{0.8}As$ MOSFETs [7]. We ascribe this improvement to the fact that $In_{0.53}Ga_{0.47}As$ is the more forgiving material with respect to Fermi level pinning and has a narrower bandgap easier to realize inversion. The maximum drain current is also increased by 16% from the previous work on $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSFET by reducing process temperature slightly [8].

Experiments

Fig. 1 and Table 1 show the schematic cross section of the device structure and the device fabrication flow. ALD high-k gate dielectrics, such as Al_2O_3, HfO_2 and HfAlO [9], were grown *directly* on MBE InGaAs surfaces. NH_4OH and $(NH_4)_2S$ were used as the pretreatment before ALD because they are hydrophilic and able to passivate InGaAs surfaces [10], as demonstrated by the contact experiment in Fig. 2. A 500 nm p-doped 4×10^{17} cm^{-3} buffer layer, a 300 nm p-doped 2×10^{16} cm^{-3}, or 1×10^{17} cm^{-3}, or 2×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$ channel layer were sequentially grown by MBE on a 2-inch InP p+ substrate. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300°C as an encapsulation layer. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 30 keV and 1×10^{14} cm^{-2} at 80 keV through the 30 nm thick Al_2O_3 layer. Implantation activation was achieved by rapid thermal anneal (RTA) at 750-800 °C for 10 s in a nitrogen ambient. An 8 nm Al_2O_3 or HfO_2, or HfAlO film was regrown by ALD after removing the encapsulation layer by BOE solution and ammonia sulfide surface preparation. After 400-600 °C PDA process, the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA process at 400 °C for 30 s also in a N_2 ambient. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.50 μm to 40 μm and a gate width of 100 μm. An HP4284 LCR meter was used for the capacitance measurement and a Keithley 4200 was used for MOSFET output characteristics.

Results and discussion

A well-behaved I-V characteristic of a 0.5 μm-gate-length inversion-type $In_{0.53}Ga_{0.47}As$ NMOSFET is demonstrated in Fig. 3 with the maximum drain current of 430 mA/mm and transconductance of 160 mS/mm. The gate leakage current is less than 10^{-4} A/cm^2 at 3 V gate bias. The contact resistance R_C of 0.23 Ω·mm is measured by TLM. After subtracting the contact resistance, the resulting intrinsic maximum drain current and transconductance are 490 mA/mm and 175 mS/mm, respectively, as illustrated in Fig. 4. Fig. 5 is the scaling characteristics of maximum drain current versus different gate length. The drain current or transconductance is linearly and inversely proportional to the gate length, as expected, and starts to saturate at 0.75 μm. Maximum drain current of 1A/mm can be achieved at the gate length of 0.15

μm without considering short channel effect, parasitic effect and velocity saturation. It's significantly different from GaAs HEMTs, which the saturation occurs at a few-μm-gate-length. The effect of post deposition anneal (PDA) process is also studied as shown in Fig. 6. Device performance is degraded under 600ºC PDA, compared to that under 500ºC PDA in regards of drain current and transconductance. It is due to the lower thermal budget for In-rich InGaAs material, compared to GaAs. Subthreshold slope and drain induced barrier lower (DIBL) can be both derived from the logarithm scale of transfer characteristics in Fig. 7. For the same device under test (DUT), the subthreshold slope (S.S.) is ~ 240 mV/dec and DIBL is ~ 350 mV/V. Fig. 8 shows the temperature dependent measurement on I_{ds} versus V_{gs}. The increase of off-current indicates that DIBL is the limitation for I_{on}/I_{off} ratio instead of impact ionization. ON/OFF ratio of ~ 4×10^3 is achieved at V_{gs}=5 V (ON) and V_{gs}=0 V (OFF), and V_{ds}=1.0 V on these devices. The temperature dependence of S.S. and I_{off} is also summarized in Fig. 9. Fig. 10 is the study of device electrical characteristics with different channel doping concentration. It is summarized as I_{on}, I_{off}, and G_m of the devices with three different doping concentrations. It is clear that the channel doping can significantly affect the source and drain junction with the channel and the inversion conduction; therefore it can affect the final device performance. The choice of doping concentration of p-channel is also crucial to the device output characteristics. The threshold voltage is also shifted to more positive with increase of p concentration as in Si case.

Fig. 11 shows the *C-V* characteristics of Al_2O_3 on InGaAs with NH_4OH or $(NH_4)_2S$ treatment at room temperature in dark. Clear transitions from accumulation to depletion for HF *C-V* and the inversion features for LF *C-V* below 1KHz are observed. The mid-gap D_{it} is estimated to be around 1.4×10^{12} /cm^2-eV on sulfur treated device by HF - LF method. Hysterisis of both *C-V* curves is about 100 mV in Al_2O_3 (not shown). The inversion features of low-frequency *C-V* from 1 kHz down to 300 Hz indicate that the conventional Fermi-level pinning phenomenon on III-V is overcome in this ALD high-k/$In_{0.53}Ga_{0.47}As$ interface. Small difference in D_{it} exhibits at interfaces using different surface pretreatment before ALD.

Different high-k dielectrics, such as HfO_2 and HfAlO nanolaminates, have also been studied. Fig. 12 and Fig. 13 show the well-behaved *I-V* characteristics of the InGaAs MOSFETs with ALD HfO_2 and HfAlO as gate dielectrics. The G_m increases to 180 mS/mm by applying HfO_2. It doesn't scale well with high-k value and oxide thickness due to the higher D_{it} or C_{it} at $HfO_2/In_{0.53}Ga_{0.47}As$ interface, compared to $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. Fig. 14 summarizes the device performance with different high-k gate dielectrics at the same 2×10^{17} cm^{-3} channel doping concentration. The higher k leads to higher vertical electric field in oxide and larger inversion current at the same gate bias. The advantage of implementation of high-k dielectrics on III-V MOSFETs is obvious if $HfO_2/In_{0.53}Ga_{0.47}As$ interface or HfAlO/ $In_{0.53}Ga_{0.47}As$ interface can be further improved. The "split-*CV*" and I_d-V_g method is used for obtaining the effective mobility μ_{eff}. Fig. 15 shows the μ_{eff} comparison of different channel doping concentrations. The effective mobility is corrected by overestimated inversion charge by the dc split C-V due to the interface traps. [11] It is obvious that p-channel doping concentration and PDA process affect the final maximum drain current and transconductance, thus affect effective mobility of inversion electrons. Fig. 16 summarizes effective mobility μ_{eff} obtained from HfO_2/InGaAs MOSFETs with and without correction. The effective mobility μ_{eff} has a peak value of ~1200 cm^2/Vs around a normal electric field E_{eff} of 0.25 MV/cm and increase to ~4000 cm^2/Vs after the interface trap correction.

Conclusion

We have demonstrated high-performance inversion-type E-mode $In_{0.53}Ga_{0.47}As$ MOSFETs using ALD high-k gate dielectrics such as ALD Al_2O_3, HfO_2 and HfAlO with maximum inversion current as high as 430 mA/mm and transconductance of 180 mS/mm. These results suggest $In_{0.53}Ga_{0.47}As$ could be an ideal channel material which is easy to integrate with high-k dielectrics and has higher electron effective mobility and wide enough bandgap for low drain voltage ultimate CMOS applications.

Acknowledgement

The authors would like to thank M. Lundstrom, J. Woodall, J. A. Cooper, M. A. Alam, J. del Alamo, R. M. Wallace, G. D. Wilk, A. Kummmel, J. C. M. Hwang for the valuable discussions. The work is supported in part by NSF and the MARCO MSD Focus Center.

References

[1] F. Ren et al., *IEEE Electron Device Lett.,* vol. 19, pp. 309-311, Aug. 1998.
[2] K. Rajagopalan et al., *IEEE Electron Device Lett.,* vol. 27, 959-961, 2006.
[3] P.D. Ye et al., *IEEE Electron Device Lett.,* vol. 24, pp. 211-213, Apr.2003.
[4] I. Ok et al., in *IEDM Tech. Dig*., pp. 829-832, Dec. 2006.
[5] F. Gao et al., in *IEDM Tech. Dig*., pp. 833-836, Dec. 2006.
[6] Y. Sun et al., *IEEE Electron Device Lett.,* vol. 28, pp. 473-475, June 2007.
[7] Y. Xuan et al., *Appl. Phys. Lett.,* vol. 88, pp. 263518-520, June 2006.
[8] Y. Xuan et al., *IEEE Electron Device Lett.,* to be published.
[9] T. Yang et al., *Appl. Phys. Lett.*,to be published.
[10] Y. Xuan et al., *IEEE Trans. Electron Dev.*, vol. 54, pp. 1811-1817, 2007.
[11] W.J. Zhu et al., *IEEE Trans. Electron Devices,* vol. 51**,** 98-105, Jan. 2004.

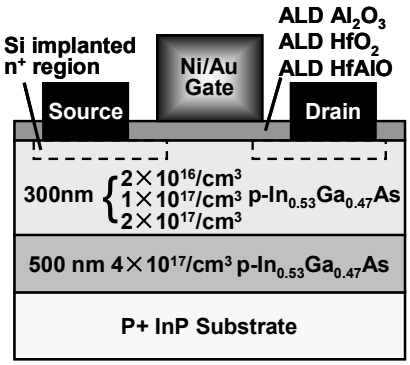

Fig. 1 Schematic view of an inversion type E-mode n-channel InGaAs (2×10^{16}, 1×10^{17}, or $2\times10^{17}/cm^3$) MOSFET with ALD Al_2O_3, HfO_2, or HfAlO as gate dielectrics.

1) NH_4OH surface treatment and ALD Al_2O_3 30nm deposition
2) S/D patterning and Si implantation ($30KeV/1\times10^{14}/cm^2$ & $80KeV/1\times10^{14}/cm^2$)
3) S/D activation using RTA (750-800°C 10s in N_2)
4) $(NH_4)_2S$ or NH_4OH surface treatment and ALD re-growth: Al_2O_3, HfO_2 and HfAlO
5) PDA: 400-600°C 30s in N_2
6) S/D contact patterning and Au/Ge/Ni ohmic metal evaporation and 400°C anneal
7) Gate patterning and Ni/Au evaporation

Table 1 Fabrication process flow for E-mode high-k/InGaAs MOSFETs. 30nm Al_2O_3 acts as an encapsulation layer to protect the surface during implantation and the following activation. All the high-k gate oxides were re-grown by ALD and followed by a PDA step.

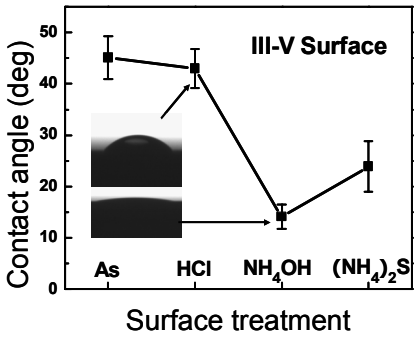

Fig. 2 Contact angle measurement of III-V surfaces after different surface treatments. NH_4OH and $(NH_4)_2S$ pretreated surfaces are hydrophilic with small contact angles.

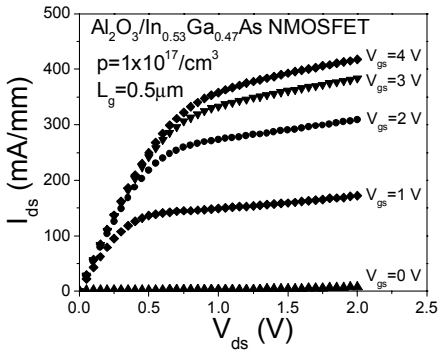

Fig. 3 Drain current versus drain bias as a function of gate bias for an Al_2O_3 InGaAs MOSFETwith the channel doping concentration of $1\times10^{17}/cm^3$. This device was $(NH_4)_2S$ passivated before ALD. The maximum current exceeds 430 mA/mm.

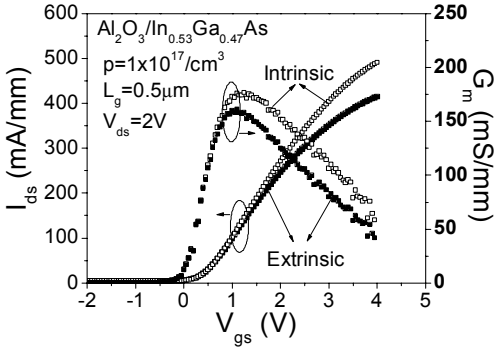

Fig. 4 Extrinsic and intrinsic drain currents and transconductances versus gate bias. The maximum extrinsic and intrinsic G_m is about 160 mS/mm and 175 mS/mm, respectively. Threshold voltage (V_T) of 0.8V is obtained in the linear region (V_{ds}=0.05V).

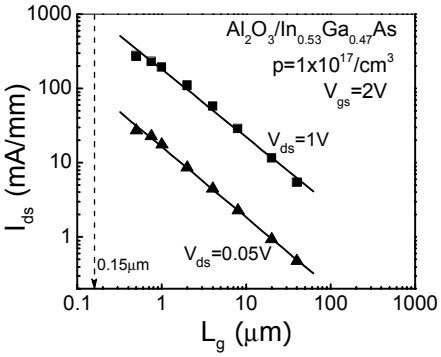

Fig. 5 Scaling characteristics of drain current versus gate length of ALD Al_2O_3/InGaAs MOSFET in logarithm scale at gate bias of 2V and drain bias of 0.05V (mobility region) and 1V (saturation region), respectively. The dashed line is for 0.15 μm gate length. Note that gate bias is 2V and the drain current is about two third of maximum drain current.

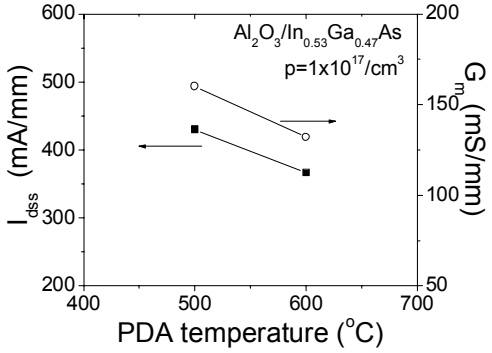

Fig. 6 Saturation drain current and maximum transconductance dependence on PDA temperature. 500ºC PDA is more favorable than 600ºC PDA due to In-rich InGaAs channels.

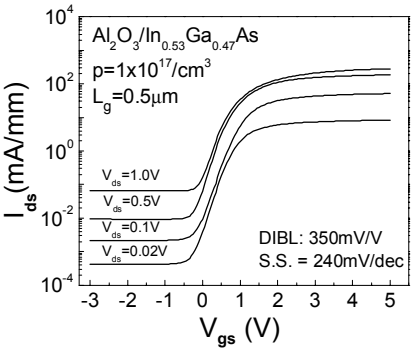

Fig. 7 Drain currents versus gate biases as a function of drain voltages measured at room temperature. The DIBL and subthreshold slope of the Al_2O_3/InGaAs MOSFET is determined by this plot.

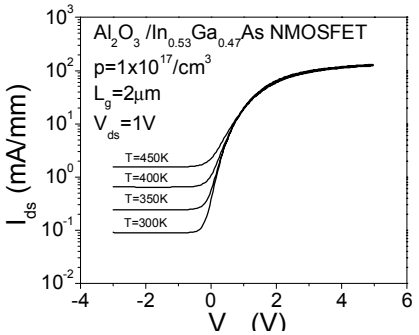

Fig. 8 Drain currents versus gate biases as a function of measurement temperatures at V_{ds}=1V. I_{on}/I_{off} ratio is mainly limited by DIBL of narrow bandgap semiconductors.

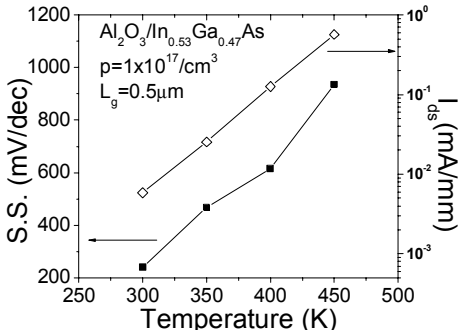

Fig. 9 Temperature dependence of S.S. and off-current (at V_{gs}=0V and V_{ds}=0.05V) of an ALD Al_2O_3/InGaAs MOSFET. The increase of off-current with temperature indicates the I_{on}/I_{off} ratio is determined by DIBL effect.

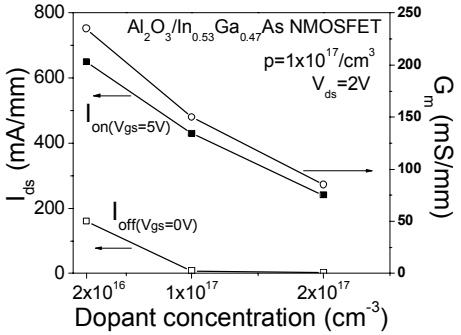

Fig. 10 Comparison of the drain currents at on and off states and maximum trans-conductance with different InGaAs channel doping concentrations. Higher channel doping concentration has better off-current but smaller on-current and transconductance.

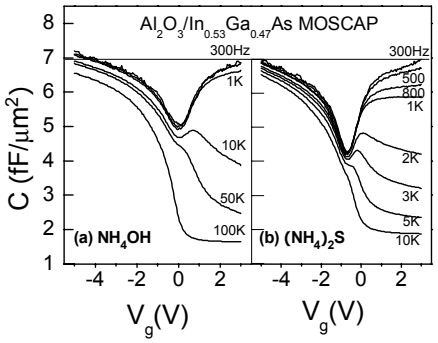

Fig. 11 Capacitance-Voltage characteristics measured from 8nm ALD Al_2O_3/InGaAs MOS capacitors with different surface passivations: (a) NH_4OH and (b) $(NH_4)_2S$.

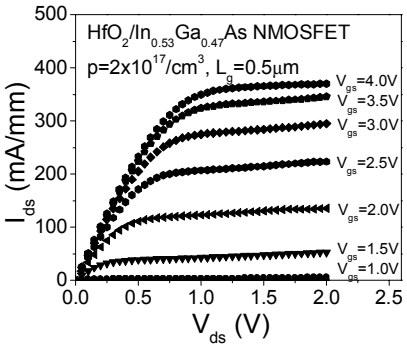

Fig. 12 Drain current versus drain bias as a function of gate bias of a HfO_2/InGaAs MOSFET. ALD HfO_2 was directly deposited on InGaAs after $(NH_4)_2S$ passivation. The maximum current exceeds 370 mA/mm with capacitance equivalent thickness (CET) of 3.6 nm.

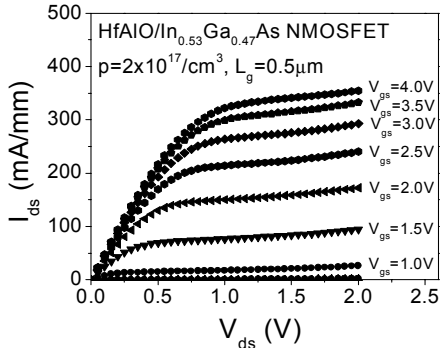

Fig. 13 Drain current versus drain bias as a function of gate bias of a HfAlO/InGaAs MOSFET. ALD HfAlO was directly deposited on InGaAs after $(NH_4)_2S$ passivation. The maximum current exceeds 355 mA/mm with capacitance equivalent thickness of 4.0 nm.

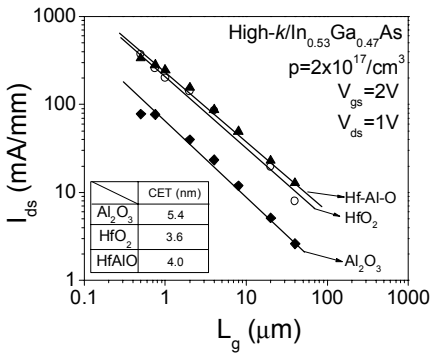

Fig.14 Comparison of scaling behavior of drain current versus gate length with different high-k dielectrics as gate oxides. With lower CET, HfO_2 and HfAlO has better performance over Al_2O_3 at the same gate bias.

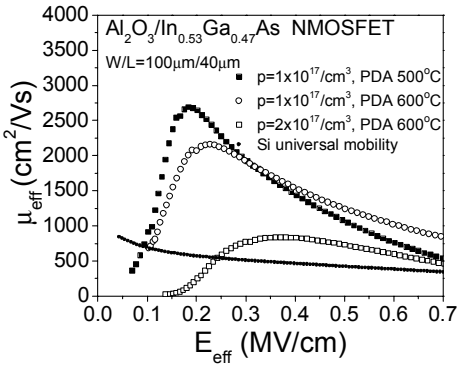

Fig.15 Effective mobility versus effective electric field derived from split-*CV* and linear region transfer characteristics as a function of different channel doping and different PDA temperature. The mobility curves are corrected by the method introduced by Ref.[11].

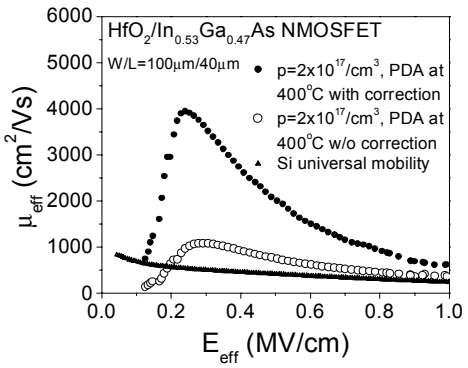

Fig.16 Uncorrected and corrected effective mobility versus effective electric field derived from split-*CV* and linear region transfer characteristics of InGaAs MOSFETs with ALD HfO_2 as gate dielectric.