High-performance Surface Channel In-rich $In_{0.75}Ga_{0.25}As$ MOSFETs with ALD High-*k* as Gate Dielectric

Y. Xuan, T. Shen[1)], M. Xu, Y.Q. Wu, and P. D. Ye*[)]

School of Electrical and Computer Engineering, Department of Physics[1)], Purdue University, West Lafayette, IN 47906
*[)] Tel: 1-765-494-7611, Fax: 1-765-496-7443, Email: yep@purdue.edu

Abstract

High-performance *inversion-type* enhancement-mode n-channel MOSFETs on In-rich $\mathbf{In_{0.75}Ga_{0.25}As}$ using ALD Al_2O_3 as high-*k* gate dielectrics are demonstrated. The maximum drain current, peak transconductance, and the effective electron velocity of 1.0 A/mm, 0.43 S/mm and 1.0×10^7 cm/s at drain voltage of 2.0 V are achieved at 0.75-µm gate length devices. The device performance of In-rich InGaAs NMOSFETs with different indium contents, $\mathbf{In_{0.53}Ga_{0.47}As}$, $\mathbf{In_{0.65}Ga_{0.35}As}$ and $\mathbf{In_{0.75}Ga_{0.25}As}$, are systematically studied.

Introduction

Although *in-situ* MBE grown $Ga_2O_3(Gd_2O_3)$ shows promising results as a good gate dielectric on III-V compound semiconductors [1-4], the current research is mainly focused on *ex-situ* atomic layer deposited (ALD) Al_2O_3 and HfO_2 due to its potential manufacturability [5-16]. In this paper, we report, for the first time, a complete study of *inversion-type* enhancement-mode (E-mode) n-channel MOSFETs on In-rich $In_{0.75}Ga_{0.25}As$ using ALD Al_2O_3 as high-*k* gate dielectrics with the gate length down to 0.75-µm. The maximum drain current (I_{DMAX}), peak transconductance (G_m), and the effective electron velocity of 1.0 A/mm, 0.43 S/mm and 1.0×10^7 cm/s at drain voltage (V_{DS}) of 2.0 V are achieved at 0.75-µm gate length devices instead of 0.4-µm devices reported before [10]. The device performance of In-rich InGaAs MOSFETs with three different indium contents, $\mathbf{In_{0.53}Ga_{0.47}As}$, $\mathbf{In_{0.65}Ga_{0.35}As}$ and $\mathbf{In_{0.75}Ga_{0.25}As}$, are systematically studied. The results indicate that In-rich narrow band gap InGaAs could be ideal as the alternative n-channel material, which has no Fermi level pinning with high-*k* dielectrics and has a high electron mobility and velocity. Its smaller bandgap is also well positioned for low voltage supply and high-speed low-power logic applications.

Experimental

Fig. 1 shows the schematic cross section of the device structure. The channel is 15~20 nm thick $1\times10^{17}/cm^3$ p-type doped $In_{0.53}Ga_{0.47}As$ or $In_{0.65}Ga_{0.35}As$ or $In_{0.75}Ga_{0.25}As$ channel layer, which is MBE epitaxially grown on $In_{0.53}Ga_{0.47}As$/InP substrate. An 8~10 nm thick ALD Al_2O_3 is used as gate dielectric while Ni or Al is used as gate electrodes. Table 1 shows the device fabrication flow. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C as an encapsulation layer. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} /cm^2 at 30 keV and 1×10^{14} /cm^2 at 80 keV through the 30 nm thick Al_2O_3 layer. Implantation activation was achieved by rapid thermal annealing (RTA) at 700-800 °C for 10 s in a N_2 ambient. An 8~10 nm Al_2O_3 film was then re-grown by ALD after removing the encapsulation layer by BOE etching and ammonia sulfide surface preparation. After 400-600 °C Post Deposition Anealing (PDA), the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA at 400 °C for 30 s also in N_2 ambient. The gate electrode was defined by electron beam evaporation of Ni/Au or Al/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.40 µm to 40 µm and a gate width of 100 µm. An HP4284 LCR meter was used for the capacitance measurement and a Keithley 4200 was used for MOSFETs output characteristics.

Results and discussion

Well-behaved I-V characteristic of 0.75-µm gate length inversion-type E-mode $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ NMOSFETs are demonstrated in Fig. 2-4 with the I_{DMAX} of 0.3 A/mm, 0.86 A/mm and 1.0 A/mm, respectively. The gate leakage current (I_G) is less than 10^{-4} A/cm^2 at 4.0 V gate bias (V_G) for all devices. The extrinsic G_m, the intrinsic G_m, and the threshold voltage V_T for $In_{0.75}Ga_{0.25}As$ NMOSFETs are 0.43 S/mm, 0.52 S/mm, and 0.5 V respectively, as illustrated in Fig. 5. Fig. 6 shows the source current (I_S) versus V_G at different V_{DS}. The I_{on}/I_{off} ratio is 10^6 at V_{DS}=1.0 V, and the subthreshold swing (S.S) is around 190 mV/dec. The low I_{on}/I_{off} ratio reported previously [10] is mainly due to the large drain junction leakage current instead of the intrinsic limitation from the narrow bandgap InGaAs channel. It could be eliminated by more sophisticated junction engineering.

Fig. 7 is the I_{DMAX} and G_m versus different indium content InGaAs MOSFETs with 0.75-µm gate length. The I_{DMAX} and G_m increase with increasing indium content in InGaAs due to

the increase of mobility and saturation velocity and reduced contact resistance. Fig. 8 is the scaling characteristics of I_{DMAX} and G_m versus different gate length for different indium content devices. $In_{0.75}Ga_{0.25}As$ MOSFETs show the best device performance due to its narrowest bandgap of 0.52 eV, which is the easiest to realize inversion, and its largest mobility and saturation velocity. The I_D of $In_{0.75}Ga_{0.25}As$ MOSFETs at gate length greater than 10 μm is a little bit smaller than that of $In_{0.65}Ga_{0.35}As$. It could be related to more defects in long gate length devices due to larger lattice mismatch between $In_{0.75}Ga_{0.25}As$ and $In_{0.53}Ga_{0.47}As$. The intrinsic properties of $In_{0.75}Ga_{0.25}As$ are still believed to be superior to those of $In_{0.65}Ga_{0.35}As$. Electron velocity is also studied for all devices with different indium content as in Fig. 9. The effective electron velocity reached $1.0x10^7$ cm/s for $In_{0.65}Ga_{0.35}As$ at 0.4-μm gate length and for $In_{0.75}Ga_{0.25}As$ at 0.75-μm gate length. The effective electron velocity could be significantly above $1.0x10^7$ cm/s (also the value for Si MOSFET) at deep submicron gate length.

Fig.10 is the weak inversion characteristics of $In_{0.53}$-$Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ devices. The drain induced barrier lowering (DIBL) is less than 20 mV/V and the S.S. is around 150-250 mV/decade with long gate-length. The roll up of the DIBL and S.S. at gate length less than 1-μm is because of short channel effect and non-optimized implanted source and drain. This statement is further confirmed by the new work on deep submicron gate length $In_{0.75}Ga_{0.25}As$ MOSFETs with full electron beam lithography process. [17].

Fig. 11 shows the I_D, I_S, I_G and substrate current (I_{SUB}) versus V_{GS} for $In_{0.75}Ga_{0.25}As$ MOSFETs at V_{DS}=2.0 V. It is clear that I_{SUB} determines the leakage floor which constrains I_D at $V_{GS} < 0$. There is no Fermi level pinning at V_{GS} less than 0 V since the gate still controls the channel well as I_S can still be modulated by four orders of magnitude by the gate bias. The analysis on I_S can more accurately reflects the intrinsic properties of devices by avoiding the substrate current. I_{SUB} is mainly from the reverse biased drain-substrate p-n junction. Since III-V semiconductors include elements from relatively volatile V group, activation and/or annealing at high temperature leads to more bulk defects hence produce more junction leakage. In order to reduce junction leakage, development of low temperature activation technique such as spike RTA or laser annealing is critical. The reverse current increases as the activation temperature increases as shown in Fig. 12. The $In_{0.53}Ga_{0.47}As$ MOSFETs show larger reverse current than GaAs MOSFETs due to its narrower bandgap.

Fig.13 shows the quasistatic *C-V* and 100 KHz *C-V* of $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOS capacitor measured at room temperature in dark. Interfacial trap density (D_{it}) extracted from HF-LF method and Terman method are shown in Fig. 14. The D_{it} minimum is $8x10^{11}/cm^2$-eV at 0.33 eV from Terman method. Fig. 15 shows the I_S and band bending versus V_{GS} for $Al_2O_3/In_{0.75}Ga_{0.25}As$ NMOSFETs. By comparing ideal I_S and experimental I_S curves, band bending is extracted to be ranging from 0.22eV to 0.65eV, almost covers the whole bandgap, showing no sign of Fermi level pinning. Similar large band bendings are also observed for both $In_{0.53}Ga_{0.47}As$ and $In_{0.65}Ga_{0.35}As$ NMOSFETs. Fig. 16 shows the *C-V* characteristics of Al_2O_3 on $In_{0.75}Ga_{0.25}As$ with Al and Ni as gate metal. The Al gated device shows smaller C_{ox} mainly due to the oxidation of Al during Al evaporation, which severely degrades the oxide capacitance. The shift of flat-band voltage (~1.0 eV) is the difference of work function of Al and Ni, which further confirms no Fermi level pinning in InGaAs.

Conclusion

We have demonstrated high-performance inversion-type E-mode $In_{0.75}Ga_{0.25}As$ MOSFETs using ALD Al_2O_3 as gate dielectrics with maximum inversion current as high as 1.0 A/mm and transconductance of 0.43 S/mm at 0.75-μm gate length. $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ MOSFETs are systematically studied indicating higher device performance with higher indium content. These results suggest indium-riched InGaAs could be an ideal channel material to integrate with high-*k* dielectrics for ultimate CMOS applications.

Acknowledgement

The authors would like to thank M.S. Lundstrom, J.M. Woodall, D.A. Antoniadis, M.A. Alam, J.A. del Alamo, and J.C.M. Hwang for the valuable discussions. The work is supported in part by NSF and the SRC FCRP MSD Focus Center.

References

[1] M. Hong *et al.*, *J. Vac. Sci. Tech.* B., vol. 14, 2297-2300, 1996.
[2] M. Passlack, *et al., IEEE Trans. Electron Devices,* vol. 44, 214-225, 1997.
[3] F. Ren *et al.*, *IEEE Electron Device Lett.,* vol. 19, 309-311, 1998.
[4] T.D. Lin *et al.*, *66th Device Research Conference,* vol. 27, 39-40, 2008.
[5] P.D. Ye *et al., IEEE Electron Device Lett.*, vol. 24, 209-211, 2003.
[6] P.D. Ye *et al.*, *Appl. Phys. Lett.,* vol. 83, 180-182, 2003.
[7] P.D. Ye *et al., Appl. Phys. Lett.,* vol. 84, 434-436, 2004.
[8] Y. Xuan *et al.*, *IEEE Electron Device Lett.,* vol. 28, 935-938, 2007.
[9] Y. Xuan *et al.*, *in IEDM Tech. Dig.,* 637-640, Dec. 2007.
[10] Y. Xuan *et al.*, *IEEE Electron Device Lett.,* vol. 29, 294-296, 2008.
[11] Y.N. Sun *et al.*, *IEEE Electron Device Lett.,* vol. 28, 473-475, 2007.
[12] H. Zhao *et al.*, *Appl. Phys. Lett.,* vol. 92, 253506, 2008.
[13] D. Shahrjerdi *et al.*, *IEEE Electron Device Lett.,* vol. 29, 557-560, 2008.
[14] S.Koveshnikov *et al.*, *Appl. Phys. Lett.,* vol. 93, 012903, 2008.
[15] J.Q. Lin *et al.*, *IEEE Electron Device Lett.,* vol. 29, 977-980, 2008.
[16] H.C. Chin *et al.*, *IEEE Electron Device Lett.,* vol. 29, 553-556, 2008.
[17] Y.Q. Wu *et al.*, submitted to *IEEE Electron Device Lett.*

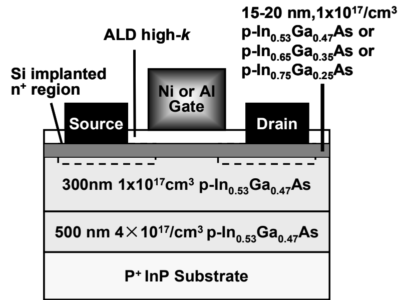

Fig. 1 Schematic view of surface channel $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$, and $In_{0.75}Ga_{0.25}As$ NMOSFETs with ALD high-*k* Al_2O_3 as gate dielectrics.

1) NH_4OH surface pretreatment
2) ALD Al_2O_3 30nm as an encapsulation layer
2) S/D patterning and Si implantation (30KeV/1E14 & 80KeV/1E14)
3) S/D activation using RTA (700-800°C 10s in N_2)
4) ALD re-growth: Al_2O_3
5) PDA: 400-600°C 30s in N_2
6) S/D contact patterning and Au/Ge/Ni ohmic metal evaporation and 400°C metallization
7) Gate patterning and Ni/Au or Al/Au evaporation

Table 1. Device process flow of surface channel E-mode In-rich InGaAs NMOSFETs with Ni or Al used as gate electrodes.

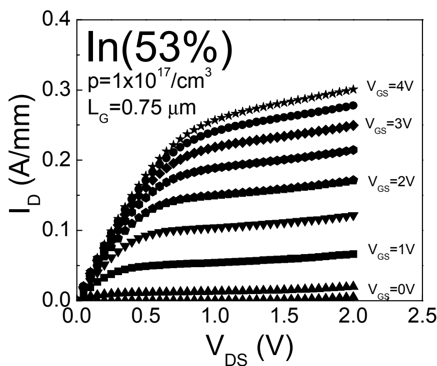

Fig. 2. Drain current (I_D) versus drain bias (V_{DS}) as a function of gate bias (V_{GS}) for Al_2O_3(8nm)/$In_{0.53}Ga_{0.47}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 0.3 A/mm.

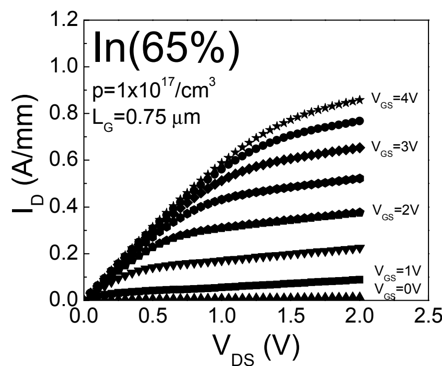

Fig. 3. Drain current versus drain bias as a function of gate bias for Al_2O_3 (10nm) /$In_{0.65}Ga_{0.35}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 0.86 A/mm.

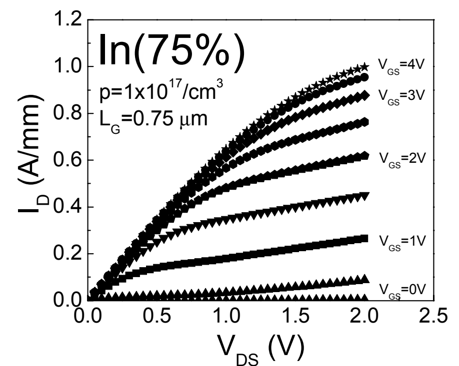

Fig. 4. Drain current versus drain bias as a function of gate bias for Al_2O_3 (10nm) /$In_{0.75}Ga_{0.25}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 1.0 A/mm.

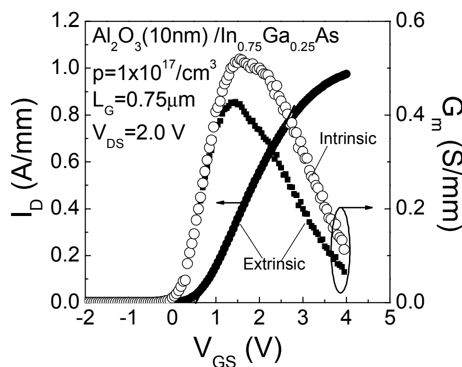

Fig. 5. Extrinsic and intrinsic peak transconductances (G_m) versus gate bias for Al_2O_3 /$In_{0.75}Ga_{0.25}As$ NMOSFETs with 0.75-μm gate length. The extrinsic and intrinsic G_m is 0.43 S/mm and 0.52 S/mm, respectively. Threshold voltage (V_T) of 0.5V is obtained in the linear region (V_{DS}=0.05 V).

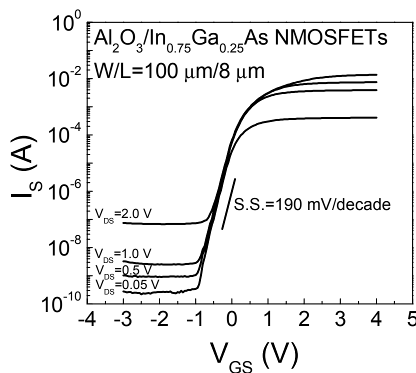

Fig. 6. Source currents versus gate bias as a function of drain voltages for Al_2O_3 /$In_{0.75}Ga_{0.25}As$ NMOSFETs measured at room temperature. The DIBL is 17 mV/V and the subthreshold swing (S.S.) is 190 mV/decade.

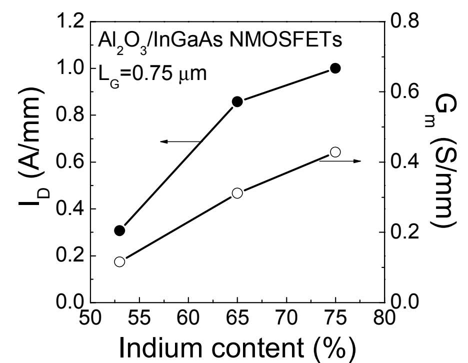

Fig. 7. The Maximum drain currents and peak-transconductance versus indium content in InGaAs channels. I_D and G_m increase with increasing indium content in InGaAs MOSFETs.

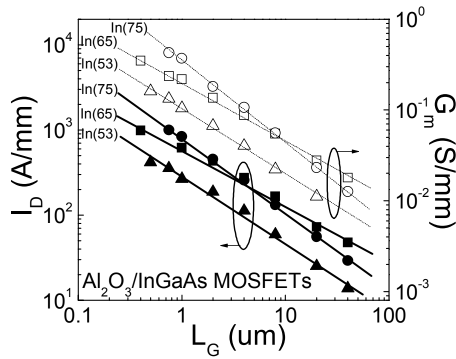

Fig.8. Comparison of scaling behavior of drain current and transconductance versus gate length with different indium content InGaAs NMOSFETs.

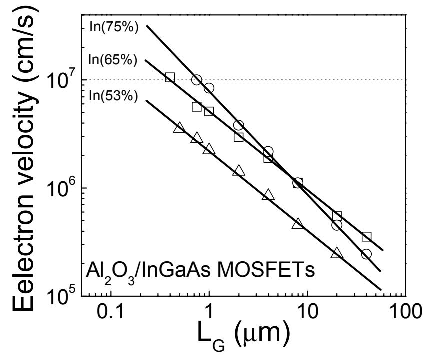

Fig.9. Effective electron velocity versus gate length with different indium content InGaAs MOSFETs. The effective electron velocity is 1×10^7cm/s for $In_{0.65}Ga_{0.35}As$ at 0.4-μm gate length and $In_{0.75}Ga_{0.25}As$ at 0.75-μm gate length.

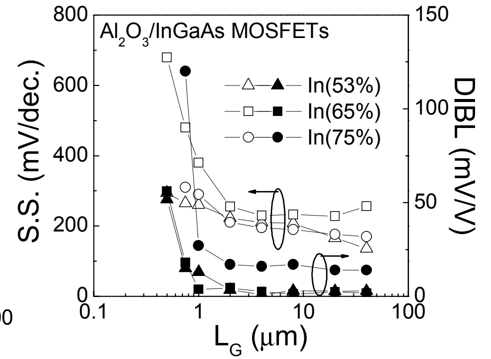

Fig.10. Comparison of subthreshold swing (S.S.) and drain induce barrier lowering (DIBL) for different indium content InGaAs NMOSFETs with different gate lengths.

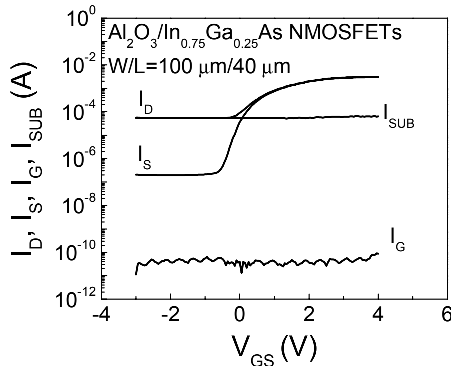

Fig. 11. Drain current (I_D), source current (I_S), gate current (I_G) and substrate current (I_{SUB}) versus gate bias for $In_{0.75}Ga_{0.25}As$ NMOSFETs at V_{DS}=2.0 V. The I_D is 2-orders higher than I_S at V_{GS}<0 V due to I_{SUB}.

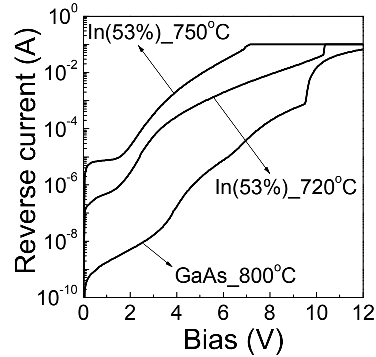

Fig. 12. The reverse biased current of p-n junction with different S/D activation temperature for GaAs and InGaAs MOSFETs. Higher activation temperature leads to more junction leakage.

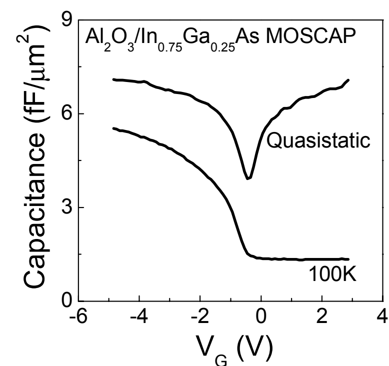

Fig. 13. Quasistatic *C-V* and high-frequency (100KHz) *C-V* for Al_2O_3 /$In_{0.75}Ga_{0.25}As$ MOSCAP measured at room temperature in dark.

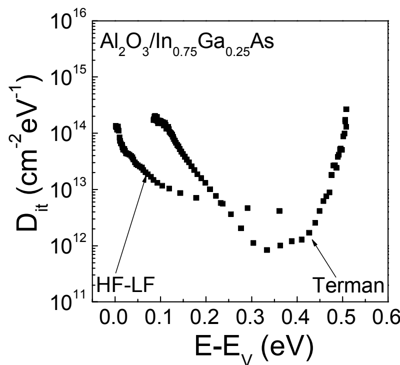

Fig. 14. The distribution of interface trap densities (D_{it}) for $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSCAP. The D_{it} is estimated through HF-LF and Terman method.

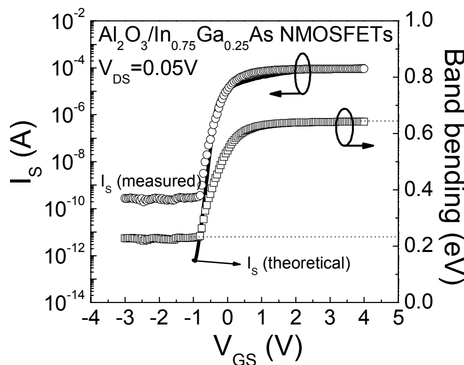

Fig. 15. Source current and band bending versus gate bias for $Al_2O_3/In_{0.75}Ga_{0.25}As$ NMOSFETs. The band bending cover almost the whole bandgap indicating no Fermi level pinning.

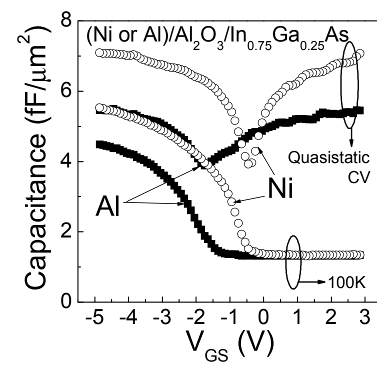

Fig. 16. Quasistatic and HF *C-V* characteristics for $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSCAP measured at room temperature in dark. The Al gated device shows smaller C_{ox} mainly due to the oxidation of 1~2 nm Al at Al/Al_2O_3 interface during Al evaporation. The shift of flat-band voltage (~ 1.0 eV) is the difference of work function of Al and Ni, also indicates no Fermi level pinning.