Multi-probe Interface Characterization of $In_{0.65}Ga_{0.35}As/Al_2O_3$ MOSFET

D. Varghese, Y. Xuan, Y. Q. Wu, T. Shen, P. D. Ye, and M. A. Alam

Purdue University, West Lafayette, IN• 47907, Ph-765-494-5988, dvarghe@purdue.edu

Abstract

Through a combination of measurement techniques, we study the interface properties of $In_{0.65}Ga_{0.35}As$ transistor with ALD deposited Al_2O_3 gate dielectric. We show that the interface trap density at $In_{0.65}Ga_{0.35}As/Al_2O_3$ interface can be relatively high, but the transistor still exhibits inversion characteristics. A detailed profiling of the interface traps shows that majority of the interface traps are donor-like, and explains the absence of Fermi level pinning in spite of the high interface trap density.

Introduction

With aggressive scaling of device dimensions, it is expected that the widely successful silicon CMOS technology will approach its fundamental limits within the next few technology nodes. Substrate material based on III-V compound semiconductor like $In_xGa_{1-x}As$ is an attractive choice for replacing silicon NMOS transistors due to their higher electron mobility [1-5]. However the interface properties of transistors based on III-V substrate materials are not well understood, and are often a topic of significant debate. In this paper we use a wide range of measurement techniques to characterize the $In_{0.65}Ga_{0.35}As/Al_2O_3$ interface so as to obtain the trap density, type and location in position and energy. *We show that the interface trap densities are high, but remarkably/counter-intuitively, it is still possible to attain large inversion current since majority of the traps are donor-like*.

Interface trap characterization

Fig. 1 shows the device structure used in the study, the fabrication steps of which are discussed in [1-2]. The I_D-V_D characteristics of the device are shown in Fig. 2, and drain current exceeding 1A/mm is obtained. Capacitance-voltage (CV) measurements are carried out at various frequencies (Fig. 3) to study the interface properties of the transistor. The inversion capacitance increases at lower frequencies, suggesting the formation of inversion channel. The interface trap density (D_{IT}) within the semiconductor bandgap is measured using the Hi-Lo CV method [6], and trap densities above $4.8x10^{12}/cm^2$ eV are obtained (see Fig. 9). Similar values of D_{IT} in the order of $2\text{-}3x10^{12}/cm^2$ eV were also obtained using conductance (G-V) method [7].

Fig. 4a shows the transistor I_D-V_G characteristics. The sub-threshold slopes (SS) of the transistors are found to be high, indicating large interface trap density. Fig. 4b shows the SS and corresponding D_{IT} which is in the order of $1\text{-}2x10^{13}/cm^2$ eV. It is interesting to note that although

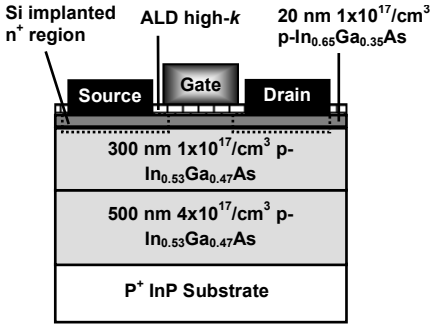


Figure 1. Device structure of InGaAs MOSFET used in the study. The fabrication steps are discussed in [1-2].

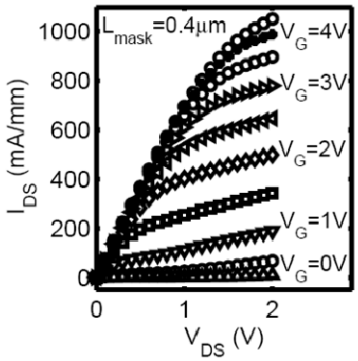


Figure 2. I_D-V_D characteristics of InGaAs MOSFET structure in Fig. 1. Drain current above 1A/mm is obtained with the $In_{0.65}Ga_{0.35}As$ channel material. High drain current indicates formation of inversion channel.

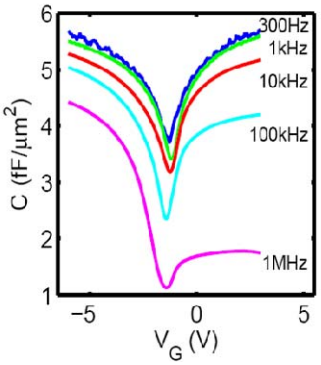


Figure 3. C-V characteristics measured at various frequencies with source/drain floating. C_{INV} increases at lower frequencies suggesting channel inversion. The HF/LF CV curves are used to obtain D_{IT} profile within the semiconductor bandgap.

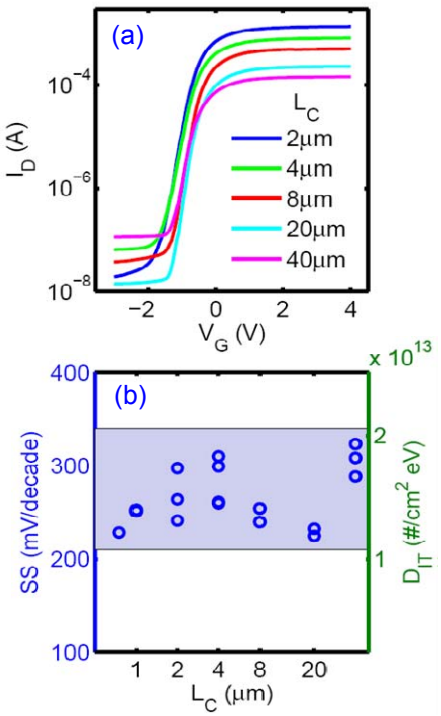


Figure 4. (a) I_D-V_G characteristics in logarithmic scale. Sub-threshold slopes (SS) obtained from I_D-V_G characteristics are high, suggesting high interface trap densities. (b) SS and interface trap density for various channel lengths. SS shows a larger variation compared to V_T suggesting donor-like traps.

D_{IT} shows variation close to factor of 2, the V_T shows a smaller variation, suggesting predominantly donor-like traps within the InGaAs band gap.

Charge pumping (CP) currents measured on various channel length devices are shown in Fig. 5a. A high offset CP current is obtained as the channel length is extrapolated to zero, which has been identified as contribution from substrate region under the gate pad (see Fig. 6). The slope of I_{CP} vs. L is used to obtain D_{IT} ~ 1.5x10^{13}/cm^2 eV. Note that the energy window scanned by

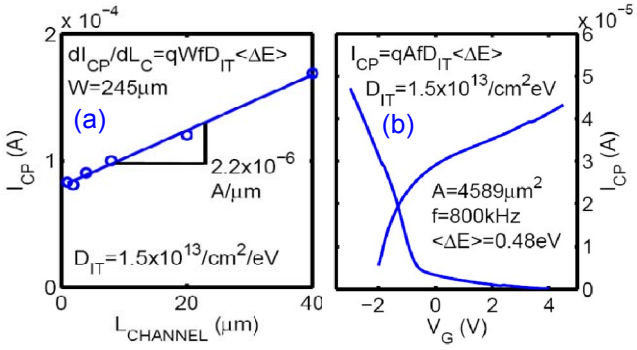


Figure 5. (a) CP measurements at various channel lengths. The constant offset current at L_C=0 is due to region under the gate pad (see Fig. 6). D_{IT} is obtained from slope of I_{CP} vs. L_C. (b) CP measurements with gate pad cut off. Both measurements give very close D_{IT} values.

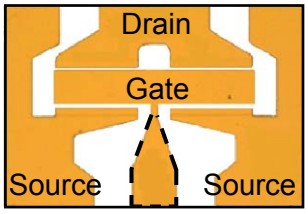


Figure 6. Photograph showing device layout. Gate pad extension is found to corrupt CP measurement and is cut apart (region enclosed by dashed line). Channel width W=100μm for each side and channel length L_C=40μm.

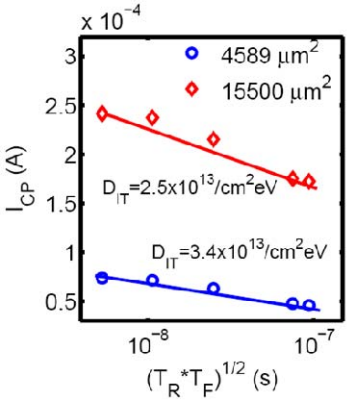


Figure 7. Multiple rise/fall time CP measurements provide energy profile of interface damage. D_{IT} is obtained from the slope of I_{CP} vs. $\ln((T_R*T_F)^{1/2})$ and is found to be close to that computed from full CP measurements (see Fig. 5).

CP vary within the oxide (see Fig. 13a), and hence a weighted average ΔE is used. *Full CP sweep on device with gate pad partly removed (Fig. 5b), and multiple rise/fall time CP measurement carried out on devices with different gate areas (Fig. 7) also give similar D_{IT}.*

The low frequency CV (LF-CV) has been simulated in presence of D_{IT} and matched with measurement (see Fig. 8). The D_{IT} profile that has been used to match the simulated CV curve with measurement is shown in Fig. 9a. Fig. 9b explains the algorithm used to

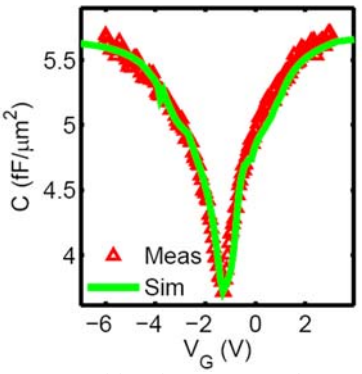
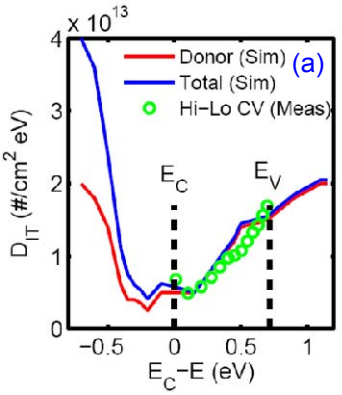


Figure 8. Measured low frequency CV characteristic (f=300Hz) is matched with simulation by introducing interface traps. The D_{IT} profile used to obtain the match is shown in Fig. 9a and the algorithm used to model the impact of D_{IT} is explained in Fig. 9b.



1: Simulate ideal CV for D_{IT}=0 (b)

For each V_G on the ideal CV curve:

2: Obtain surface band bending ψ_S and location of quasi-Fermi level F_N.

3: Compute occupancy of $D_{IT}(E)$, net charge and corresponding ΔV_G.

4: Compute $C_{IT}=qD_{IT}(\psi_S)$

5: Compute capacitance for $V_G+\Delta V_G$:

$$C_G = \frac{C_{OX}(C_{IT}+C_S)}{C_{OX}+C_{IT}+C_S},$$

where $C_S(\psi_S)$ is the semiconductor capacitance obtained from ideal CV.

Figure 9. (a) D_{IT} profile used to match measured and simulated LF-CV characteristic. A good match is obtained by using donor-like traps below the InGaAs conduction band. The trap density within InGaAs band gap agrees well with that measured using Hi-Lo CV technique. (b) Algorithm used to obtain LF CV characteristic in the presence of interface traps from the ideal CV.

Method	D_{IT} (E) ($cm^{-2}eV^{-1}$)			Trap type
	$E=E_C$	$E=E_{MID-GAP}$	$E=E_V$	
G-V	$2x10^{12}$	$3x10^{12}$	–	*
Hi-Lo CV	$6.7x10^{12}$	$8.4x10^{12}$	$1.6x10^{13}$	*
LF-CV	$5.6x10^{12}$	$1x10^{13}$	$1.5x10^{13}$	Donor
SS/V_T	–	$1\text{-}2x10^{13}$	–	Donor
CP	–	$1.5\text{-}3.5x10^{13}$	–	*

Figure 10. Summary of D_{IT} profile obtained from various techniques. Note that the sensitivity of the G-V method is lower at high interface trap densities ($qD_{IT}>C_{OX}$) [9], and might explain the slightly lower D_{IT} values compared to other techniques. SS/V_T and LF-CV techniques suggest significant contribution from donor-like traps. *Cannot distinguish between donor/acceptor traps.

model the impact of interface traps into the simulated CV curve. Full numerical simulation also gives identical results [8]. Donor-like traps with density ~$1x10^{13}/cm^2$ eV within the energy bandgap of InGaAs is required to match the experimental CV characteristics.

Fig. 10 provides a summary of interface trap profile from various characterization techniques. Different interface characterization techniques, depending on the region probed, provide a range D_{IT} from $2x10^{12}$-$3x10^{13}/cm^2$ eV. For Si/SiO_2 systems, the CP in general provides most accurate/reliable estimates of D_{IT}, however since various methods probe different spatial/energy extends into the dielectric and since consistency of assumptions in various techniques cannot be guaranteed a-priori, additional work is needed for quantitative measure of D_{IT} at high-k/III-V interface. However it is interesting that the inversion-mode InGaAs MOSFET still works well with the relatively high D_{IT}, and we will address this question in the next section.

Simulation Results

The relatively high D_{IT} obtained from various characterization techniques have often been linked to Fermi level pinning, which in turn will prevent transistor inversion. However, I_D-V_G and CV characteristics clearly show inversion operation. This puzzle is resolved by noting that if the interface states are due to donor-like traps as suggested by I_D-V_G (Fig. 4) and LF-CV techniques (Fig. 8, 9), the V_T and ON-current of the transistor remain unaffected. This is also proven by the I_D-V_G characteristics obtained from detailed MEDICI simulation for various donor-like trap densities (Fig. 11a). Note that the SS values alone cannot distinguish between acceptor/donor-like traps (Fig. 11c), and hence cannot be used as a signature of Fermi level pinning. However, I_D-V_G characteristics for acceptor-like traps show an increase in V_T which makes inversion operation difficult (Fig. 11b), while full inversion – consistent with observed results in Fig. 4 is possible with donor-like traps. *We emphasize that this key*

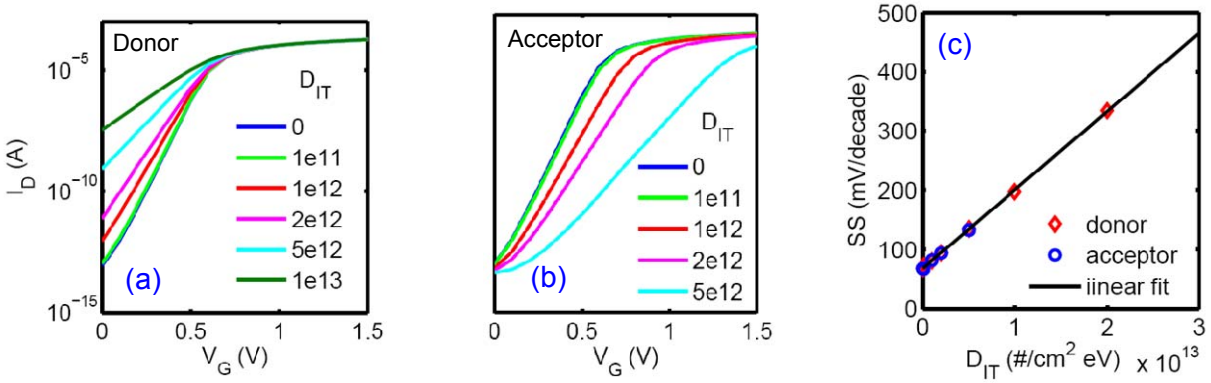


Figure 11. MEDICI simulation of InGaAs MOSFET with (a) donor-like and (b) acceptor-like interface traps. Donor-like traps change the SS and OFF-current of the device, keeping the V_T and ON-current unchanged. Acceptor-like traps degrade SS, V_T and ON-current. (c) SS from simulated I_D-V_G for various acceptor/donor-like trap densities. SS is independent of the nature of the traps and depends only on the trap density.

distinction has been absent in all debates regarding the influence of interface traps at the III-V/high-k interface.

It is interesting to note a couple of things from the above analysis. The concept of charge neutrality level (CNL) is often linked with Fermi level pinning at metal-semiconductor interface, in which the Fermi level is assumed to be pinned close to the CNL [10]. Similarly, the closer the CNL at semiconductor/dielectric interface is to the conduction band, the easier it is to attain inversion. A dominant contribution from donor-like traps moves the CNL closer to the conduction band, and is therefore consistent with the previous reports [11] that suggested CNL in $In_{0.65}Ga_{0.35}As$ might be close to the conduction band edge.

Secondly, significant contribution of donor-like traps in the semiconductor bandgap makes it difficult to move the Fermi level towards the valence band edge, in order to turn off the transistor. Therefore, the SS and OFF currents of such transistors can be relatively high, as shown in Fig. 11a. Also, a similar interface trap profile in PMOS transistors might result in Fermi level pinning for the same reason explained above, thereby lowering the drive currents.

Bulk trap characterization

In addition to interface trap characterization, the multi-frequency CP (MFCP) measurement [12] (Fig. 12) is used to profile the trap densities into the bulk of Al_2O_3. The spatial and energy extends scanned by MFCP are obtained through a numerical solution of carrier capture and emission between substrate and the trap level, with charge pumping pulse applied at the gate. Simulation results in Fig. 13a indicate that CP scans non-uniform energy extends into the bulk, which can be as large as 0.8eV at the region where differential CP current is to be computed. A non-uniform bulk trap profile is extracted and is shown in Fig. 13b. Bulk trap densities in the order of 7-20x10^{19}/cm^3 eV are obtained, which is a reasonable value for deposited high-k dielectrics [13-14].

Conclusions

Based on a combination of measurement techniques and simulation we show that the nature of the trap – and not the number alone – determines Fermi level pinning and surface inversion. The InGaAs/Al_2O_3 based transistors are shown to exhibit strong inversion characteristics in spite of the relatively high trap densities as majority of the traps are donor-like. And thereby, our work addresses a long-standing controversy in the field and provides a new approach to understand high-k/III-V interface properties and their effect on device performance.

Acknowledgement: We would like to acknowledge Md. Masuduzzaman for the MFCP simulation, Birck Nanotechnology Center at Purdue for the experimental facilities, and NCN, NSF, SRC FCRP MSD Center for providing financial support.

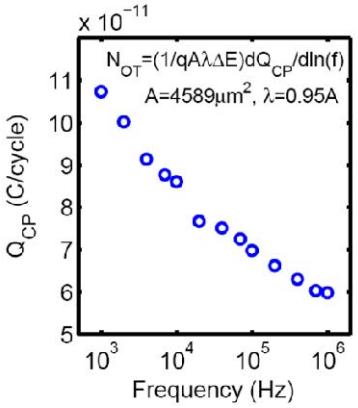


Figure 12. Charge pumped per cycle for various frequencies. Bulk trap density is obtained from the slope of Q_{CP} vs. ln(f) curve (see Fig. 13b).

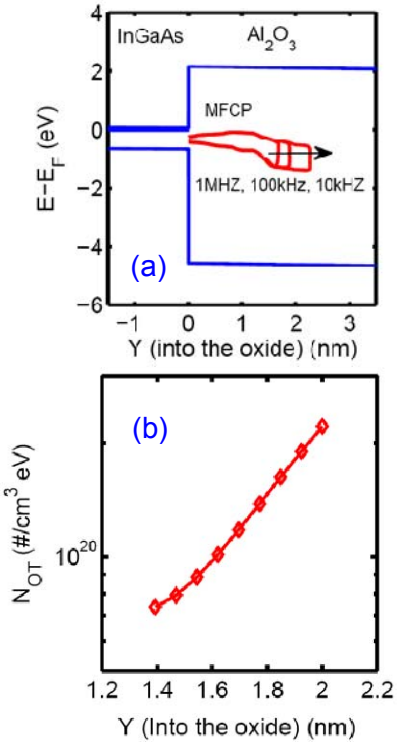


Figure 13. (a) Position and energy scanned by MFCP measurement. ΔE scanned by CP is ~0.18eV at the interface, but increases to ~0.8eV deeper into the oxide. (b) Bulk trap density obtained from MFCP measurement. D_{IT} values summarized in Fig. 10 are consistent with the obtained bulk trap density.

References: [1] Y. Xuan *et al.,* IEDM, p. 637, 2007. [2] Y. Xuan *et al.,* EDL, **29(4)**, p.294, 2008. [3] Y. Sun *et al.,* CS MANTECH Conference, p. 231, 2007. [4] S. Datta *et al.,* EDL, **28(8)**, p.685, 2007. [5] D-H Kim *et al.,* IEDM, p. 629, 2007. [6] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, Wiley-Interscience, 1982. [7] K. Martens, Personal communication, 2008. [8] M. Satter, Personal communication, 2008. [9] K. Martens *et al.,* TED, **55(2)**, p.547, 2008. [10] A. Dimoulas *et al.,* APL, **89**, p.252110, 2006. [11] Y. Xuan *et al.,* APL, **91**, p.232107, 2007. [12] Y. Maneglia *et al.,* JAP, **79**, p.4187, 1996. [13] H. D. Xiong *et al.,* IRPS, p. 319, 2008. [14] H. D. Xiong *et al.,* Microelectronic Engineering, **84**, p.2230, 2007.