Positive Bias Temperature Instability Degradation of InGaAs n-MOSFETs with Al_2O_3 Gate Dielectric

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Abstract

CP measurements show that PBTI stress induced interface trap area density ΔN_{it} in InGaAs/Al_2O_3 n-MOSFET is very small and has power law time evolution $At^{0.22}$ in the stress phase, and is partially recovered in the recovery phase. However the DC I_s-V_g measurements show large degradations of negative ΔV_g and sub-threshold swing S in the sub-threshold region and are recovered in the recovery phase, also show degradation of positive ΔV_g in the on-current region and continuing degradation in the recovery phase until reaching a stable state. The I_s-V_g degradation is mainly contributed by generation of near interface slow oxide traps under stress with recoverable donor trap energy density ΔD_{SOX}^{DONOR} in the InGaAs energy gap with a tail extended to the conduction band energy, and permanent acceptor trap energy density $\Delta D_{SOX}^{ACCEPTOR}$ in the conduction band energy with a tail extended to the energy gap. This trap model explains all experimental details perfectly.

Introduction

InGaAs n-MOSFET has attracted great attentions for possible replacement of its Si counterpart in the future (1-3). However, its reliability research is still in the infant stage (3, 4). In this work, we systematically investigate the InGaAs n-MOSFETs degradation under PBTI stress and recovery in the recovery phase by comprehensive experiments (at room temperature) and physical interpretations.

Transistor Fabrication

The $In_xGa_{(1-x)}As$ (x = *0.53* and *0.65*) n-MOSFET fabrication process and structure were illustrated in (1), with *8 nm* physical thickness Al_2O_3 gate dielectric, Ni/Au metal gate, and channel doping $1\text{-}2\times10^{17}\ cm^{-3}$.

Experimental Results and Interpretations

(1). *Charge Pumping (CP) measurements:* Figures 1-3 show generation of interface traps ΔN_{it} in the stress phase and partial recovery in the recovery phase. The time evolution of ΔN_{it} in the stress phase shows a power law $\Delta N_{it} \propto t^n$ with index $n = 0.22$, close to the index n of Si/SiON pMOSFET under NBTI stress with same CP measurement (5). In the Si case, $n = 0.25$ corresponds to the H atoms released from the Si dangling bond (6). In the InGaAs/Al_2O_3, there are Ga (or In) and As dangling bonds. $n = 0.22$ may provide a starting point for investigation of the interface trap degradation mechanism.

(2). *DC I_s-V_g measurements:* Figures 4-11 are the results of DC (slow) measurements by *Agilent 4156C*.
(2.1). ΔV_g extracted at low I_s in the sub-threshold region has negative shift after PBTI stress (Figures 4, 8), accompanying by degradation of sub-threshold swing (S) (Fig. 6), and partial recovery when the stress is terminated (Figs 5, 6, 8). This is explained by donor interface traps (7, 8) generation in the stress phase and recovery in the recovery phase.

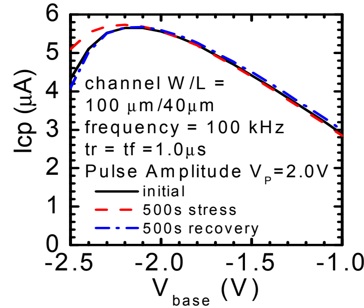


Fig.1. Charge Pumping (CP) current for the fresh $In_{0.65}Ga_{0.35}As$ n-MOSFET, after *500s* PBTI stress, and after *500s* recovery, respectively. The interface trap area density $N_{it} = I_{cp}/(fqA_G)$, A_G is gate area. From the I_{CP} peak of the fresh device, $N_{it}^0 \approx 9\times10^{12}\ cm^{-2}$.

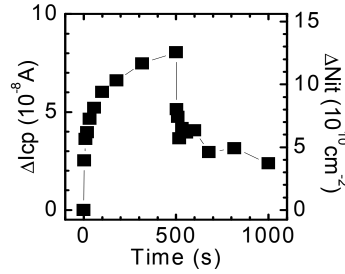


Fig.2. The time evolution of ΔI_{cp} in PBTI stress phase (*0-500s*, V_g*=3V*) and recovery phase (*500-1000s*, V_g*=0*). The interface trap area density ΔN_{it} is calculated by $\Delta I_{cp}/(fqA_G)$.

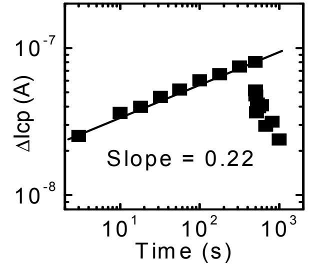


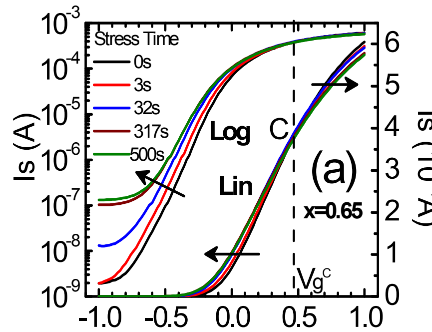
Fig.3. Same as Fig. 2, plot in log-log scale, indicates power law $\Delta N_{it} \propto t^{0.22}$ in the stress phase.

(2.2) ΔV_g extracted at high I_s (on-current region) has positive shift after PBTI stress (Figs 4, 8), accompanying by transconductance degradation (Fig. 7). In Figures 5, 8, ΔV_g at high I_s continuously degrades (increases) in the recovery phase and approaches a stable value after few thousands of seconds (not shown in the Figures). By these facts, we propose the generation of permanent acceptor interface traps under stress phase. When acceptor traps are generated and trapped by electrons, give rise positive ΔV_g and mobility degradation.
(2.3) As shown in Fig. 4, when V_g = *-0.8 V* to *-1 V*, the I_s (denoted by I_s^{off}) is almost saturated with V_g (weak dependence of V_g). The increased ΔI_s^{off} under stress is recovered in the recovery phase. If ΔI_s^{off} is due to change of surface potential pinning (4), ΔI_s^{off} is the current in the sub-threshold region and should satisfy (9)

$$\Delta I_s^{off} = A\,[1-\exp(-qV_d/kT)] \qquad (1)$$

which saturates with V_d when $V_d > 3kT/q \approx 0.1V$. For x = *0.53* device, I_s^{off} is in the range of 10^{-10} *A* (Fig. 4(b)). In Fig. 9, ΔI_s^{off} satisfies eq. (1), implying that the degradation (and

recovery) of ΔI_s^{off} is due to generation (and recovery) of large energy density of donor traps above the valence band E_V, causing change of surface potential pinning. For $x = 0.65$ device, I_s^{off} is in the range of 10^{-9}-$10^{-7}A$ (Fig. 4(a)). As shown in Fig. 10, ΔI_s^{off} does not satisfy eq. (1). On the other hand, the drain pn junction has larger reverse bias leakage as shown in Fig.11, probably due to the narrower energy gap for $x = 0.65$ device. The ΔI_s^{off} is likely due to existence of a surface conduction path across the source and drain. This could be due to orbital overlap between neighboring donor traps induced by the stress. The drain leakage partially flow to source through the surface conduction path and ΔI_s^{off} satisfies a near ohmic relationship with V_d as shown in Fig. 10.



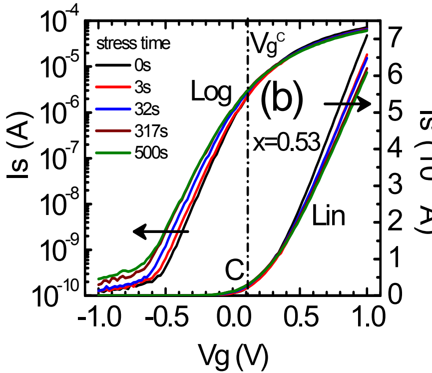
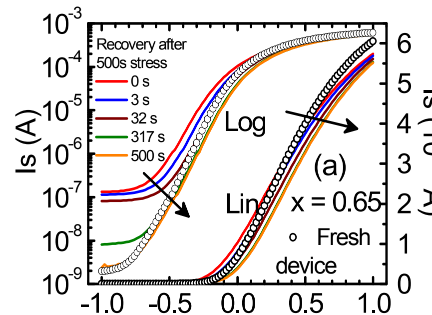


Fig.4 I_s-V_g curves (curves **Log** in Log I_s scale, curves **Lin** in linear I_s scale), V_d=*50mV*, for the fresh $In_xGa_{1-x}As$ n-FET and the change under PBTI stress (V_g=*3V*), **(a)** x= *0.65* , *W/L*= 100/4 (μm),**(b)**x=*0.53*, *W/L*= 100/8 (μm). The ΔV_g at constant current I_s is negative in the sub-threshold region, accompanying degradation of S, support donor interface traps (7) generation under stress. ΔV_g is positive at high I_s in the on-current region due to acceptor interface traps generation, accompanying degradation of transconductance G_m (Fig.7). A crossing point C with V_g^C is defined by ΔV_g=*0.*



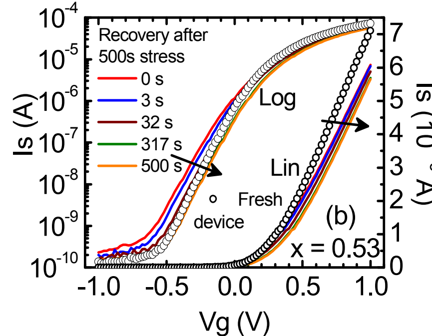


Fig.5 Same as Fig.4, however for change in the recovery phase. Negative ΔV_g at I_s in the sub-threshold region and degraded S recover gradually, indicating recovery of the donor interface traps. The positive ΔV_g at high I_s does not recover, but continuously increases in the recovery phase, also shown in Fig.8. Comparing with fresh device, the I_s-V_g curve after *500s* recovery shows existence of acceptor interface traps extending to the lower half energy gap (7), explained by Fig.17.

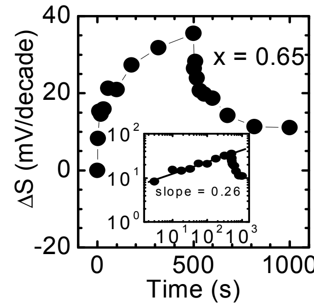


Fig.6. Time evolution of change of sub-threshold swing ΔS extracted from Figs. 4, 5 (a).

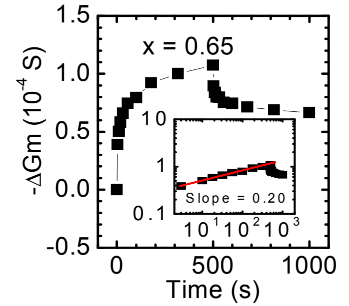


Fig.7. Time evolution of degradation of peak transconductance ΔG_m extracted from Figs. 4, 5(a).

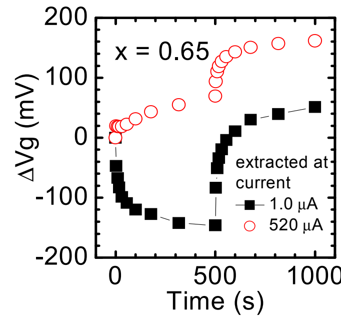


Fig.8. Time evolution of ΔV_g at sub-threshold I_s (1.0 μA) and on-current I_s (520 μA) in PBTI stress phase (*0-500s*) and recovery phase (*500-1000s*), extracted from Figs.4, 5(a). ΔV_g at on-current region continuously increases in the recovery phase, and ΔV_g at SS region turns to positive at the end of recovery phase, all explained by Fig.17.

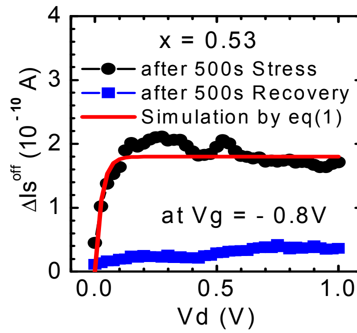


Fig.9. For x=*0.53* FET, ΔI_s^{off} at V_g=*-0.8V* is in the range of $10^{-10}A$. ΔI_s^{off}-V_g satisfies eq(1), implying that ΔI_s^{off} under stress is due to generation of donor traps close to the valence band and close to interface, causing change of surface potential pinning.

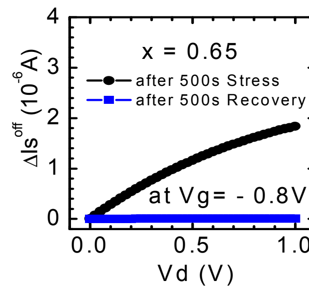


Fig.10. For x=*0.65* FET, ΔI_s^{off} at V_g=*-0.8V* is in the range of 10^{-7} *to* $10^{-6}A$. ΔI_s^{off}-V_d does not satisfy eq(1). Different conduction mechanism is proposed in the text.

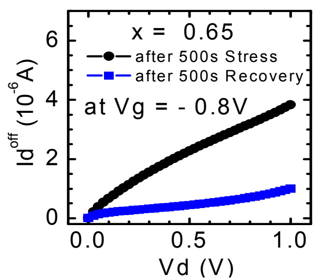


Fig.11 same as Fig.10 however for I_d^{off}-V_d curve. Comparing with Fig.10, only *1/2* drain pn junction leak current flow to source, other part flow to the substrate.

(3) ***Four issues resolved by one trap model:*** In above experimental results, there are four issues to be resolved: (i) by CP measurement, the stress induced interface trap area density ΔN_{it} is only 1.3×10^{11} cm^{-2} , comparing with the process induced interface trap area density N_{it}^0 ($\approx 10^{13}$ cm^{-2}) of the fresh device (Figures 1, 2). However ΔN_{it} is very large (10^{12} cm^{-2}) estimated by I_s-V_g measurement (Fig. 4) by $\Delta N_{it} = (C_{OX}/q)\Delta V_g$ (9), C_{OX} is the gate oxide capacitance. (ii) There

is an I-V curve crossing point C at $V_g^{\ C}$ from negative to positive ΔV_g (Fig. 4). Point C may be interpreted by that the interface charge neutrality level E_{CNL} (8) roughly coincides with the Fermi level, all ΔN_{it} are neutral and $\Delta V_g = 0$. However as shown in Fig.4, $V_g^{\ C}$ is in the inversion region and E_{CNL} is above the bottom of the conduction band E_C (confirmed by Atlas simulation), in conflict with the well known results that E_{CNL} is below E_C for $In_xGa_{1-x}As$ when $x = 0.65$ or 0.53 (8). (iii) ΔV_g extracted at high current continuously degrades (increases) when the stress is terminated (Figures 5, 8). This can not be interpreted by permanent acceptor traps generated only in the stress phase. (iv) Carefully observing the I_s-V_g curve after *500 s* recovery in Fig. 5, in the sub-threshold region it has larger positive ΔV_g extracted at higher I_s level comparing with the fresh device I_s-V_g curve, indicating existence of acceptor interface traps (7) in the energy gap below E_{CNL}, in conflict with the conventional interface trap model (8) that acceptor interface traps only exist above E_{CNL}.

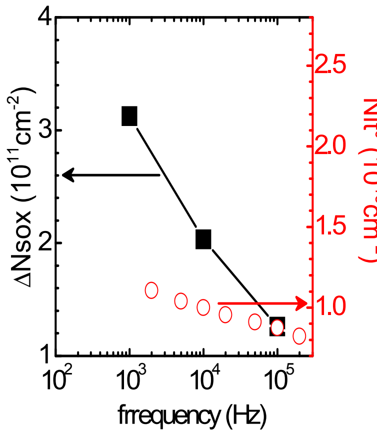


Fig.12 Frequency f dependence of $N_{it}^{\ 0}$ of fresh device and stress induced ΔN_{SOX} estimated by CP experiments by $(I_{cp}/f)/qA_G$. The process induced $N_{it}^{\ 0}$ has major component of fast interface traps and therefore has weak f dependence. The stress induced ΔN_{SOX} has major component of slow near interface oxide traps and therefore has strong f dependence (10), seriously underestimated by CP. This is further confirmed by I_s-V_g measurement at the sub-threshold region in Figs.4, 15 in much slower time zone.

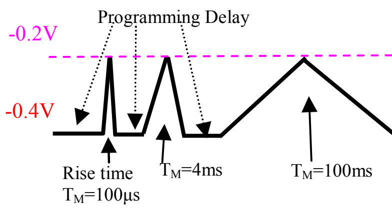


Fig.13. The pulse waveform for the pulsed I_s-V_g measurement (11). Each measurement procedure consists of three sequential pulses with measurement times T_M=*100µs, 4ms* and *100 ms* respectively.

To resolve these issues, the following experiments are conducted. In Fig. 12, the strong frequency f dependence of $Q_{CP} = Icp/f$ of ΔN_{it} indicates that ΔN_{it} has major component of near interface slow oxide traps (10). Therefore we re-denote stress induced traps ΔN_{it} by slow oxide traps ΔN_{SOX}. ΔN_{SOX} can not follow fast surface potential change and therefore is seriously underestimated by CP measurement. However it can follow slow surface potential change and induces large degradation in slow I_s-V_g measurements. Comparing with f dependence of ΔN_{SOX} in Fig. 12, the extension of ΔN_{SOX} to lower than *1 KHz* frequency can explain the large S and ΔV_g degradations in DC I_s-V_g measurement quantitatively. To further inspect this point, experiment in 10^{-1}-10^{-4} second time zone of the pulsed I_s-V_g measurement we developed in 2004 (11) was employed, however extend to the sub-threshold region with much lower current level and more challenging. Reducing the pulse rise time T_M in the I_s-V_g measurement should reduce the S degradation if ΔN_{SOX} can not follow the fast surface potential change. This is verified and explained in Figs. 13-16.

Combining Fig. 12 and Fig. 15 gives very strong support of domination of slow ΔN_{SOX} in the stress induced traps. Further, ΔN_{SOX} trap energy density could be different from the conventional interface trap density explained in (8). We propose that ΔN_{SOX} includes recoverable donor traps with energy density $\Delta D_{SOX}^{\ DONOR}(E)$ in the energy gap however has a tail extended to above E_c in the conduction band energy, and the permanent acceptor trap with energy density $\Delta D_{SOX}^{\ ACCEPTOR}(E)$ above E_c , however has a tail extended to the energy gap, as shown in Fig. 17. This trap model perfectly interprets all experimental results in all aspects and resolves all issues in a unified frame as explained in Figs. 17, 18.

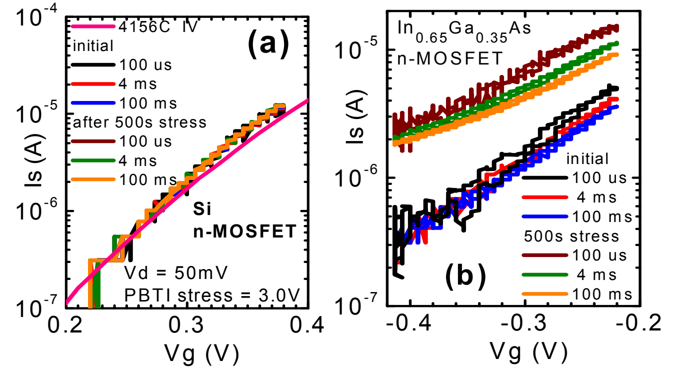


Fig.14. I_s-V_g curves in the sub-threshold region measured by the pulsed I-V method (Fig.13). **(a)** For Si nMOSFET. All curves measured by different T_M coincide completely, implying no error introduced by the fast pulsed method. Small deviation from the curve measured by *Agilent 4156C* is due to scaling difference between *4156C* and the amplifier. **(b)** For fresh $In_{0.65}Ga_{0.35}As$ nMOSFET and after *500s* PBTI stress. The curves measured by faster T_M has smaller sub-threshold swing S and larger ΔV_g, indicating existence of slow donor traps as explained by Fig.16.

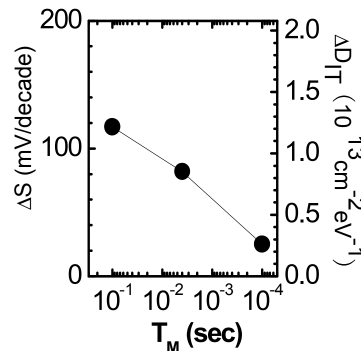


Fig.15. Degradation of sub-threshold swing ΔS after 500s PBTI stress, extracted from the data in Fig.14(b).The generated slow oxide trap energy density $\Delta D_{SOX}=[C_{OX}/(qkTln10)]\Delta S$ (9) is also plotted. ΔD_{SOX} is seriously underestimated when T_M is reduced, indicating domination of slow donor oxide traps as explained by Fig.16.

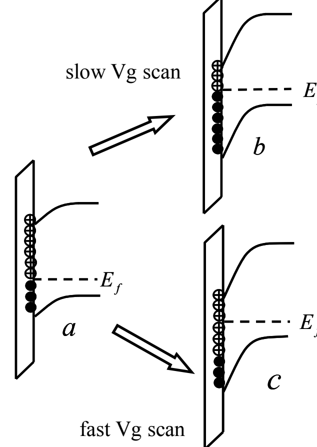


Fig.16. Surface potential band diagrams of $In_{0.65}Ga_{0.35}As$ n-MOSTEF used to explain the results of Figs. 14(b), 15. **(a)** Surface potential for V_g=*-0.4V,* **(b)** Surface potential for V_g=*-0.2V* by slow V_g scan from -0.4V. Slow donor traps can response to capture electrons to reduce the positive charge, causing smaller ΔV_g and larger ΔS. **(c)** Same as (b) however fast scan of V_g, slow donor traps can not response, no change of positive charge, causing larger ΔV_g and smaller ΔS.

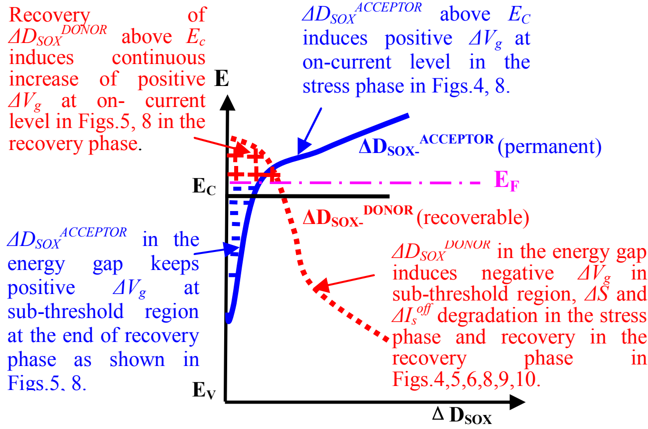


Fig.17. Stress induced near interface slow oxide trap energy density $\Delta D_{SOX}(E)$ consists of permanent acceptor traps $\Delta D_{SOX}^{ACCEPTOR}$ and recoverable donor traps ΔD_{SOX}^{DONOR}, with electrons slowly exchanging with the channel. When moving E_F to a level above E_C slowly during DC *I-V* measurement that positive donor trap charge equals to the negative acceptor trap charge, it corresponds to V_g^C point in Fig.4 with $\Delta V_g=0$. This trap model explains all aspects in all experimental results in this work in a unified frame, also shown by simulation in Fig.18

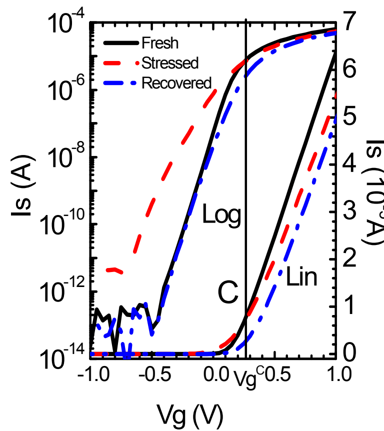


Fig.18. Atlas simulation using trap model of Fig.17 explains all degradation characteristics and all issues in Figs.4-12, including: (1) degradation and recovery of negative ΔV_g, ΔS, ΔI_s^{off}, at the subthreshold region, (2) positive ΔV_g at on current region, and continuous increase in the recovery phase, (3) crossing point *C* at the inversion region, (4) positive ΔV_g in the SS region as well as in the inversion region after *500s* recovery.

Summary

The degradation characteristics of InGaAs/Al_2O_3 n-MOSFET under PBTI stress were investigated. The following conclusions are obtained for the first time: **(1)** Charge pumping (CP) measurements show that the PBTI stress induced interface traps ΔN_{it} is very small ($10^{11}cm^{-2}$) comparing to the large process induced interface traps N_{it}^0 ($10^{13}cm^{-2}$) in the fresh device. ΔN_{it} has power law time evolution $At^{0.22}$ in the stress phase and is partially recovered in the recovery phase. **(2)** The DC I_s-V_g measurements show large degradation in the stress phase and recovery in the recover phase. There is negative ΔV_g (and recovery) in the sub-threshold region and degradation of *S* (and recovery); and positive ΔV_g in the on-current region, continuously degrades (increases) in the recovery phase until reaching a stable value. These degradation characteristics are perfectly explained by generation of near interface slow oxide traps ΔN_{SOX} with recoverable donor traps with energy density ΔD_{SOX}^{DONOR} and permanent acceptor traps with energy density $\Delta D_{SOX}^{ACCEPTOR}$ as shown in Fig. 17. The slow oxide traps can not response to the fast surface potential change and therefore are seriously underestimated in CP and fast *I-V* measurements. **(3)** Large degradation under stress (and recovery) of off-current ΔI_s^{off} at $V_g = -0.8\ V$ *to* $-1\ V$ is due to ΔD_{SOX}^{DONOR} induced change of surface potential pinning for $x = 0.53$ devices with ΔI_s^{off} at $10^{-10}A$ level, however is probably due to creation of another conduction path by orbital overlap between neighboring ΔD_{SOX}^{DONOR} traps for $x = 0.65$ devices with ΔI_s^{off} at $10^{-7}A$ level, with higher pn junction leakage because of the narrower energy gap. This high ΔI_s^{off} of $x = 0.65$ FET is an obstacle to be improved for low standby power application. Very different degradation characteristics comparing with Si MOSFETs is summarized in Table I.

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Table I. Different PBTI degradation characteristics of Si/SiON and InGaAs/Al_2O_3 n-MOSFETs

	I_s-V_g degradation under PBTI stress	Properties of traps generated under PBTI stress	Recovery of traps after stress termination
Si/ SiON n-FET	Very small positive ΔV_g in on-current region, observed by DC I_s-V_g measurement (12).	Stress induced fast interface traps ΔN_{it}, donor traps below CNL, acceptor interface traps above CNL with CNL at mid-gap. ΔN_{it} can be estimated by charge pumping (CP) measurement (12).	A big issue with debate regarding the recovery of interface traps ΔN_{it}. Ref. 5 reported no recovery of ΔN_{it} by CP measurement after NBTI stress in p-MOSFETs. Other groups reported ΔN_{it} recovery (12, 13).
InGaAs /Al_2O_3 n-FET	Large degradation with negative ΔV_g in sub-threshold region accompanying degradation of sub-threshold swing S, large degradation of off-current ΔI_s^{off}, all due to generation of near interface slow donor oxide traps. Positive ΔV_g in on-current region and degradation of G_m, due to generation of near interface slow acceptor oxide traps.	Stress mainly induces near interface slow oxide traps with acceptor trap energy density $\Delta D_{SOX}^{ACCEPTOR}$ above E_C with a tail in the energy gap, and donor trap energy density ΔD_{SOX}^{DONOR} in the energy gap with a tail above E_C, as shown in Fig.17. These traps can exchange electrons slowly with the channel, therefore can response to DC I_s-V_g measurement, however cannot response to the fast surface potential change and seriously underestimated by CP and fast I_s-V_g measurement.	Very small recovery of interface traps ΔN_{it} measured by CP. Very large recovery of stress induced near interface slow donor oxide traps ΔD_{SOX}^{DONOR}. No recovery of stress induced near interface slow acceptor oxide traps $\Delta D_{SOX}^{ACCEPTOR}$