

# Extraction of Channel Electron Effective Mobility in InGaAs/Al<sub>2</sub>O<sub>3</sub> n-FinFETs

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**Abstract**—A compact set of equations based on the multiple subbands quasi-ballistic transport theory is developed, and is used to investigate the channel electron effective mobility in recently reported In<sub>0.53</sub>Ga<sub>0.47</sub>As/Al<sub>2</sub>O<sub>3</sub> tri-gate n-FinFET. The extracted electron effective mobility  $\mu_n$  is around 370 cm<sup>2</sup>/V·s at low  $V_g - V_{th}$  bias at room temperature and decreases with increasing  $V_g$ , and increases with increasing temperature (240–332K). It is very different from the case of Si n-MOSFETs, where the electron mobility decreases with increasing temperature. The low channel effective mobility and the ab-normal temperature dependence of  $\mu_n$  are ascribed to the high acceptor interface trap and border trap energy densities in the conduction band energy of InGaAs. The ballistic channel resistance  $R_{Ball}$  at low  $V_{ds}$  is calculated and compared with the measured channel resistance  $R_{CH}$ . The low transmission coefficient  $T = R_{Ball}/R_{CH} \approx 0.06$  to 0.05 indicates that there is a large room to improve the InGaAs/Al<sub>2</sub>O<sub>3</sub> n-FinFET performance.

**Index Terms**—Al<sub>2</sub>O<sub>3</sub>, FinFETs, InGaAs, mobility, nano scale transistor, quasi-ballistic transport.

## I. INTRODUCTION

INGAAS has high bulk electron mobility [1] and the potential to replace the conventional Si for the channel material in n-MOSFETs for low power low voltage logic applications [2]–[4]. However, the channel mobility in MOSFET is very different from the bulk mobility [5]. Particularly, it is size and structural dependent when the device is scaled down to the nanosize, due to the more severe effect related to the surface or interface scattering mechanisms [6], [7]. Therefore, it is highly desirable (however is lack of existing work) on reliable channel mobility extraction directly from nanoscale InGaAs n-MOSFETs. In this study, based on the quasi-ballistic transport theory of nano MOSFETs by Lundstrom's group [8], [9], we have developed a compact set of equations for physical characterization of quasi-ballistic transport and channel electron effective mobility  $\mu_n$  in

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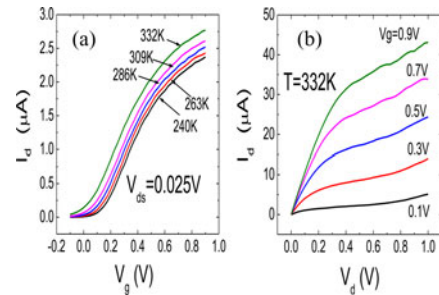


Fig. 1. (a)  $I_d$ - $V_g$  curves of In<sub>0.57</sub>Ga<sub>0.47</sub>As n-FinFET with channel length  $L = 100$  nm, Fin width  $W_{Fin} = 40$  nm, Fin Height  $H_{Fin} = 40$  nm, at different temperature. (b)  $I_d$ - $V_d$  curves of the same device. The curves are measured by Agilent 4156 and after source-drain resistance correction [10].

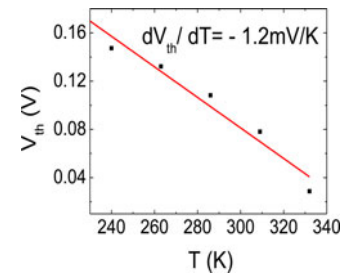


Fig. 2.  $V_{th}$  versus temperature of In<sub>0.57</sub>Ga<sub>0.47</sub>As n-FinFET with  $L = 100$  nm.  $dV_{th}/dT \approx -1.2$  mV/T.

the In<sub>0.53</sub>Ga<sub>0.47</sub>As n-FinFET with fin width  $W_{Fin} = 40$  nm, fin height  $H_{Fin} = 40$  nm, and channel length  $L = 100$  nm, and with 5 nm ALD Al<sub>2</sub>O<sub>3</sub> gate dielectric thickness. The detailed device structure and fabrication process were described in [4].

## II. EXPERIMENTAL DATA AND THE MOBILITY EXTRACTION ALGORITHM

Figs. 1 and 2 show the experimental  $I_d$ - $V_g$  and  $I_d$ - $V_d$  curves and the temperature dependence of the threshold voltage  $V_{th}$  of the In<sub>0.53</sub>Ga<sub>0.47</sub>As n-FinFET, measured by Agilent 4156 and after source-drain resistance correction [10] in the temperature range of 240–332 K.

For one subband electrons, the  $I_d$ - $V_g$  equation in the low  $V_{ds}$  region in [8] can be expressed by

$$I_d \approx \frac{1}{L} \left[ \frac{1}{\mu_n} + \frac{1}{\mu_{Ballistic}} \right]^{-1} Q_n V_{ds} \quad (1)$$

Different from the conventional 2-D area charge density description as in [1], [8], in (1), we introduce the 1-D line density of mobile charge  $Q_n$  along the channel direction at the top of the source-channel barrier.  $\mu_n$  and  $\mu_{Ball}$  are the diffusive mobility and ballistic mobility, respectively. In the Boltzmann distribution case, from the well-known relationship between

the electron mean free path  $\lambda_n$  and the mobility  $\mu_n$  and the diffusion coefficient  $D_n$  derived by Shockley [11], the diffusive

mobility:

$$\mu_n = \frac{q}{k_B T} D_n = \frac{q}{k_B T} \left[ \frac{v_T \lambda_n}{2} \right]. \quad (2a)$$

Here  $q$  is the absolute value of the electron charge,  $v_T$  is the electron thermal velocity

$$v_T = \sqrt{\frac{2k_B T}{\pi m_n^*}}$$

where  $m_n^*$  is the electron effective mass of In<sub>0.53</sub>Ga<sub>0.47</sub>As (= 0.043 $m_0$ ) [12]. Extend to the Fermi–Dirac distribution for one subband case, the following equation can be obtained [8]:

$$\mu_n = \frac{qv_T \lambda_n}{2k_B T} \left[ \frac{F_{-1/2}(\eta_F)}{F_0(\eta_F)} \right]. \quad (2)$$

Here,  $F_j(\eta_F)$  is the  $j$ th-order F-D integral [13],  $\eta_F = (E_F - E_s)/k_B T$ ,  $E_s$  is the bottom energy of the subband.

The ballistic mobility  $\mu_{Ball}$  is first introduced by Shur in the Boltzmann distribution case [14], and later extended to the Fermi–Dirac distribution case by Lundstrom *et al* [8]

$$\mu_{Ballistic} = \frac{qv_T L}{2k_B T} \left[ \frac{F_{-1/2}(\eta_F)}{F_0(\eta_F)} \right]. \quad (3)$$

The following two issues should be carefully considered for reliable mobility extraction.

1) In In<sub>0.53</sub>Ga<sub>0.47</sub>As n-FinFET with 40-nm fin width, the quantum confinement induced energy lifts for the electron subbands  $E_c - E_s^i$  are very small (quasi-classic).  $E_s^i$  is the bottom energy of the  $i$ th subband. For a very rough approximation of an infinitely high barrier square quantum well,  $E_c - E_s^1$  is only  $(\pi\hbar)^2/2m_n^* W_{Fin}^2 = 5.5$  meV for the first subband. When increasing  $V_g$ , the number of occupied subbands increases and (1) to (3) should be extended to include multiple subbands.

2) The charge density  $Q_n$  cannot be estimated by the conventional experimental method by measuring the gate capacitance versus  $V_g$  [5]. The gate capacitance cannot be accurately measured because of the high density of interface traps induced dispersion [15] and very small gate area of the FinFET, and can only be estimated by careful simulation. The 1-D line density of gate capacitance  $C_G = dQ_n/dV_g$  corresponding to the 1-D charge density  $Q_n$  is introduced. If the low doping acceptor charge in the fin body under volume inversion is neglected,  $C_G$  consists of two components in series. The first component is the oxide capacitance 1-D line density

$$C_{OX} = \frac{\kappa\epsilon_0}{t_{ox}} (W_{Fin} + 2H_{Fin}) = (14.2 fF/\mu m^2) (W_{Fin} + 2H_{Fin}) \quad (4a)$$

where  $\kappa = 8$  is the dielectric constant of Al<sub>2</sub>O<sub>3</sub> [16],  $\epsilon_0$  is the permittivity of vacuum, and  $t_{ox} = 5$  nm is the physical thickness of the dielectric. For Fin body with  $W_{Fin} = H_{Fin} = 40$  nm  $\gg$  dielectric thickness 5 nm, (4a) is a good approximation for  $C_{OX}$ .

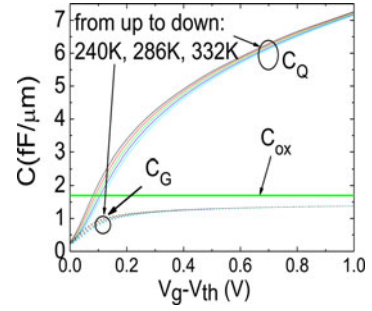


Fig. 3. Simulation results of 1D  $C_Q$  and  $C_G$  versus  $V_g - V_{th}$  at different temperature by using (11)–(13). The gate oxide 1-D capacitance  $C_{OX}$  (5 nm thick Al<sub>2</sub>O<sub>3</sub> with dielectric constant = 8, Fin width  $W_{Fin} = 40$  nm, Fin Height  $H_{Fin} = 40$  nm) is also shown as reference.

The second component is the quantum capacitance (inversion capacitance) 1-D line density  $C_Q = dQ_n/dV_Q$  here  $dV_Q$  is the Fin inversion potential change under volume inversion induced by the change of gate voltage  $dV_g$ . According to [17] and under volume inversion, we can estimate the one subband quantum capacitance 1-D line density to be

$$C_Q(\text{one subband}) = (q^2 m_n^* / \pi \hbar^2) H_{Fin} = (28.7 fF/\mu m^2) H_{Fin} \quad (4b)$$

which is comparable with the value of  $C_{OX}$ . The multiple subband quantum capacitance  $C_Q$  is a function of  $V_g$  (see (12) and Fig. 3), also comparable with  $C_{OX}$ .

Keeping points (I) and (II) in mind, we have extended (1)–(3) to a generic and compact set of (5)–(13) for multiple subbands quasi-ballistic transport in nanoscale FinFETs (or nanowire MOSFETs) in the linear  $V_{ds}$  region.

According to the similar method in [8], the 1-D  $Q_n$  can be expressed by

$$Q_n = \sum_i Q_i \approx q N_{2D} H_{Fin} \sum_i F_0(\eta_F^i) \quad (5)$$

$$N_{2D} = \frac{m_n^* k_B T}{\pi \hbar^2}. \quad (5a)$$

Extending  $I_d$  in (1) to the multiple subbands case in the low  $V_{ds}$  region, and combining (2), (3), and (5)

$$\begin{aligned} I_d &\cong \frac{1}{L} \sum_i \left[ \frac{1}{\mu_n^i} + \frac{1}{\mu_{Ballistic}^i} \right]^{-1} Q_i V_{ds} \\ &\approx \left[ \frac{H_{Fin}}{L} \right] \left[ \frac{qv_T}{2kT} \right] \left[ \frac{1}{\lambda_n} + \frac{1}{L} \right]^{-1} V_{ds} q N_{2D} \sum_{i=1}^n F_{-1/2}(\eta_F^i). \end{aligned} \quad (6)$$

Introducing the 1-D channel resistance  $R_{CH}$  and using (5) (6)

$$\begin{aligned} R_{CH} &= \left[ \frac{V_{ds}}{I_d} \right]_{V_{ds} \rightarrow 0} = L \left[ \frac{1}{Q_n \mu_{Ball}} + \frac{1}{Q_n \mu_n} \right] \\ &= R_{Ball} + R_{diffusive}. \end{aligned} \quad (7)$$

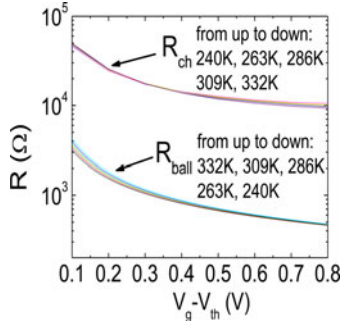


Fig. 4. Calculated  $R_{\text{Ball}}$  and measured  $R_{\text{CH}}$  for  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  n-FinFET with channel length  $L = 100$  nm, Fin width  $W_{\text{Fin}} = 40$  nm, Fin Height  $H_{\text{Fin}} = 40$  nm. The transmission coefficient  $T = R_{\text{Ball}}/R_{\text{CH}}$  is around 0.06–0.05 for these curves.

Here the ballistic and channel mobilities are

$$\mu_{\text{Ball}} = \frac{qv_T L}{2k_B T} \left[ \frac{\sum_i F_{-1/2}(\eta_F^i)}{\sum_i F_0(\eta_F^i)} \right] \quad (8)$$

$$\mu_n = \frac{qv_T \lambda_n}{2k_B T} \left[ \frac{\sum_i F_{-1/2}(\eta_F^i)}{\sum_i F_0(\eta_F^i)} \right]. \quad (9)$$

Here  $\eta_F^i = (E_F - E_s^i)/k_B T$ . (7) indicates that the channel resistance  $R_{\text{CH}}$  consists of two components in series. In the ballistic limit when  $L \ll \lambda_n$ , there is only the first term  $R_{\text{Ball}}$  with ballistic electron mobility  $\mu_{\text{Ball}}$ .  $R_{\text{Ball}}$  is independent of  $L$ , originated from the quantum contact resistance [18]. In the diffusive limit when  $L \gg \lambda_n$ , there is only the second term  $R_{\text{diffusive}}$  with conventional channel electron mobility  $\mu_n$ , and (7) is reduced to the long channel  $I_d$ - $V_g$  equation [1].  $Q_n$  and  $C_Q$  can be obtained by (10) to (13):

$$Q_n = \int_{V_g} C_G(V) dV = \frac{qm_n^* kT H_{\text{Fin}}}{\pi \hbar^2} \sum_i F_0(\eta_F^i) \quad (10)$$

$$C_G(V) = \frac{C_{\text{OX}} C_Q}{C_{\text{OX}} + C_Q} \quad (11)$$

$$C_Q = H_{\text{Fin}} \sum_i \frac{q^2 m_n^*}{\pi \hbar^2} F_{-1}(\eta_F^i). \quad (12)$$

The relationship between  $V_g$  and  $\eta_F^1$  can be obtained by the following consideration. Since a change in the gate voltage  $dV_g$  induces a change in the Fin inversion potential  $dV_Q$  by  $dV_g/dV_Q = C_Q/C_G$ , we can derive

$$V_g(\eta_F^1) - V_{\text{th}} = \int_{\eta_F^1}^{\eta_F^1} \frac{C_Q kT}{q C_G} d\eta_F \quad (13)$$

where  $\eta_F^1$  in (13) is the  $\eta_F^1$  value corresponding to  $V_g = V_{\text{th}}$ , and can be estimated by (10) with mobile charge area density  $= 10^{11} \text{ cm}^{-2}$  [19]. The calculated  $C_G$  versus  $V_g$  is shown in Fig. 3.

The calculated results of  $R_{\text{Ball}}$  in (7) are shown in Fig. 4. It is the typical ballistic limit of the channel resistance of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  n-FinFET. The measured channel resistance  $R_{\text{CH}} = [V_{ds}/I_d]_{V_{ds} \rightarrow 0}$  obtained from the experimental data of  $I_d$ - $V_g$  curves in Fig. 1 is also shown in Fig. 4 for comparison.

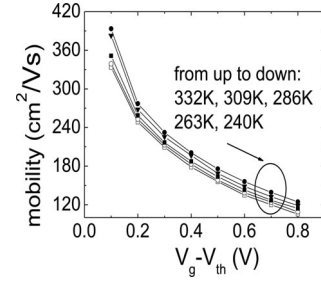


Fig. 5. Electron channel effective mobility  $\mu_n$  of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  n-FinFET with  $L = 100$  nm at different temperature 240–332 K versus  $V_g - V_{\text{th}}$ .

The transmission coefficient  $T$  of the flow of electrons [18] in low  $V_{ds}$  can be expressed by

$$T = \frac{\lambda_n}{\lambda_n + L} = \frac{R_{\text{Ball}}}{R_{\text{CH}}} \quad (14)$$

where  $T$  is related to the backscattering (or reflection) coefficient  $r$  by  $T = (1-r)$  [18], [8], [9]. From the curves in Fig. 4,  $T$  is estimated to be around 0.06–0.05 only. It indicates that there is still a large room to be improved for the present fabrication technology, as will be further discussed later.

### III. DISCUSSION

From the data in Fig. 4 and  $Q_n$  calculated by using (10)–(13), the channel electron mobility  $\mu_n$  can be obtained from (7). The results are plotted in Fig. 5. There are two points worth to be mentioned for the results in Fig. 5. 1) The overall channel mobility  $\mu_n$  in the  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  n-FinFET is quite low. 2) The  $\mu_n$  increases with increasing temperature, in contrast with the case in Si planar n-MOSFETs where  $\mu_n$  decreases with increasing temperature at moderate surface field due to the phonon scattering [5].

These ab-normal mobility characteristics are ascribed to the high density of acceptor like interface traps [15], [20] and border traps [21], [22] in the conduction band of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  in the  $\text{InGaAs}/\text{Al}_2\text{O}_3$  n-MOSFETs. The high densities of acceptor interface traps and border traps may response to the charge density estimated by (10) and (13). As a result, the real mobile charge density and the measured  $I_d$  are reduced. In the discussion of high- $k$ /metal gate Si n-MOSFETs, Zhu *et al.* [23] have developed a method of correction to estimate the real mobile charge density out of high density of interface trap charge. The real mobility extracted by their method after correction is much higher than the effective mobility extracted by the conventional method [5], [24]. However, this higher real mobility actually is not beneficial to higher  $I_d$ . In our work, we would rather follow the conventional mobility studies [5], [24], [25] and ascribe the degraded effective mobility extracted by (7) to (13) to the existence of high density interface traps and border traps [26]. The charged interface traps and border traps not only reduce the mobile charge density at fixed  $V_g$ , but also induce Coulomb scattering associated with a Coulomb scattering mobility component  $\mu_{\text{Coulomb}}$ , which increase with increasing temperature [1]. It is consistent with our experimental result. The results shown in Fig. 4 indicate that there is a large room to improve the present



InGaAs n-FinFET fabrication technology. The first way to improve the transmission coefficient  $T$  is obviously to reduce the channel length  $L$ . The more difficult task to improve  $T$  is to improve the InGaAs/dielectric interface to reduce the acceptor like interface trap and border trap energy densities in the InGaAs conduction band [15], [20], [21], [22]. On the other hand, the scattering mechanism and the ab-normal temperature dependence of effective mobility  $\mu_n$  need more deep investigation and understanding to further improve the electric performance of the nano-InGaAs n-FinFETs.

#### IV. CONCLUSION

The quasi-ballistic transport and the effective electron mobility  $\mu_n$  of In<sub>0.53</sub>Ga<sub>0.47</sub>As n-FinFET are investigated, based on the multiple subband quasi-ballistic theory and the experimental measurements on the FinFET devices with 100-nm channel length reported in [4]. The extracted  $\mu_n$  is quite low, around 370 cm<sup>2</sup>/V·s at room temperature at low  $V_g - V_{th}$  bias and decreases with increasing  $V_g$ , and increases with increasing temperature (240–332 K), in contrast with the case of planar Si n-MOSFET where  $\mu_n$  decreases with increasing temperature. The ballistic channel resistance  $R_{Ball}$  at low  $V_{ds}$  is calculated and compared with the measured channel resistance  $R_{CH}$ . The ab-normal mobility characteristic is ascribed to high densities of acceptor interface traps and border traps in the energy range of InGaAs conduction band. The low transmission coefficient  $T = R_{Ball}/R_{CH} \approx 0.06$  to 0.05 indicates that there is large performance room to be improved when the InGaAs/dielectric interface traps and border traps can be significantly reduced.

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Authors' photographs and biographies not available at the time of publication.