Origin and Implications of Hot Carrier Degradation of Gate-all-around nanowire III-V MOSFETs

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***Abstract* – Although ultra-scaled III-V Gate-all-around (GAA) nanowire (NW) MOSFETs have been studied for their immunity to short channel effects, the degradation mechanisms, such as, hot carrier injection (HCI) in the NW MOSFETs are yet to be studied systematically. In this paper, we examine how HCI affects the NW device performance (ΔV_{th}, ΔSS in both stress and recovery) at different bias conditions, and demonstrate that, unlike positive bias temperature instability (PBTI) in NMOS transistors, the HCI degradation is dominated by charge trapping. We analyze the implications of spatial charge trapping on device performance through experiments and simulation. We find that the distinctive features of HCI degradation of GAA NWs structure can be consistently interpreted by a Sentaurus™-based TCAD simulation.**

[Keywords: multi-gate FET, Gate-all around nanowire MOSFET, reliability, hot carrier, interface charge, charge trapping]

I. Introduction

The continued scaling of modern MOSFETs has increased both the packing density and the speed of modern ICs. However, the reduction of channel length below a critical dimension often leads to a commensurate increase in the short channel effects (SCEs), such as drain-induced barrier lowering (DIBL) [1]. A number of technologies, such as, Silicon-On-Insulator (SOI) and multi-gate device structures (e.g., FINFET) have been introduced to improve gate control and suppress SCEs [2]. Among them, Nanowire (NW) Gate-all-around (GAA) MOSFET is considered a leading candidate to address the scaling challenges below 20nm technology nodes, because of its excellent SCE immunity and low source-drain leakage current. With a number of high-mobility n-channel InGaAs NWs configured in parallel, such GAA transistors can already satisfy the target ITRS requirement for the ON current, with excellent on-off ratio [3, 4].

With the performance and scalability of GAA technology assured, the obvious next concern is the variability and reliability associated with such a transistor technology. For example, any process or stress induced variation of the threshold voltage (V_{th}), contact resistances, or mobility may be reflected in the degradation in the subthreshold slopes, reduction of ON-current, or increase in the off-state leakage. The surround-gate technology makes heat dissipation difficult [5], and this self-heating may degrade PBTI and TDDB performances, because these degradation processes are exponentially sensitive to operating temperature [6]. Apart from self-heating, the geometry and reduced cross-section of the NW transistors are expected to increase NBTI and HCI degradations [7]. The radiation susceptibility of the finite-volume NWs has been discussed [8], but not in the specific context of GAA NW technology with multiple NWs in a parallel configuration. To sum, therefore, the improved electrostatic control of reduced cross-sectional GAA NW transistors must be analyzed in the context of a new class of device-specific reliability concerns, so as to evaluate the full potential of the transistor technology.

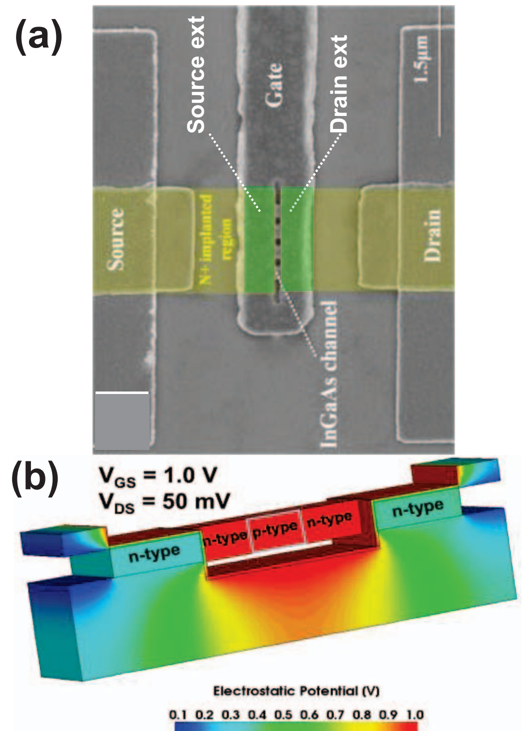

Fig. 1: (a) SEM image of top view of a NW GAA InGaAs n-MOSFET. Entire NW region (both source/drain extension and channel) are controlled by a gate bias. (b) Simulated potential profile of the MOSFET.

In this paper, we explore the physics of the hot carrier degradation (HCI) in GAA transistor technology. In long channel planar MOSFETs, the maximum HCI degradation occurs at $V_{GS} \sim V_{DS}/2$, because while the electron flux increases with V_{GS}, the energy of the electrons decreases with (V_{DS}-V_{GS}), so that the energy-flux is maximized halfway in between, at the specific gate-drain voltage combination [9-12]. The majority of the HCI research dates back to 1980s, because since then the scaling of the operating voltage (V_{DD}) has removed HCI as a primary concern for logic transistors [13, 14]. Unfortunately, one cannot continue scaling V_{DD} in the same proportion to the channel length, therefore, the high electric field of the surround gate technologies, coupled with high density of carriers in these transistors, suggest the reemergence of HCI as an important reliability concern for the sub-20 nm transistors. In this case, $V_{GS} \sim V_{DS}$ bias characterizes the maximum damage condition, where trapping of hot electron and kinetic dissociation of Si-O bonds by hot electrons dictate HCI degradation [15-18]. The issue is further complicated by the significant ON-state self-heating of the GAA transistors and III-V/high-k gate stack which affects the HCI performance in a complex way [19, 20]. Therefore, it is important to explore the physics, kinetics, and projected lifetime associated with HCI degradation of III-V GAA transistors within a comprehensive experimental and modeling framework. (Fig. 1a, b) [21]. It is likely that the conclusions we reach for the III-V GAA technology would be general, and therefore, would apply to other ultra-scaled, parallel array, surround gate technologies, such as, FINFET or Omega FET, etc.

In this paper, we

(i) Examine how hot carrier injection (HCI) affects NW device performance (ΔI_{OFF}, ΔI_{ON}, ΔV_{th}, ΔSS in both stress and recovery) at different bias conditions;

(ii) Determine the density of interface charge created by HCI degradation by measuring changes in subthreshold slope and 1/f noise;

(iii) Verify (by comparing with PBTI results) that charge trapping is the dominant mechanism on HCI degradation; and

(iv) Analyze the implications of localized trapping on device performance by inverting the source-drain configuration.

This article, therefore provides a broad physical understanding of HCI degradation of the GAA NWs transistor technology and we interpret the physical origin of these features by Sentaurus-based TCAD simulation.

II. Hot Carrier Injection Degradation

Device Configuration. The fabrication process of the InGaAs GAA n-MOSFET NW transistors is described in [22-25]. In this structure (Fig. 1a), implant-defined variable channel length devices (L_{CH} = 30~80nm) are embedded within fixed length NWs (L_{NW} = 200nm), so that the source/drain extension lengths ($L_{S,ext}/L_{D,ext}$) are defined by $L_{NW} = L_{S,ext} + L_{CH} + L_{D,ext}$. The entire NW region is covered with gate oxide layer (Al_2O_3), with EOT~1.7nm.

Device Simulation. The Sentaurus-based TCAD simulator is used to solve the three-dimensional (3D) electrostatic potential and the charge density. The self-consistent simulation allows us to get the energy band-diagrams and currents for different combinations of gate and drain bias. To simulate the effects of charge trapping following the HCI stress, localized fixed charges are incorporated in the Poisson equation to explore the implications of HCI degradation on the I-V characteristics of GAA transistors.

The simulation model is based on device geometry and doping densities obtained from the experimental data. $In_xGa_{1-x}As$ band-gap is assumed to be 0.63 eV, corresponding to the Indium-mole-fraction of x=0.65. We have used field dependent mobility model were used for both carriers; the I_D-V_{GS} characteristics are well matched with a peak electron mobility of 70 cm^2/V-S.

The 3D potential profile, associated with the ON-state of the transistor, is shown in Fig. 1b. Specifically, note that the gate voltage (V_{GS}) controls the entire NW region, *including the channel and source/drain extension regions*.

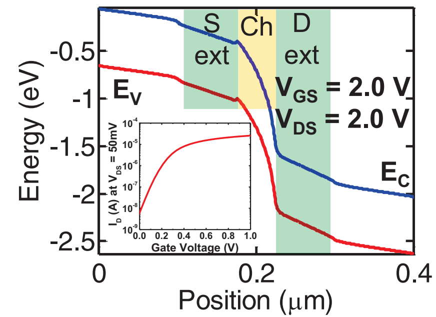

Fig. 2: The band diagram for the MOSFET in HCI stress condition (V_{GS} = 2.0V and V_{DS} = 2.0V).The source/drain extension region are defined in Fig. 1a. The inset shows I_D-V_{GS} at V_{DS} = 50mV.

Fig. 2 shows the 1D band diagram under HCI condition ($V_{DS} = V_{GS} = V_{DD}$); it is easy to see that the maximum energy drop occurs near the edge between channel and drain extension. The TCAD model is well-calibrated and can reproduce the full range of I_D-V_{GS} characteristics as a function of operating conditions and transistor dimensions (Fig. 2, inset).

HCI degradation Characterized by SS-slope and Noise Measurements. The HCI measurements are done with an automated measure-stress-measure (MSM) setup at various bias conditions. The full transfer characteristics are obtained during each measurement step. A broad range of devices with different channel widths (W_{CH}) and lengths (L_{CH}) were used for this study. In order to examine the dynamics of interface trap generation (N_{it}) during the HCI, we measured the subthreshold slope (SS) and calculated N_{it} (Fig. 3a) [26] by the textbook formula.

$$SS = (ln10)\left(\frac{k_B T}{q}\right)\left(1 + \frac{C_{dep} + C_{it}(\psi_s)}{C_{ox}}\right), \quad (1)$$

where, C_{ox}, C_{dep}, C_{it} (= $q \times N_{it}$) are oxide, depletion, trap capacitances, respectively. The absence of a body contact preclude the use of more sophisticated N_{it} characterization techniques, such as Charge-Pumping measurements [27, 28]. As shown Fig. 3a, we observe generation and relaxation of N_{it} during the 10^4 sec stress and 10^4 sec recovery phases. The results show that N_{it} increases to as much as 9×10^{12} $eV^{-1}cm^{-2}$.

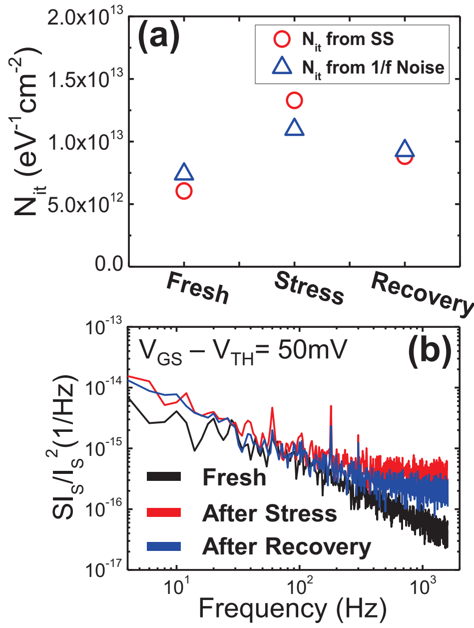

Fig. 3: (a) Characterization of N_{it} values before/after HCI stress (10^4s) and recovery (10^4s) with $V_{GS} = V_{DS} = 2.0$V by SS and noise measurement. N_{it} changes depending on the HCI is observed. (b) 1/f noise measurement data. Power of noise spectra (SI_S) is normalized by I_S^2 at $V_{GS} - V_{th} = 50$mV.

As shown Fig. 3a, we observe generation and relaxation of during stress, and a substantial fraction of the defects recover during the relaxation phase. Additionally, in order to confirm the N_{it} value, 1/f noise power spectrum density is measured at each phase as shown in Fig. 3b and N_{it} is extracted using unified noise model [29] as shown below:

$$S_{I_s}/{I_s}^2 = k_B T N_{it}/f\gamma N^2 r_{nw} L_{CH}. \quad (2)$$

The N_{it} obtained from noise-measurements (blue triangles) are generally consistent with those obtained for the SS-degradation.

Time-dependent V_{th} degradation. Fig. 4a shows the experimental results of the shift in V_{th} as a function of the V_{GS} for a fixed V_{DS} = 2V. V_{th} values are extracted by a linear extrapolation of the g_m-V_{GS} from the full transfer characteristics [30]. We find that the degradation increases substantially beyond a critical voltage of V_{GS}=1.6 V and maximizes close to V_{GS}~V_{DS}. *The maximum HCI degradation close to V_{GS}~V_{DS} is consistent with other recent reports in the literature for short channel transistors* [31]. To understand the physical origin of this worst-case bias configuration, we calculate the maximum power density along the channel at different gate biases. Fig. 4c shows the simulated results for the electric field and the current taken at the maximum electric field location (at the edge between the channel and drain extension, as shown in blue circle in Fig. 4b. The channel hot electrons are affected by increasing V_{GS} in two ways, (a) an increase in the density of the hot carriers (I_D) as a function of applied bias (V_{GS}), and (b) a decrease in the electric field close to the channel-drain overlapped region. Indeed, hot carrier induced ΔV_{th} is strongly correlated to the power density of the hot carriers, (i.e., power density (MW/cm) = electric field (MV/cm) × current (A)) at the channel/drain extension junction. Therefore, the maximum damage occurs at V_{GS}~V_{DS}, where the localized power dissipation is maximized.

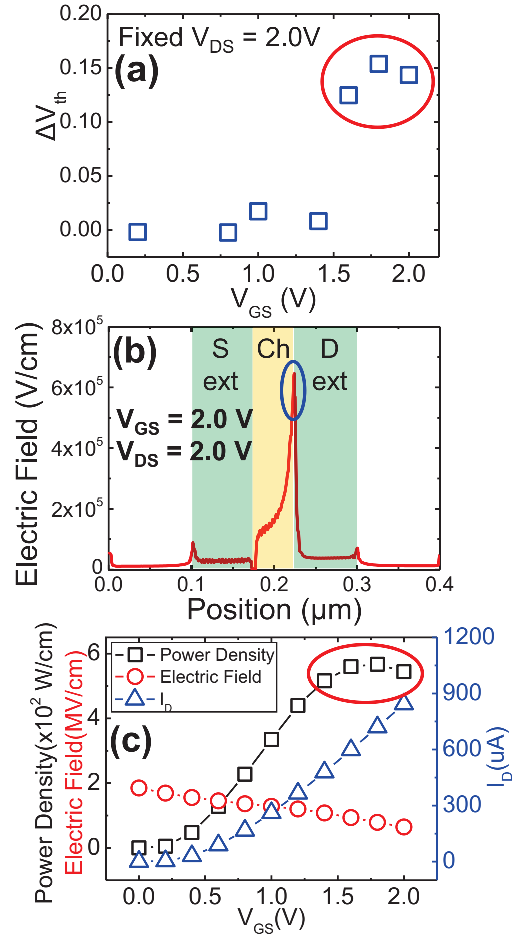

Fig. 4: (a) ΔV_{th} depending on V_{GS} with fixed V_{DS} = 2.0V. Maximum damage condition is V_{GS} ~ V_{DS}. (b) Electric field distribution along lateral NW under HCI condition ($V_{GS} = V_{DS} = 2.0$V). (c) At the edge between channel and drain extension, power density (black), electric field (red), and I_D (blue). The power density of the carrier = electric field obtained from blue circle in Fig. 4b × I_D.

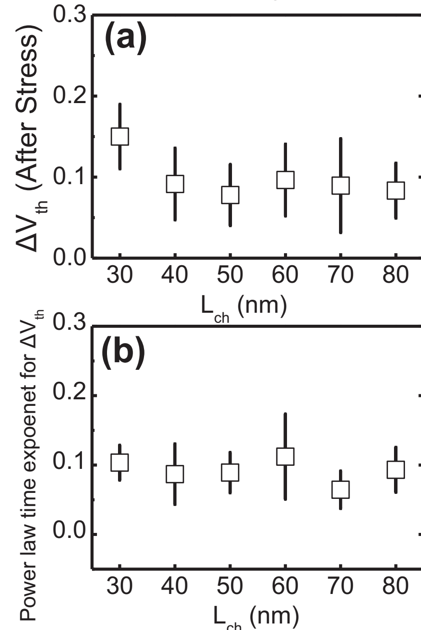

Fig. 5: (a) ΔV_{th} depending on channel length extracted from ΔV_{th} (10^1-10^4s). (b) Power law time exponent (n) of ΔV_{th} depending on channel length extracted from ΔVth (10^1-10^4s). In a wide range of channel length, ΔV_{th} is 0.1V and the time exponent (n) is 0.1 under HCI condition (V_{GS} =2.0V and V_{DS} = 2.0V)

Finally, we find that ΔV_{th}~100mV and the power law time exponent of ΔV_{th} ($\propto t^n$) lies within 0.08 ~ 0.11, following a 10^4s HCI stress at $V_{DS} = V_{GS} = 2V$. These values are robust across a broad range of devices with varying channel lengths and widths (Fig. 5a, b). It is interesting that ΔV_{th} does not show the characteristic inverse dependence on the length of the channel, but is relatively independent of L_{CH}. This feature may not be an intrinsic characteristic of the HCI degradation of GAA NW transistors, but is likely to be a consequence of the electric field profiles arising from the peculiar source-drain extension regions that bracket the actual channel, see Fig. 1b.

III. Dominant Mechanism for HCI

Let us now explore the dominant physical mechanism for HCI degradation, by comparing the process with PBTI degradation. After 10^4 seconds of HCI stress, we observe ΔV_{th} ~100 mV, characterized by power law time exponent n ~ 0.1. In contrast, PBTI degradation of the same transistor has ΔV_{th} comparable to HCI, but with considerably higher n ~ 0.15 [24]. The difference in *n* may be a consequence of different relative contributions of trapping (N_{ot}) and trap generation (N_{it}) for the two cases. In order to isolate the relative contributions, we examine the transient data (ΔI_{OFF}, ΔV_{th}, and ΔSS) for both stress and recovery cycles for PBTI and HCI stresses, respectively.

First, Fig. 6a shows that during the stress phase, ΔI_{OFF} *decreases* for HCI ($V_{GS} = V_{DS} = 2.0V$), but *increases* for PBTI ($V_{GS} = 1.8V$, $V_{DS} = 0V$). Here, I_{OFF} is defined at $V_{th} - 3/2 \times V_{DS}$. This suggests the increase (reduction) of the OFF state energy barrier from source to drain in the former (later) case. The increase of the energy barrier might be caused by the dominance of electron trapping (or, generation of acceptor type trap N_{IT} during the HCI stress. On the other hand, the reduction of the energy barrier during the PBTI stress has been previously attributed by the generation of donor type N_{IT} for the planar InGaAs devices [32].

In order to identify whether the electron trapping or the acceptor-type N_{it} generation causes the increase of the source to drain energy barrier for HCI, we look at the degradation rates, as shown in Fig. 6b. Note that, although ΔV_{th} are comparable for both HCI and PBTI for 10^4 sec of stress, ΔV_{th} under HCI stress shows faster initial degradation and smaller time exponent at the later part (n_{HCI}~0.1 and n_{PBTI}~0.15) as compared to PBTI. The degradation part is also shown in log-log scale for clarity see at Fig. 6c. A faster initial degradation of HCI stress compared to PBTI stress implies that electron trapping to the pre-existing bulk traps might be the dominant physical mechanism of the HCI degradation.

In order to confirm the above hypothesis, we refer to Fig. 6d, where we compare the time evolution of the degradation of the subthreshold slope for the two cases. Our results for GAA transistors show that $\Delta SS_{HCI} << \Delta SS_{PBTI}$ after each stress, as has been the case for InGaAs bulk planar MOSFETs [19]. Since ΔSS is attributed primarily to N_{it}, the results imply smaller $N_{it,HCI} << N_{it,PBTI}$. Taken together, we conclude the dominant degradation mechanism for HCI is due to electron trapping in pre-existing defects.

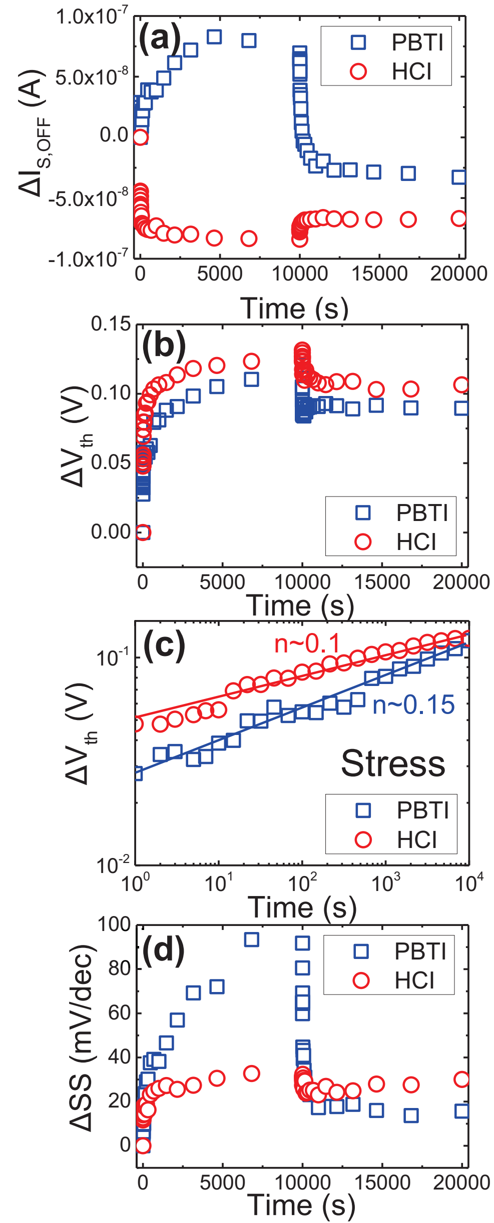

Fig. 6: (a) Time evolution of $\Delta I_{S,OFF}$ in HCI and PBTI stress (0-10_4s) & recovery (10^4-2×10^4s). $\Delta I_{S,OFF}$ has different signs for the two cases. (b) Time evolution of ΔV_{th} in HCI stress (0-10^4s) & recovery (10^4-2×10^4s). Initial increase in ΔV_{th} under HCI is much faster than ΔV_{th} under PBTI, suggesting the presence of trapping for the HCI. (c) Log scales of time evolution of ΔV_{th} in HCI stress (0-10^4s) in stress phase (d) Time evolution of ΔSS in HCI stress (0-10^4s) & recovery (10^4-2×10^4s). Initial increase in ΔSS under HCI is much smaller than ΔSS under PBTI.

It is noteworthy that, in PBTI, a large (~80 percent) recovery of ΔSS occurs after 10^4s of relaxation (Fig. 6d). In contrast, the recovery phase of ΔSS, following a HCI degradation, is limited to ~20 percent. The smaller portion of the recovery in HCI is consistent with the localized N_{it} generation at the channel/drain extension area as compared to the entire channel area in the PBTI case [7].

IV. Implication of the Spatially Localized Degradation

In section 2 we mentioned that the point of maximum power dissipation is close to the edge between the channel and the drain extension. Later in section 3, we found that the channel hot carriers are primarily injected into the oxide close to this HCI injection position and are trapped by the pre-existing defects. We have seen that in addition to the V_{th} shift, the trapping of hot electrons also increases the source to drain energy barrier, that is reflected in the reduced off current following the HCI degradation. Note that this increase of the barrier (damage region) should only occur at the HCI injection point (i.e., channel/drain extension interface).

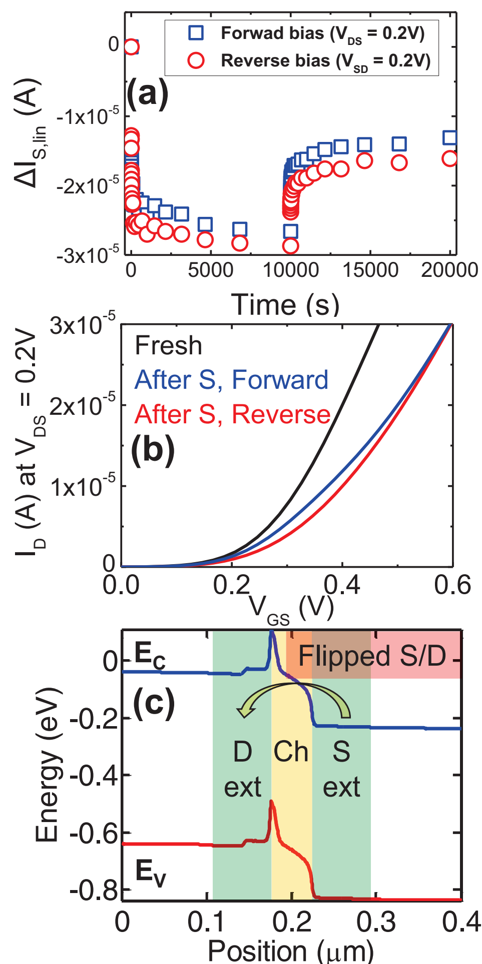

Fig. 7: (a) Time evolution of $\Delta I_{S,lin}$ in HCI stress (0-10^4s) & recovery (10^4-2×10^4s). Under HCI stress, $\Delta I_{S,lin}$ is measured at both forward operation (V_{GS} = 0.5V , V_{DS} = 0.2V) and reverse operation (V_{GS} = 0.5V , V_{SD} = 0.2V). (b) After HCI stress, simulated I_D-V_{GS} characteristic. The line for drain side trap (blue) is the forward operation and the line for source side trap (red) is reverse. (c) After interface charges build up, Simulated band diagram in reverse operation (V_{GS} = 0.5V, V_{SD} = 0.2V), Carrier faces large barrier early due to electron trapping.

In order to verify this hypothesis, we apply the HCI stress in a transistor in the normal way, but measure the ON current periodically for both forward (V_{DS} = 0.2V) and reverse (V_{SD} = 0.2V) configurations, while keeping the V_{GS} fixed at 0.5V. A barrier at the drain side would affect the reverse current (V_{DS} < 0) more strongly than the forward current (V_{DS} > 0), see Fig. 7c. Indeed, Fig. 7a shows that the reversed ON current is suppressed compared to the forward ON current, confirming that the continued electron trapping creates an increasing energy barrier at the drain side. The results from the TCAD simulation, shown in Fig. 7b, supports this assertion. In this simulation, an electron charge (= 9×10^{12} cm^{-2}) is placed close to the 'drain' side (forward) or the 'source' side (reverse). We find that I_{ON} is different depending on spatial location of the electron charge. Also, we can consistently confirm charge flows faces different magnitude of energy barrier from 1D band diagram in Fig. 7c. Therefore, it is confirmed that the spatial location of the electron trapping under HCI is nearby the channel-drain extention region.

V. Conclusion

In this paper, we have shown that the bias condition for the maximum damage by the HCI stress is V_{GS}~V_{DS} for InGaAs GAA NW structure. It is confirmed by several experiments (ΔI_{OFF}, ΔV_{th}, and ΔSS) that the dominant HCI degradation mechanism involves electron charge trapping. Finally, we verify spatial location of HCI damage is on channel-drain extension region by flipping the source-drain current. The experimental observations are supported by well-calibrated TCAD simulation. Remarkably, despite the dramatic difference in materials/geometry, it appears that the HCI degradation in GAA-NW is essentially classical, suggesting that HCI-reliability may not be a fundamental bottleneck for the adoption of GAA-NW as a sub-20nm technology.

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