Effects of Channel Hot Carrier Stress on III-V Bulk Planar MOSFETs

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***Abstract*—We performed channel hot carrier stress on enhancement-mode, inversion-type III-V MOSFETs with Al_2O_3 gate dielectric. The stress induces subthreshold swing degradation, increase on the threshold voltage and reduction of drain saturation current. Nonetheless, no appreciable transconductance degradation can be observed at least with a stress time as long as 10^5 s.**

Keywords-stress; III-V MOSFET; reliability; Hot Carrier Stress.

I. INTRODUCTION

As the Moore's law proceeds with its trends, new technologies are being investigated, to allow the increase of the transistor density [1-3]. One of the main problems of high-speed ULSI devices is the dynamic power dissipation, which depends on the square of the power supply voltage. On the other hand, in order to operate at high frequencies, the power supply voltage must be kept high enough to achieve a small dynamic ON-resistance value. However, the dynamic ON-resistance value not only depends on the power supply voltage, but also on the carrier mobility. For this reason, many efforts are currently being undertaken to find techniques or materials, which allow higher electron mobility than plain silicon. Among them, we can cite the use of intrinsic silicon, strain techniques and the employment of III-V high mobility semiconductors. The usage of III-V semiconductors seems a good choice for n-MOSFETs, as they allow for very high electron mobility values. High mobility MOSFETs permit to lower the supply voltages, reducing the power dissipation, while maintaining high speed capability.

In the past, MOSFETs based on III-V semiconductors were affected by many problems, mainly due to the Fermi level pinning, because of the lack of a good gate dielectric. In fact, the native oxide forms a very poor interface with the III-V semiconductor, resulting in extremely limited electrical performances [4-11]. Consequently, a lot of research has been carried out to find materials and deposition techniques to improve the interface quality [12]-[25].

Now, both flatband and inversion mode III-V MOSFETs allow to reach electron mobility exceeding 5000 $cm^2V^{-1}s^{-1}$ [17],[26],[27]. However, despite these improvements, III-V MOSFETs have still many open issues, such as very exacerbated short channel effects [28], which negatively impact on the static power consumption. Furthermore, the reliability of III-V MOSFETs is still a widely unexplored field.

In this work, we performed channel hot carrier (CHC) stresses on InGaAs inversion-type enhancement-mode MOSFETs. While the effects CHC stresses have been thoroughly studied on silicon MOSFETs [29]-[36], to our knowledge, this is the first work, which reports the effects of CHC stress on III-V MOSFETs.

This work is organized as follows: in Section II, we describe the devices and the experimental procedure; in Section III-A, we show and discuss the gate and drain current stress kinetics;

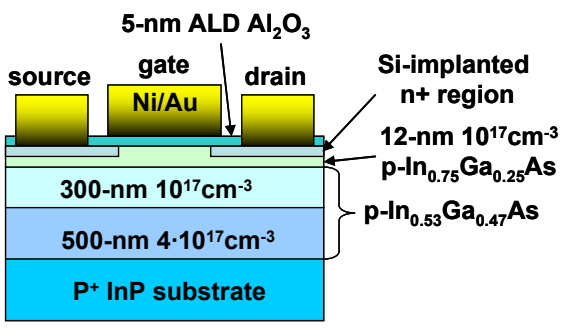

Figure 1. Cross section of the devices used throughout this work.

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in Section III-B, we discuss the impact on the electrical characteristics and the degradation kinetics on some important MOSFETs parameters; finally, in Section IV, we draw our conclusions.

II. Experimental and Devices

Throughout this work, we analyzed inversion-type enhancement-mode InGaAs with Al_2O_3 gate dielectric. Fig. 1 shows a schematic cross section of the analyzed devices. A 500-nm p-type $4\times10^{17}/cm^3$ buffer layer, a 300-nm p-type $1\times10^{17}/cm^3$ $In_{0.53}Ga_{0.47}As$ layer, and a 12-nm strained p-type $1\times10^{17}/cm^3$ $In_{0.75}Ga_{0.25}As$ channel were sequentially grown by molecular beam epitaxy over a p^+-InP substrate. The devices feature a 5-nm Al_2O_3 gate oxide, grown by ALD at 300°C, after $(NH_4)_2S$ surface treatment. For further details, the interested reader may refer to [28]. The MOSFETs feature a 250-nm gate length and a 5-µm channel width.

The procedure for the CHC stress is schematically shown in Fig. 2. The devices were initially characterized and they were subjected to a stress-characterization-relax-characterization loop, which lasted until a total cumulative stress time of 10^5s was reached. During each stress step, we applied a drain-to-source voltage double of the gate-to-source voltage ($V_{DS} = 2\cdot V_{GS}$), which also grants the lowest gate dielectric field along the whole channel length. In this way, electrons are strongly accelerated by the high drain to source electric fields and they become "hot".

The V_{DS} stress voltages were 2.5V, 2.6V, 2.7V and 2.8V. These values were empirically chosen to achieve a measurable degradation within the 10^5-s stress time. The low-field phase consists of a 200-s constant bias time, in which we monitor the gate current at V_{GS}=0.8V. In this way, we can identify if a permanent gate dielectric damage occurred. The 200-s relax phase was introduced to neutralize any unstably trapped charge, which may affect the first characterization performed after each stress step. During the relax phase, the gate was biased to -0.5V, while the other terminals were grounded.

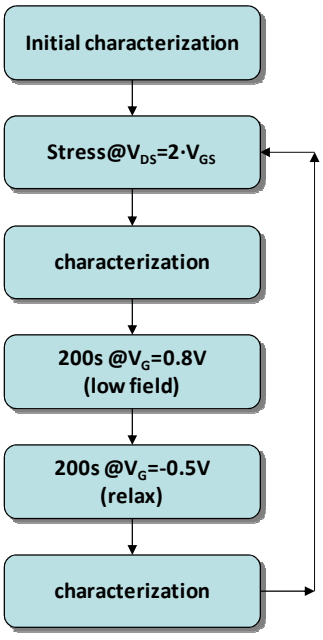

Figure 2. Experimental stress procedure used in this work.

III. Results and Discussions

A. Gate and drain currents stress kinetics

In Fig. 3, we plot the gate and drain current evolutions measured during the stress, performed with the lowest (V_{DS}=2.5V, see Fig. 3a) and highest (V_{DS}=2.8V, see Fig. 3b) stress voltages. Remarkably, the gate current is below 1pA in Fig. 3a for the whole stress duration ($V_{DS,stress}$=2.5V), but it features a noticeable increase after 2 hours when the higher V_{DS} stress voltage (2.8V, Fig. 3b) is employed. At the end of the stress of Fig. 3b, the gate current value exceeds 10nA, indicating that a soft breakdown occurred. The drain current decreases during stress, indicating that some degradation is occurring, likely due to stress induced interface traps, as we will discuss later. These traps, in turn, increase the subthreshold swing, thus the device threshold voltage increases, decreasing

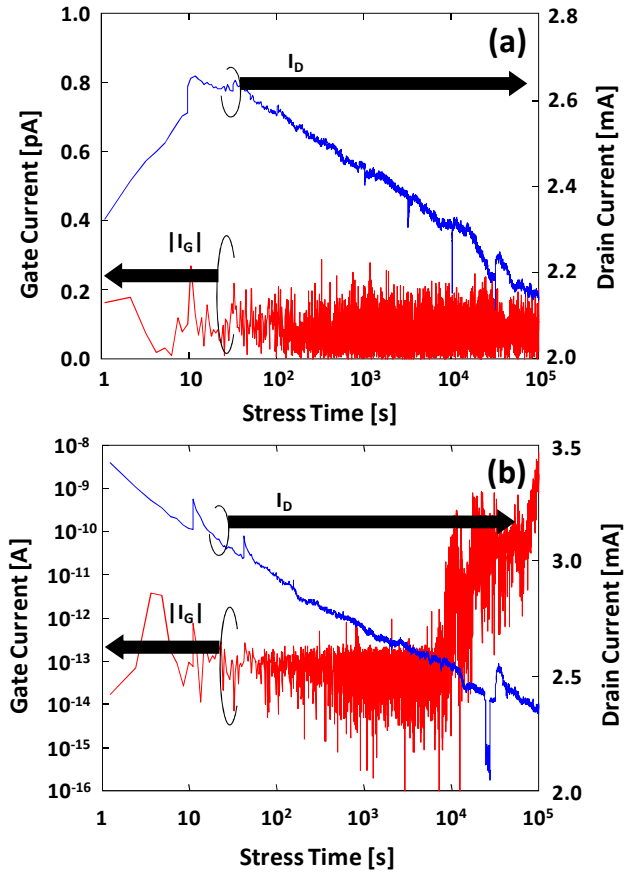

Figure 3. Evolution of the gate (red, left axis) and drain currents (blue, right axis) measured during the 2.5-V (a) and 2.8-V (b) V_{DS} stress. The relax and low-field phases are not shown here.

the drain current value. Similar behavior occurs when V_{DS}=2.7V (V_{GS}=1.35V). Instead, no noticeable gate current increase is observed before 10^5s if $V_{DS}\leq$2.6V ($V_{GS}\leq$1.3V).

Noticeably, the V_{GS} and $|V_{GD}|$ values are at most equal to 1.4V, corresponding to a gate dielectric field as low as 2.8MV/cm during the stress. Despite such a low field, dielectric (soft) breakdown occurred. It is interesting to compare this result with what we found in [37]-[38] with a staircase gate stress. In fact, in [37]-[38], dielectric breakdown occurred only when the gate-to-source voltage was higher than 3.8V, corresponding to a dielectric field almost 3 times higher. Also, other authors reported much higher Al_2O_3 breakdown fields [39]-[41]. Nonetheless, there are many differences with respect the previous works. In fact:

1) In [37]-[38], there was almost no drain-to-source current during the stress, while, in this work, a current as high as 3 mA flows through the channel, and hot electrons are generated (CHC stress). Hot electrons can damage the device near the drain if adequate countermeasures are not employed [31]-[34]. Furthermore, hot electrons might generate electron-hole pairs by impact ionizations. This is very likely because of the very narrow $In_{0.75}Ga_{0.25}As$ energy-gap (about 0.55eV). In this way, holes might be accelerated and induce damage near the source. In the literature there are some works on conventional silicon MOSFETs, which investigated the accelerated oxide breakdown induced by CHC [36]-[37]. In these works, the gate and drain bias voltages allowed not only hot carrier generation but also injection in the oxide, because the electron energy overwhelmed the conduction band offset, and there was a positive gate to drain voltage. In our case, the conduction band offsets are as small as 2.4eV [42], and with our V_{DS} values we can generate hot electrons with enough energy to overcome the barrier height at the interface. However, in this work, $V_G<V_D$, so injection of hot electrons is very unlikely, at least at the drain side.

Because of the relatively low thermal resistivity, we estimated that the temperature rise at the channel is very small, below 10°C, therefore we might exclude the temperature rise as main factor for the accelerated degradation phenomena.

2) In [37]-[38] the stress time was considerably shorter than that used in this work. Therefore, it's reasonable that much higher gate-to source voltages were required to induce a dielectric breakdown in such a short time.

3) The breakdown effects in this work are much less severe than those reached in [37]-[38]. This is not unexpected, as the electric field were much higher in [37]-[38], so catastrophic breakdowns are much more likely to occur. In contrast, we believe that few dielectric traps are generated in this work, thus the increased gate leakage arises from few percolation paths in the gate dielectric, and due to (multi-) trap assisted tunneling.

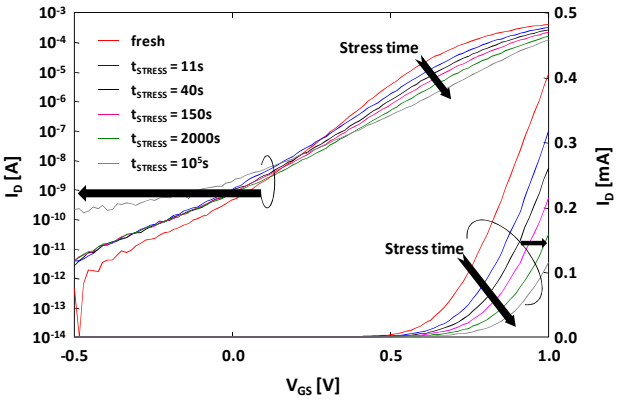

Figure 5. Samples of I_D-V_{GS} curves measured after the relax phases of the stress performed with V_{DS}=2.8V. For clarity, we only show the curves measured at selected intervals. In the same Figure, the currents are plotted in linear (right axis) and logarithmic (left axis) scale. These curves were taken with V_{DS}=200mV

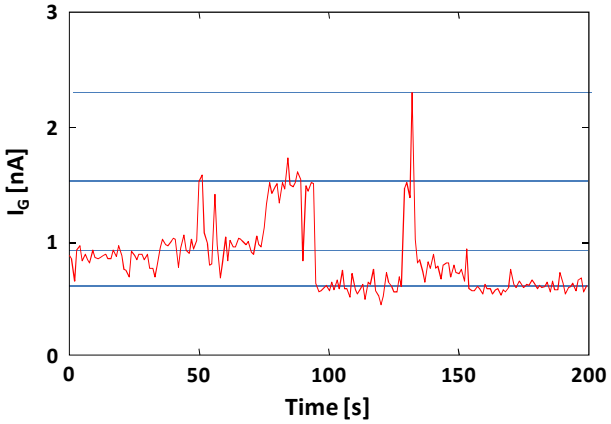

Figure 4. Gate current measured during the low-field phase after a breakdown occurred in stress performed at V_{DS}=2.7V. The gate current shows discrete level fluctuations, which we highlighted using horizontal lines.

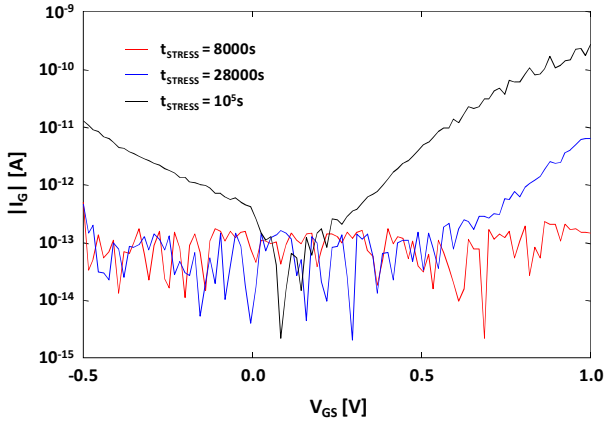

Figure 6. I_G-V_{GS} (taken with V_{DS}=200mV) at different stress times ($V_{DS,stress}$=2.8V). Before 8000s of stress time, the gate current is below 1pA. After 28000 s, a microbreakdown can be observed from the increased gate current.

This behavior is similar to conventional silicon MOSFETs subjected to constant current or constant voltage gate stress after soft-breakdown [43]. These gate currents are frequently characterized by multilevel random-telegraph-noise (RTN). In Fig. 4, we show an example of gate current evolution measured during the low-field phase at the end of the stress performed with V_{DS}=2.8V. Noticeably, discrete-level fluctuations can be observed, indicating that the gate leakage current indeed comes from few discrete traps in the gate dielectric.

B. Effects on the I-V characteristics and degradation kinetics

In Fig. 5 and 6 we plot some representative samples of I_D-V_{GS} and I_G-V_{GS} taken after various stress times. This device was stressed with V_{DS}=2.8V (V_{GS}=1.4V). The curves shown in Fig. 5 and 6, were taken with V_{DS}=0.2V. The most noticeable variations are:

1) The increase in the subthreshold slope.

2) The decrease of the drain current.

3) The increase of the gate current after the last steps on the device stressed with V_{DS}=2.8V.

From the curves measured after the relax phase of each stress step, we calculated the following parameters:

1) The subthreshold swing (S), shown in Fig.7.

2) The gate to source voltage required to achieve I_D=100μA, shown in Fig. 8, with V_{DS} = 0.2V

3) The saturation drain current with V_{GS}=V_{DS}=1V, shown in Fig. 9.

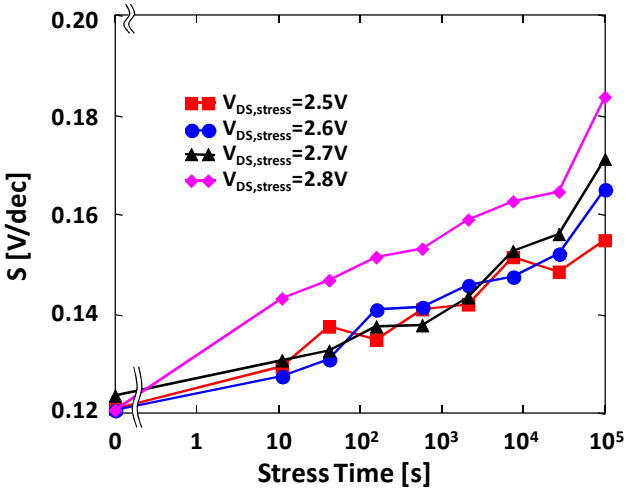

Figure 7. Evolution of the subthreshold swing (S) as a function of the stress time, for various stress voltages.

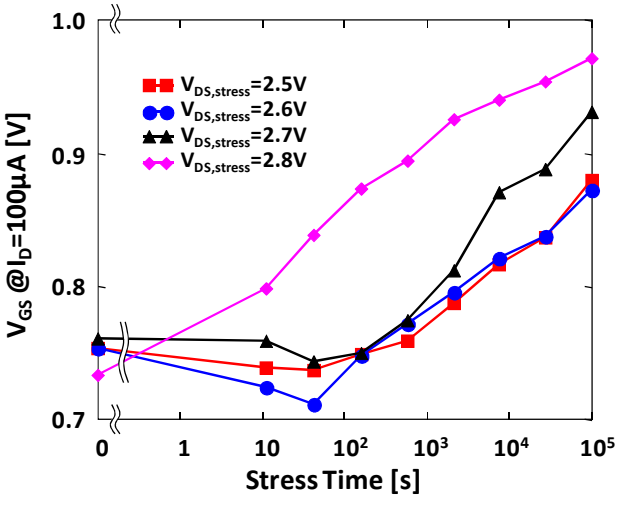

Figure 8. Evolution of the V_{GS} required to achieve I_D=0.1mA as a function of the stress time.

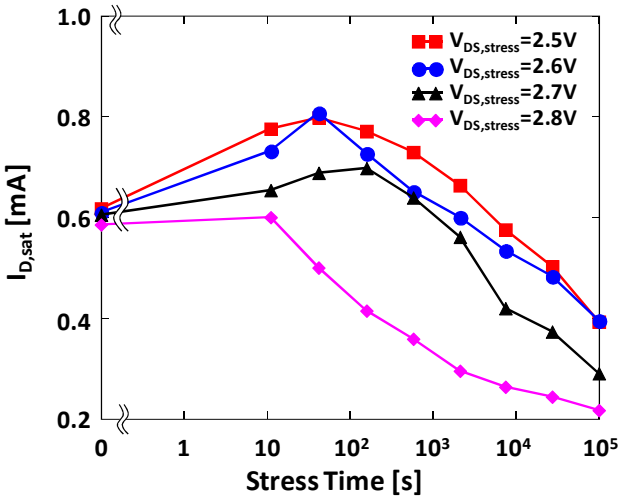

Figure 9. Evolution of the saturation drain current as a function of the stress time. After an initlai increase, the current constantly drops as the stress time increases.

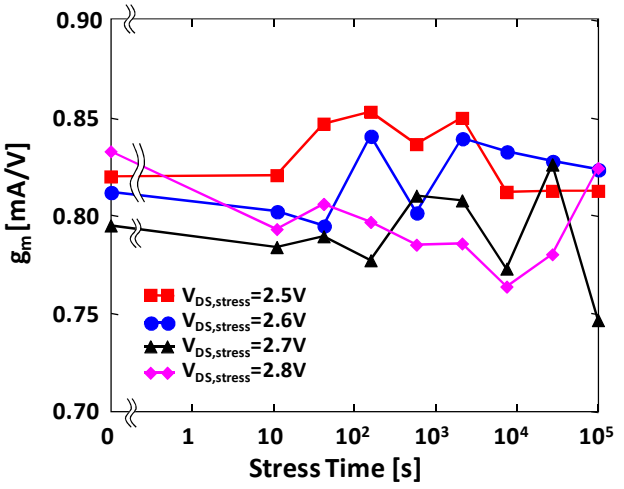

Figure 10. Evolution of the transconductance averaged between I_D=60 μA and I_D=100μA. The variations are below the measurement noise.

4) The average transconductance value (g_m) evaluated between I_D = 60μA and I_D = 100μA, shown in Fig. 10.

For each stress voltage value, in Figs. 7-10 we plotted the average values calculated from all the stressed samples.

As anticipated in the previous section, a soft breakdown occurred in some samples stressed at the higher voltages (2.7V and 2.8V). After breakdown, the gate current permanently increases and it becomes measurable even at V_{GS} values much smaller than the stress voltages. Noticeably, we found two different kinds of oxide breakdown, which we might tentatively ascribe to the different locations of the breakdown (near the source or near the drain). One (found on one device stressed with V_{DS}=2.8V, see Fig. 11a), likely occurred both at the drain and at the source, because there is a strong V_{DS} dependence on the I_G-V_{GS} curves. Furthermore, this is also confirmed by the I_G measured during stress, which becomes negative after 8200 s, indicating that, at the breakdown location, the gate has a lower voltage than the channel (the sign of I_G is not shown in Fig. 3). Another (found on one device stressed with V_{DS}=2.7V, see Fig 11b) likely experienced a breakdown only near the source, because the I_G-V_{GS} curves are symmetric with respect the origin and there is almost no dependence on V_{DS}. This is also confirmed by the positive I_G during the 2.7-V stress (not shown). As discussed above, the regions near the drain and source are most likely to experience the strongest degradation. In fact, with our setup, in the gate dielectric regions near the source and near the drain, the electric field is larger (with opposite polarity). Furthermore, energetic electrons (near the drain) and holes (near the drain) are present. It is also worth to remark that in [38] we found that the positive gate-bias induces breakdown earlier than negative-gate bias. This might explain why we found a breakdown at the drain only on devices stressed at V_{DS}=2.8V, while we found breakdown at the source also on devices stressed at V_{DS}=2.7V In fact, V_{GS} is positive, while V_{GD} is negative, so we expect that the breakdown near the drain will occur later. Noticeably, the oxide breakdown does not induce an abrupt varation on the transfer characteristics.

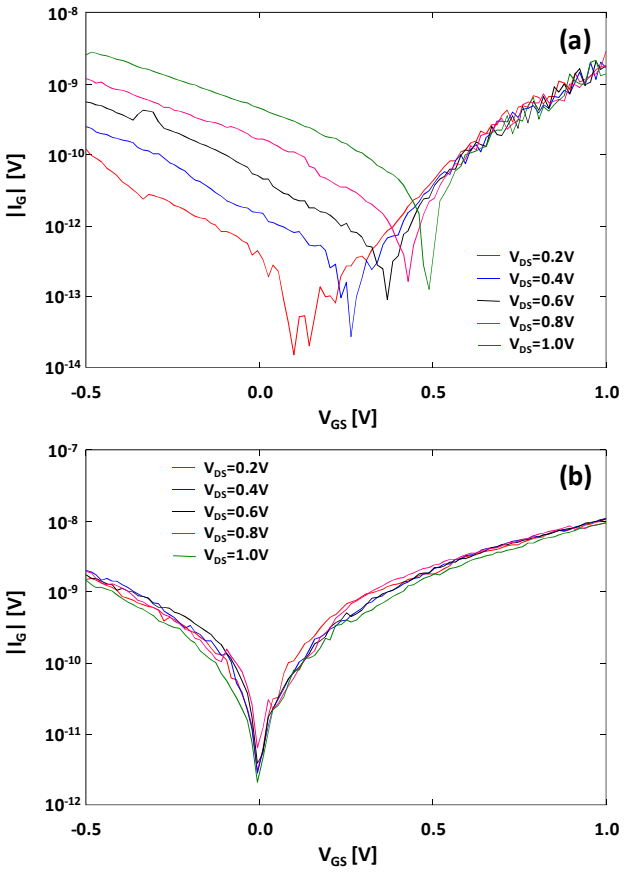

Figure 11. I_G-V_{GS} (absolute value) on a device which had a breakdown both near the source and drain (a) and only at the source (b), taken at different V_{DS} values. When the breakdown occurs just at the source, almost no V_{DS} dependence is observed.

During the stress, the subthreshold swing increases, as shown in Fig. 7, due to the interface degradation, that is, due to generation of new traps. The subthreshold swing increase is more pronounced at the higher stress voltage, especially in the latter stress steps. In fact, only after long stress times the additional stress-induced interface trap density becomes comparable with the interface trap density of the fresh device. The increased subthreshold swing has other detrimental effects on the electrical characteristics, as can be seen from Fig. 8, where we show the V_{GS} required to achieve I_D = 0.1mA. In other words, the threshold voltage increases and higher V_{GS} values are required to achieve the same drain current value. The effects of the increased subthreshold swing can be also seen on the saturation drain current, which decreases after 50-150 s of CHC stress (see Fig. 9). Noticeably, there is an initial increase of the saturation current, but we can tentatively ascribe this to positive charge trapping, which decreases the device flatband voltage. When the effects of interface trap generation overwhelm the positive charge trapping, a turnover occurs. The reduced saturation drain current also means that the device turn-on becomes slower as the stress proceeds, as the dynamic resistance (which depends on the $I_{D,sat}$) increases.

Remarkably, the I_D-V_{GS} curves after each stress step are strongly stretched out in the subthreshold region, but they are only negligibly affected in the linear region. In fact, by leftward shifting each curve after stress, it is possible to almost perfectly overlap each I_D-V_{GS} in the linear region. Of course, the overlap is not possible in the subthreshold region. This suggests that the device transconductance in the linear region is almost not affected by the stress, as confirmed by Fig. 10, where we show the transconductance, which shows changes smaller than 7% with no monotonic trends as a function of the stress time.

This allows us to make an interesting observation, because the subthreshold slope increases, but the transconductance (if evaluated as a function of the drain current) does not decrease noticeably. This suggests us that:

1) The new traps are not effective as electron scattering centers. In particular, we believe the additional stress-induced trap

density might not be large enough to appreciably affect the electron mobility. For instance, from the 60-mV/dec increase on S (see Fig. 7) on the device stressed at 2.8V, we estimated an increase on the interface trap density of about $8 \cdot 10^{12}$ $cm^{-2} \cdot eV^{-1}$. For comparison, for similar devices in [44] the authors reported a donor-like interface trap density in the order between 1 and 3.5 10^{13} $cm^{-2} \cdot eV^{-1}$.

2) These traps are energetically located deep enough so that, once inversion is reached, they are (almost) all already filled, so that they do not stretch out the I-V curve anymore. For instance, from the 200-mV increase on the threshold voltage (see Fig. 8), we estimate that the number of interface trapped electrons is 1.7 10^{12} cm^{-2}.

In [44] it was found that process-induced traps were donor-type. However, by comparing our I-V curves with those simulated in [44] we conclude that CHC-stress-induced traps are acceptor type. In fact, as can be seen from Fig. 5, the I-V curves show very small off-state current variations, while there is a large positive threshold voltage variation. Acceptor-traps were also found as the main responsible for the permanent I-V degradation after constant voltage stress performed on similar devices [45]. In [45] the acceptor traps were supposed located in the conduction band, with a tail in the energy gap. The presence of such acceptor trap distribution is also consistent with the noticeable transconductance degradation found in our previous work (see [37]). However, in the present work, we do not find appreciable transconductance degradation. Therefore, we argue that our CHC stress procedure generates only deep acceptor traps, without affecting the trap concentration near the conduction band. The differences between this work and [37],[45] are not surprising, due to the different stress techniques. In fact, in [37] and [45], a uniform gate injection was employed (V_D=V_S=0V) instead of CHC stress. Furthermore, higher dielectric field were employed in [45] and [37] (about 3.8MV/cm in [45], and even more in [37]), while the maximum field in this work is at most 2.8MV/cm.

IV. Conclusions

In this work we showed the first results of CHC stresses performed on III-V inversion mode MOSFETs.

The stress not only induces interface trap generation but also it eventually leads to a soft breakdown if the stress voltages are high enough. However the soft breakdown is reached at dielectric fields much lower than those reported in previous works MOSFETs and capacitors employing Al_2O_3. This increased sensitivity might be induced by the hot carriers.

The interface trap generation reduces the ON-state current due to subthreshold swing degradation, which increases the device threshold voltage. However, the stress-induced additional interface traps seem not to affect the electron mobility, at least with our stress procedure. We ascribed this behavior to the generation of deep acceptor-like interface traps.

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