Charge-pumping characterization of interface traps in $Al_2O_3/In_{0.75}Ga_{0.25}As$ metal-oxide-semiconductor field-effect transistors

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Charge pumping was used to characterize the interface traps between Al_2O_3 and $In_{0.75}Ga_{0.25}As$ in an *n*-channel inversion-mode metal-oxide-semiconductor field-effect transistor (MOSFET). By analyzing the charge pumped under gate voltage pulses of different rise and fall times, the interface trap density was extracted across the band gap of $In_{0.75}Ga_{0.25}As$. The interface trap density was found to be 4×10^{12} $cm^{-2}\,eV^{-1}$ near the conduction band and to peak at 3×10^{13} $cm^{-2}\,eV^{-1}$ mid-gap. The result helps explain the promising on-state performance of the $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSFET and the need to further improve the interface so that its off-state performance can be on par with that of the Si MOSFET. © *2010 American Institute of Physics*. [doi:10.1063/1.3315870]

The continued scaling of metal-oxide-semiconductor field-effect transistor (MOSFET) is pushing the silicon-based technology to the limit so that alternative channel materials need to be considered. Among all alternative channel materials, III-V compound semiconductors are especially attractive because they allow much higher electron mobility. However, the interface between III-V semiconductors and native or deposited oxides are typically plagued by high trap density, which makes it difficult to build inversion-mode MOSFETs necessary for low-power high-performance complimentary logic. Recently, we demonstrated[1,2] promising performance in inversion-mode pseudomorphic $In_{0.75}Ga_{0.25}As$ MOSFETs with Al_2O_3 gate oxide. In general, with increasing In mole fraction, the band gap decreases while the electron mobility increases. In contrast, using a charge-pumping technique, this letter shows that the interface trap density (D_{IT}) does not vary significantly with the In mole fraction. Since the $In_{0.75}Ga_{0.25}As$ MOSFET requires less movement of the surface Fermi level between accumulation and inversion than MOSFETs with wider band gaps such as the lattice-matched $In_{0.53}Ga_{0.47}As$ MOSFET, the $In_{0.75}Ga_{0.25}As$ MOSFET has a higher inversion charge density than the $In_{0.53}Ga_{0.47}As$ MOSFET under the same gate voltage. The combination of higher charge density and mobility leads to three to five times higher drive current in the $In_{0.75}Ga_{0.25}As$ MOSFET than in the $In_{0.53}Ga_{0.47}As$ MOSFET, which is a significant advantage.

Based on direct measurement of trap recombination current, charge pumping[3] has been the most sensitive and reliable technique to characterize interface traps in MOSFETs. Recently, the technique has been applied[4,5] to $In_{0.53}Ga_{0.47}As$ and $In_{0.65}Ga_{0.35}As$ MOSFETs. This letter reports the first charge-pumping investigation of the $In_{0.75}Ga_{0.25}As$ MOSFET. In addition, by varying the rise/fall times and temperature over a wide range, the interface trap density was characterized over a much wider energy range, which spans most of the band gap.

Figure 1(a) illustrates the structure of the $In_{0.75}Ga_{0.25}As$ MOSFET. A 500 nm layer of $In_{0.53}Ga_{0.47}As$ *p*-doped to 4×10^{17} cm^{-3}, a 300 nm layer of $In_{0.53}Ga_{0.47}As$ *p*-doped to 1×10^{17} cm^{-3}, and a 20 nm layer of $In_{0.75}Ga_{0.25}As$ *p*-doped to 1×10^{17} cm^{-3} were sequentially grown on p^+-doped InP substrate by molecular beam epitaxy. A 10 nm layer of Al_2O_3 was then formed by atomic layer deposition as the gate oxide. The gate was metallized with evaporated Ni. The gate width (W_G) was 200 μm while the gate length (L_G) was systematically varied from 1 to 40 μm. The detailed fabrication process and device performance were published elsewhere.[1]

The charge-pumping measurement was performed by using an Agilent 4156C precision semiconductor parameter analyzer with an Agilent 41501B pulse generator expander. During the charge-pumping measurement, the 41501B generated gate voltage pulses (V_G) while the 4156C measured the charge-pumping current (I_{CP}) from the source and drain. Source, drain, and substrate were all grounded. Figure 1(b) illustrates the gate voltage waveform and defines the high level (V_{GH}), low level (V_{GL}), amplitude (ΔV_G), rise time (t_R), fall time (t_F), pulse period (T), and pulse frequency (f).

By using the variable-amplitude charge-pumping technique so that V_{GL} is kept constant while V_{GH} is swept from -3 to 3 V, the measured maximum I_{CP} is linearly dependent on the gate length (or the gate area because the gate width is constant) as shown in Fig. 2(a). The measurement is performed by directly probing the gate, with the gate contact

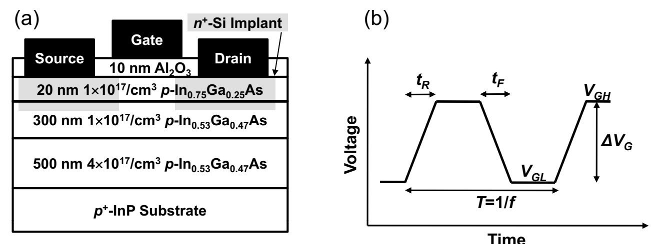

FIG. 1. (a) Schematic cross section of an $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSFET. (b) Gate voltage waveform during charge pumping.

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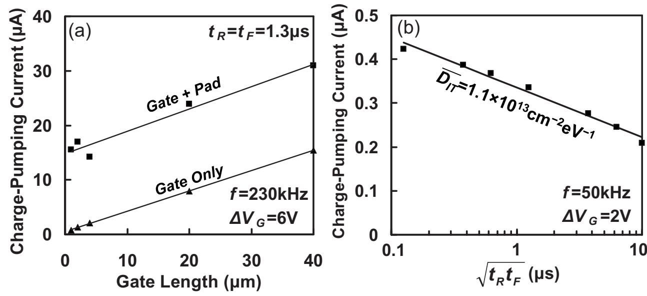

FIG. 2. (a) Maximum charge-pumping current from variable-amplitude measurement on $In_{0.75}Ga_{0.25}As$ MOSFETs with different gate lengths before (■) and after (▲) their gate contact pads are scribed off. (b) Maximum charge-pumping current from variable-base measurement on an $In_{0.75}Ga_{0.25}As$ MOSFET with 4 μm gate length.

pad scribed off. Otherwise, I_{CP} will have a large parasitic component even when the gate length diminishes. This is because in the present $In_{0.75}Ga_{0.25}As$ MOSFET, the gate contact pad is built on top of the same *p*-doped InGaAs layers and InP substrate as the gate itself. When the gate is pulsed from inversion to accumulation, minority carriers should flow back to the source and drain. However, due to the large gate pad size, this process cannot be completed before majority carriers from the substrate arrive at the $Al_2O_3/In_{0.75}Ga_{0.25}As$ interface, so that the remaining minority carriers recombine with majority carriers at the interface and contribute parasitically to I_{CP}.

After the gate contact pad was scribed off and the parasitic-free measurement was confirmed, the average D_{IT} was extracted by using the variable-base charge-pumping technique. In this case, V_{GL} is swept while ΔV_G is kept constant. Meanwhile, t_R and t_F are simultaneously varied from 0.13 to 10 μs to scan a wide energy range. Figure 2(b) shows the maximum I_{CP} as a function of $\sqrt{t_R t_F}$ for an $In_{0.75}Ga_{0.25}As$ MOSFET with $L_G=4$ μm. The average D_{IT} is extracted according to[6]

$$\overline{D_{IT}} = (\log e/2qkTA_G)[dQ_{CP}/d\log(\sqrt{t_R t_F})], \tag{1}$$

where e is Euler's number, q is the electron charge, k is Boltzmann's constant, T is the absolute temperature, A_G is the gate area, and $Q_{CP}=I_{CP}/f$ is the recombined charge per gate voltage pulse. An average D_{IT} of 1×10^{13} cm^{-2} eV^{-1} is obtained.

To extract the distribution of D_{IT} across the band gap, t_R and t_F are swept independently between 0.13 to 10 μs at 25 and −50 °C as shown in Figs. 3(a) and 3(b). In this case, I_{CP}

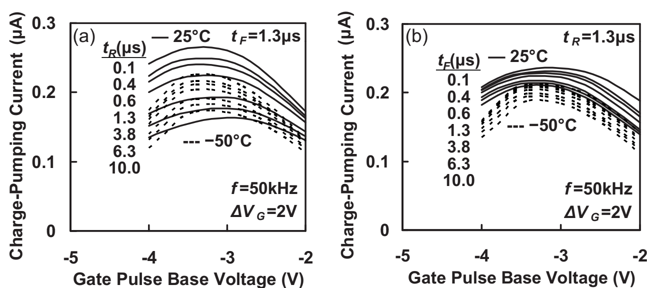

FIG. 3. Variable-base charge-pumping current of the 4-μm-gate-length $In_{0.75}Ga_{0.25}As$ MOSFET with different (a) rise and (b) fall times at 25 and −50 °C.

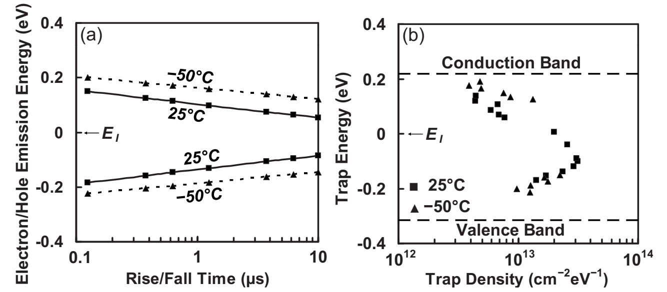

FIG. 4. (a) Calculated electron and hole emission levels and (b) interface trap density across the band gap of $In_{0.75}Ga_{0.25}As$.

is proportional to the amount of interface traps located within the electron and hole emission levels defined by t_R and t_F (Ref. 6)

$$I_{CP} = qA_G f \int_{E_{EMH}}^{E_{EME}} D_{IT}(E)dE, \tag{2}$$

where E is energy measured from the intrinsic level E_I, while E_{EME} and E_{EMH} are calculated[7] electron and hole emission levels as shown in Fig. 4(a). Basic semiconductor parameters[8] of $In_{0.75}Ga_{0.25}As$ and a trap capture cross section of 1×10^{-17} cm^{-2}, without energy or temperature dependence, are used in the calculation. Fermi–Dirac statistics is used to calculate band bending at the surface, because the Fermi level can be within $3kT$ of the conduction band due to the small band gap of $In_{0.75}Ga_{0.25}As$. Thermal velocity is calculated according to $\sqrt{3kT/m^*}$, where m^* is the effective mass of electrons or holes. After E_{EME} and E_{EMH} are calculated, the energy dependence of D_{IT} is extracted according to Eq. (2) using peak I_{CP} values of Figs. 3(a) and 3(b).

Figure 4(b) shows the extracted energy dependence of D_{IT}, with the −50 °C data consistent with the 25 °C data but spanning most of the band gap. It can be seen that D_{IT} is 4×10^{12} cm^{-2} eV^{-1} near the conduction band and it peaks at 3×10^{13} cm^{-2} eV^{-1} approximately 0.1 eV below E_I. The average D_{IT} of 1×10^{13} cm^{-2} eV^{-1} is comparable to that observed[5] in the $In_{0.65}Ga_{0.35}As$ MOSFET fabricated with a similar process, without obvious dependence on the In mole fraction. The average D_{IT} appears to be an order of magnitude higher than that reported[4] for the $In_{0.53}Ga_{0.47}As$ MOSFET. However, the D_{IT} near the conduction band reported by Ref. 4 is comparable to the presently measured value. Since Ref. 4 measures D_{IT} near the band edge only, it is not obvious what kind of weighting is used to arrive at the average D_{IT}. The interface traps in InGaAs MOSFETs have been identified as donors,[5] which are neutralized upon inversion and do not affect the on-state performance of InGaAs MOSFETs. However, they limit the off-state performance of InGaAs MOSFETs such as subthreshold slope, drain-induced barrier lowering, and on/off current ratio.[2]

In conclusion, a wide range of energy distribution of interface traps in the $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSFET was determined by the charge-pumping technique. D_{IT} was found to be 4×10^{12} cm^{-2} eV^{-1} near the conduction band and to peak at 3×10^{13} cm^{-2} eV^{-1} 0.1 eV below E_I. The result helps explain the promising on-state performance of the $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSFET and the need to improve the interface further so that its off-state performance can be on par with that of the Si MOSFET.

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