Simulation and optimization of GaN-based metal-oxide-semiconductor high-electron-mobility-transistor using field-dependent drift velocity model

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Undoped GaN-based metal-oxide-semiconductor high-electron-mobility-transistors (MOS-HEMTs) with atomic-layer-deposited Al_2O_3 gate dielectrics are fabricated with gate lengths from 1 μm up to 40 μm. With a two-dimensional numerical simulator, we report simulation results of the GaN-based MOS-HEMTs using field-dependent drift velocity model. A developed model, taking into account polarization-induced charges and defect-induced traps at all of the interfaces and process-related trap levels of bulk traps measured from experiments, is built. The simulated output characteristics are in good agreement with reported experimental data. The effect of the high field at the drain-side gate edge and bulk trap density of GaN on the output performance is discussed in detail for the device optimization. AlGaN/GaN/AlN quantum-well (QW) MOS-HEMTs have been proposed and demonstrated based on numerical simulations. The simulation results also link the current collapse with electrons spreading into the bulk, and confirm that a better electron localization can dramatically reduce the current collapse for the QW-MOS-HEMTs. Due to the large band edge discontinuity and effective quantum confinement of the AlGaN/GaN/AlN quantum well, the parasitic conduction in the bulk is completely eliminated. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2764206]

I. INTRODUCTION

AlGaN/GaN heterostructure devices are very attractive for high temperature, high power, and high frequency devices.[1,2] Recent advances in GaN-based high-electron-mobility-transistors (HEMTs) have opened the way for their practical applications in the above devices. However, the typically large gate leakage current reduces the breakdown voltage, power-added efficiency and device reliability, in addition to increasing the noise figure. The leakage current is thus an important roadblock to practical applications of these devices. To solve the problem, significant progress has been made on metal-insulator-semiconductor high-electron-mobility-transistors (MIS-HEMTs) and metal-oxide-semiconductor high-electron-mobility-transistors (MOS-HEMTs) using SiO_2,[3–7] Si_3N_4,[8,9] Al_2O_3,[10,11] and other oxides.[12] Recently, Ye *et al.*[13–15] have reported a GaN-based MOS-HEMT with atomic-layer-deposited (ALD) Al_2O_3 as the gate dielectric, showing low leakage current, high breakdown voltage, strong accumulation, and high effective two-dimensional (2D) electron mobility under both low and high transverse fields. ALD Al_2O_3 has been widely studied as a gate dielectric and has become one of the leading candidates to replace SiO_2 in future-generation Si complementary metal-oxide semiconductor (CMOS) digital integrated circuits (ICs).[16,17] However, current collapse effects observed in most of the GaN-based transistors not only degrade microwave output performance but also impede reliable operation of the GaN-based power devices.[9,18] Previous numerical simulation work[18,19] has demonstrated that the significant current collapse effect, due to the charge trapping at the GaN bulk, degrades the device performance under radio frequency (RF) operations. The trapped charges may accumulate at the drain-side gate edge, where the electric field significantly changes and gate-voltage-dependent strain is induced.

Physics-based numerical simulation provides an efficient and economical way for complementing experimental investigations. Identifying the essential physical mechanisms, which are responsible for particular effects of the MOS-HEMT's electrical behavior by means of simulation, allows pushing ahead the further development of the MOS-HEMT's. Although several numerical simulation studies[18–23] have been made on the GaN-based HEMTs, few works give a full consideration on GaN-based MOS-HEMTs and their related issues on polarization-induced charges and defect-induced traps at all of the interfaces. In addition, process-related trap levels of bulk traps measured from experiments have not been taken into account. Previous numerical simulation studies of GaN-based HEMTs mainly focused on general device aspects and mostly on simplified models. The aim of this work is to understand the underlying physics of carrier kinetics in GaN-based heterostructures and to select or develop physical models suitable for predictive simulations of the GaN-based MOS-HEMTs. Special interface models are developed on the basis of direct current (dc) characteristics simulations. A quantum-well MOS-HEMT structure is

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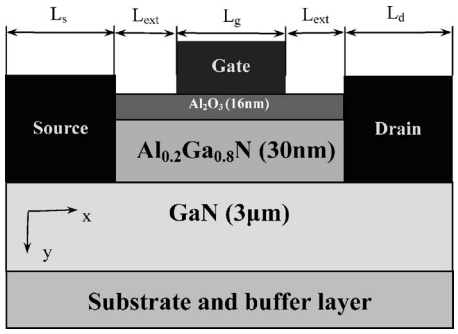

FIG. 1. Schematic structure of GaN-based MOS-HEMT with Al_2O_3 gate dielectric.

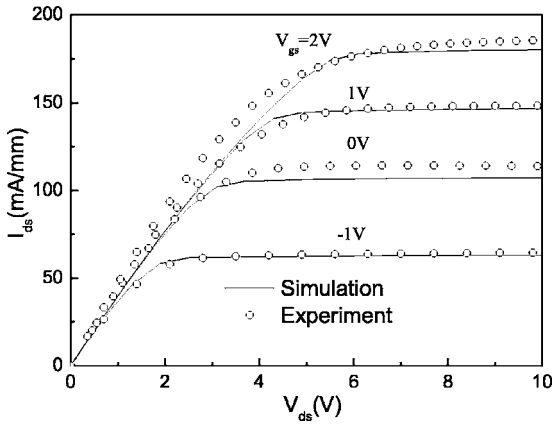

FIG. 2. The simulated and experimental $I_{ds}-V_{ds}$ of MOS-HEMT. Experiment (circles) and simulation (solid lines) with field-dependent drift velocity model for $V_{gs}=-1$, 0, 1, 2 V.

proposed and demonstrated on the basis of transient simulations for optimizations of the current collapse and parasitic conduction. The simulation results are compared with experimental data and represent a solid basis for application-specific device optimizations.

In Sec. II, we describe physical models, analyzed structures and material parameters for the simulations. In Sec. III, systematic theoretical computations of the interface charges in the GaN-based MOS-HEMT induced by the high piezoelectric and spontaneous polarization are described. A single donor-type interface trap at the Al_2O_3/AlGaN interface is assumed according to experimental measurements. In Sec. IV, the current collapse effect caused by the electric fields strain at the drain-side gate edge and the bulk traps in AlGaN and GaN is investigated. Optimizations of the geometry of current devices for reducing current collapse effect are proposed and demonstrated in Sec. V.

II. DEVICE DESCRIPTION AND SIMULATION MODEL

Figure 1 shows the cross sections of an ALD Al_2O_3/AlGaN/GaN-based MOS-HEMT. A 40 nm undoped AlN buffer layer, a 3 μm undoped GaN layer, and a 30 nm undoped $Al_{0.2}Ga_{0.8}N$ layer are sequentially grown by metal-organic chemical vapor deposition on a 2 in. sapphire substrate. After these layers are grown, the wafer is transferred via room ambient to an ASM Pulsar2000™ ALD module. A 16 nm thick Al_2O_3 layer is deposited at 300 °C then followed by annealing at 600 °C for 60 s in oxygen ambient. Device isolation is achieved by nitrogen implantation. Using a wet etch in diluted HF, the oxide on the source and drain regions is removed while the gate region is protected by photoresist. Ohmic contacts are formed by electron-beam deposition of Ti/Al/Ni/Au and a lift-off process, followed by an 850 °C anneal in nitrogen ambient, which also activated the previously implanted nitrogen. Finally, Ni/Au metals are *e*-beam evaporated and lifted off to form the gate electrodes. All four levels of lithography (alignment, isolation, ohmic, and gate) are done by using a contact aligner. The gate width (W_g) is 100 μm, the gate length (L_g) varies from 1 μm to 40 μm (most of the simulations are concentrated on 5 μm), the source and drain lengths (L_s and L_d) are 5 μm, and the source/drain extension (L_{ext}) is 2 μm.

The simulations are performed for the GaN-based MOS-HEMT described above. The simulation tool, whose validity in the GaN-based HEMTs has been established in Refs.18 and 19, is the two-dimensional device simulator Sentaurus Device (the former version of ISE-DESSIS) from Synopsys Inc. A fixed temperature of $T=300$ K is assumed in all simulations since self-heating effects go beyond the scope of this work, and experimental $I_{ds}-V_{ds}$ characteristics (see Fig. 2) indicate that no significant self-heating occurs within the range of applied bias investigated in this work. In high electric fields, the carrier drift velocity is no longer proportional to the electric field strength, instead, the velocity saturates to a finite speed. To account for the velocity saturates in wurtzite group-III nitrides, the field-dependent drift velocity (FDV) model is performed in the simulation and can be expressed by

$$\mu(F) = \frac{\mu_{\text{low}}}{[1 + (\mu_{\text{low}} F_{\text{hfs}}/v_{\text{sat}})^{\beta}]^{\frac{1}{\beta}}}, \tag{1}$$

where μ_{low} donates the low-field mobility, and v_{sat} is the saturation velocity given by

$$v_{\text{sat}} = A_{v\text{sat}} - B_{v\text{sat}}\left(\frac{T}{300\ \text{K}}\right) v_{\text{sat}} > v_{\text{sat,min}}$$
$$= v_{v\text{sat,min}} \quad \text{otherwise}, \tag{2}$$

where A_{sat}, $B_{v\text{sat}}$ is the fitting parameters. The exponent β is temperature dependent according to $\beta=\beta_0(T/300\ \text{K})^{\beta_{\text{exp}}}$ and F_{hfs} is the driving field. For hydrodynamic simulations, the driving for electrons is

$$F_{\text{hfs}} = \sqrt{\frac{\max(w_n - w_0, 0)}{\tau_{e,n} q \mu_n}}, \tag{3}$$

where $w_n=3kT_n/2$ is the average electron thermal energy, $w_0=3kT/2$ is the equilibrium thermal energy, and $\tau_{e,n}$ is the energy relaxation time. The driving fields for holes are analogous. Mobility of GaN grown on the sapphire substrate under low transverse fields is approximately 1200 $\text{cm}^2/\text{V s}$.[13] Parameters of Al_2O_3 are extracted from Refs. 11 and 13. The estimated Al_2O_3 thickness (d_{OX}) is 10 nm, which is significantly less than the design value of 16 nm.

Photoionization measurements in AlGaN/GaN HEMTs have been carried out by Klein *et al.*[24] The work has indicated that two trap levels, locating approximately 1.8 eV and

2.85 eV below the conduction band, respectively, in the high resistivity MOVCD GaN buffer layer, produced the current collapse in HEMTs.[25] These trap levels are considered in the GaN layer in our simulations. The trap density is $N_{\mathrm{GaN}}=2.5\times10^{16}$ cm^{-3} with a capture cross section of $\sigma_{\mathrm{GaN}}=1.0\times10^{-15}$ cm^{-2}. A significant amount of structural defects, such as threading or misfit dislocations, and processing damage, such as plasma damage or thermal damage, exist in the AlGaN barrier due to the immature of the AlGaN/GaN technology, which are translated into bulk traps.[26–28] Since those trap parameters are still largely unknown, we assume just a single acceptor type electron bulk trap level and fit the values from the experimental data in the AlGaN barrier. The traps density is $N_{\mathrm{AlGaN}}=5.0\times10^{16}$ cm^{-3} with a capture cross section of $\sigma_{\mathrm{AlGaN}}=1.0\times10^{-15}$ cm^{-2}. We position it 2.2 eV below the conduction band.

III. POLARIZATION EFFECT AND INTERFACE TRAPS

The strain induced and spontaneous polarization cause interface charges at heterojunctions between different group-III nitride materials.[29,30] These charges have been taken into account in our simulations by specifying the interface charges at the heterojunctions. Theoretical computations of the interface charges of the GaN-based MOS-HEMT due to the high piezoelectric and spontaneous polarization are given as follows:

The strain-induced piezoelectric polarization of $Al_xGa_{(1-x)}N$ can be expressed by

$$P_{\mathrm{pz\_AlGaN}}(x)=2\varepsilon_{xx}\left(e_{31}-\frac{c_{13}}{c_{33}}e_{33}\right), \tag{4}$$

$$\varepsilon_{xx}=\frac{[a_{\mathrm{GaN}}-a_{\mathrm{AlGaN}}(x)]}{a_{\mathrm{AlGaN}}(x)}. \tag{5}$$

The charge due to the variation of the piezopolarization at AlGaN/GaN is given by

$$D_{\mathrm{Ppz}}=0-P_{\mathrm{pz\_AlGaN}}(x), \tag{6}$$

where a is the crystal lattice constant. A linear interpolation between the lattice constant of GaN and AlN is used on the calculation of $a_{\mathrm{AlGaN}}(x)$, ε_{xx} is the strain of the $x-y$ plane, c_{13} and c_{33} are the elastic constants, and e_{33} and e_{31} are the piezoelectric constants.

The spontaneous polarization of $Al_{(1-x)}Ga_xN$ is also a function of Al mole fraction x and can be expressed by

$$P_{\mathrm{sp\_AlGaN}}(x)=xP_{\mathrm{sp\_AlN}}+(1-x)P_{\mathrm{sp\_GaN}}. \tag{7}$$

The charge due to the spontaneous polarization at AlGaN/GaN is given by

$$D_{\mathrm{Psp}}=P_{\mathrm{sp\_GaN}}-P_{\mathrm{sp\_AlGaN}}(x). \tag{8}$$

The charge due to the spontaneous polarization at GaN/AlN can be expressed by

$$D_{\mathrm{PspAlN}}=P_{\mathrm{sp\_AlN}}-P_{\mathrm{sp\_GaN}}. \tag{9}$$

Finally the interface charge induced by the polarization at AlGaN/GaN is included in our simulation as $D_{\mathrm{Psp}}+D_{\mathrm{Ppz}}$ with the value of 1.2×10^{13} cm^{-2}. The interface charge at AlGaN/Al_2O_3 is $P_{\mathrm{sp\_AlGaN}}(x)+P_{\mathrm{pz\_AlGaN}}(x)$ with the value of -2.9×10^{13} cm^{-2}. The interface charge at GaN/AlN is D_{PspAlN} with the value of -3.1×10^{13} cm^{-2}. All of the parameters in Eqs. (4)–(9) can be found in Ref. 31.

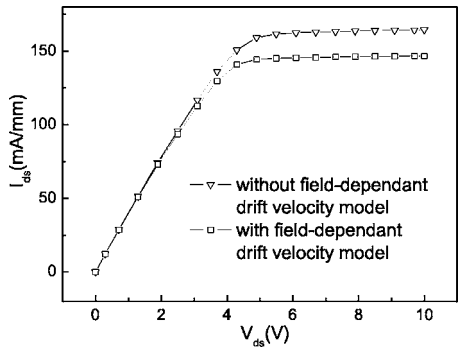

FIG. 3. The simulated current-voltage characteristics ($I_{ds}-V_{ds}$) with and without field-dependent drift velocity model at $V_{gs}=1$ V.

The dielectric passivation establishes a near-optimal dielectric/semiconductor interface.[13–15] However, a net interface charge with a density of $10^{11}-10^{12}$ cm^{-2} can still be induced by the combination of the polarized AlGaN barrier and interface states associated with surface defects, dangling bonds, and adsorbed ions or charged residuals. In practice, experiments[32–35] have shown that the polarization dipole is screened by the positively charged surface donor and two-dimensional electron gas (2DEG). Here we assume just a single donor-type interface traps with a density of 3.0×10^{13} cm^{-2} to keep the net interface charges of the Al_2O_3/AlGaN interface at the range of $10^{11}-10^{12}$ cm^{-2} extracted from the $C-V$ measurement and frequency dispersion of transconductance measurement.[13,14]

IV. SIMULATION AND DISCUSSION

Figure 2 shows the simulated and experimental dc output characteristics ($I_{ds}-V_{ds}$) of the MOS-HEMT for V_{gs} values varying from −1 to 2 V in 1 V steps. It is found that the simulation results are in good agreement with the experiment data, verifying the validity of the simulation. Figure 3 shows the $I_{ds}-V_{ds}$ characteristics as predicted with/without FDV model at $V_{gs}=1$ V. The simulation results reveal that the drain current predicted with the FDV model is suppressed by an amount approximately 10.2% due to the velocity saturation of carriers when FDV is chosen. It is well known that, at low electric fields, where there is a linear variation of velocity with electric field (E), the mobility is the slope of the drift velocity (v) versus the electric fields, and can be expressed by $\mu=v/E$. The behavior of the drift velocity of carriers at high electric fields deviates substantially from the linear relationship observed at low fields, instead, the velocity saturates to a finite speed v_{sat}. Therefore, at high electric fields region, the mobility is dependent of the electric fields. We can also note that the data from the FDV model agree more closely to that of the experimental data. Therefore, the classical approach does not account for the significant high electric field effects in wurtzite group-III nitrides.

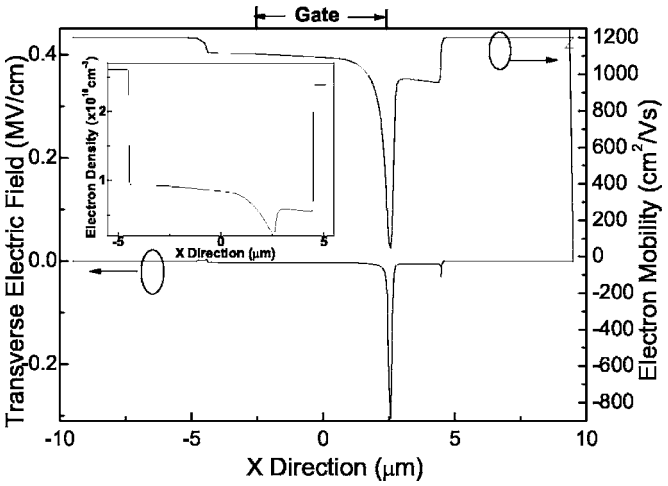

FIG. 4. The transverse electric field (left *Y* axis) and electron mobility (right *Y* axis) versus *X* direction cut at 2 nm away from AlGaN/GaN for $V_{gs}=1$ V and $V_{ds}=10$ V. The inset shows electron density vs *X* direction.

Figure 4 shows the transverse electric field (left *Y* axis) and electron mobility (right *Y* axis) versus *X* direction at AlGaN/GaN for $V_{gs}=1$ V and $V_{ds}=10$ V. The electric field significantly changes in both transverse and longitudinal directions at the drain-side gate edge. As conventional transistors, V_{gs} of HEMTs controls the depletion and accumulation of the 2DEG. The gate-voltage-dependent strain is induced by the transition from the metal covered part of the channel to the gate/drain extension region. In the simulation, this gate-voltage-dependent strain ($V_{gs}=1$ V) has the electrons trapped at the gate edge, called trapped charge. Therefore, the 2DEG significantly decreases at the drain-side gate edge (as shown in the inset of Fig. 4). The depletion of the 2DEG induces the fluctuation of the electric fields at the drain-side gate edge. According to the former discussed FDV model, the mobility will dramatically decrease at the drain-side gate edge. As shown in Fig. 4, when the fields are sufficiently large, nonlinearities in mobility are observed at the drain-side gate edge. The average effective electron mobility is about 800 cm^2/V s.

To verify the validity of our simulations, we calculate the effective 2D electron mobility μ_{eff} at the AlGaN/GaN heterojuction under the high transverse field using an analytical model used by Ye *et al.*[13] The μ_{eff} can then be calculated according to

$$R_{\text{ch}} = \frac{1}{\mu_{\text{eff}} C_{\text{MOS-HEMT}}(V_{gs} - V_{\text{Gi}})}, \tag{10}$$

$$E_{\text{eff}} = \frac{V_{gs} - V_{\text{Gi}}}{2\varepsilon_{\text{GaN}}(d_{\text{OX}}/\varepsilon_{\text{OX}} + d_{\text{AlGaN}}/\varepsilon_{\text{AlGaN}})}, \tag{11}$$

where $C_{\text{MOS-HEMT}}$ is the zero-bias gate capacitance, V_{Gi} is the zero-current intercept of V_{gs} extrapolated from the point of inflection of the I_{ds} vs V_{gs} characteristic, R_{ch} is the intrinsic normalized channel resistance, ε_{GaN} and $\varepsilon_{\text{AlGaN}}$ are the dielectric constants of GaN and AlGaN, d_{AlGaN} and d_{OX} are the thickness of the AlGaN layer and the Al_2O_3 layer, E_{eff} is the effective transverse field. All of the parameters in Eqs. (10) and (11) can be found elsewhere.[13,14] The simulated effective

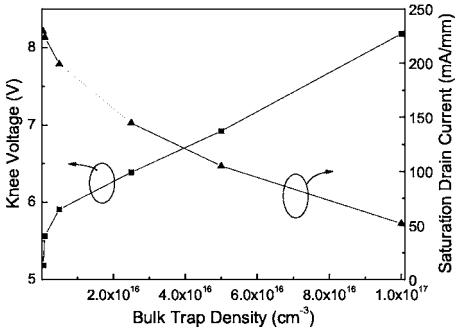

FIG. 5. The simulated knee voltage and saturation drain current as a function of bulk trap density at $V_{gs}=1$ V.

electron mobility is compared with the result from the analytical model. The mobility of 840 cm^2/V s under a high transverse field of 0.3 MV/cm is in good agreement with the simulated value. From the above results, we can confirm that the inclusion of FDV model is crucial for the accurate simulation of the GaN-based MOS-HEMTs, especially with respect to the high-voltage output $I-V$ characteristics and hot electron effects near the drain-side gate edge.

In Fig. 5, the simulated knee voltage (V_{knee}) and saturation drain current (I_{sat}) are plotted as a function of the bulk trap density at $V_{gs}=1$ V. An increase in V_{knee} is obtained when an order of magnitude increase of the bulk trap density is assumed in the MOS-HEMT. As expected, a reversed response in I_{sat} is obtained when an increase of the bulk trap density is used. It is well known that the current collapse occurs when a high drain-source voltage is applied to the device, resulting in the transfer of hot carriers from the conducting channel to an adjacent region of the device structure that contains a high concentration of deep bulk traps.[35–37] The carriers can then become trapped at these defects. The loss of channel carriers and the resulting large transverse electric field (as shown in Fig. 4) lead to a collapse of the dc $I-V$ characteristic, which exhibits a reduced drain current. As discussed above, the depletion of the 2DEG due to the bulk trapping effects induces the large transverse fields at the drain-side gate edge. A high-resistivity depletion region is formed at the drain-side gate edge. The high-resistivity region will cause a voltage drop to the drain bias. For the same drain bias, the higher bulk traps density is, the more the voltage drops. The high-resistivity depletion region can pinch off the I_{ds}. Therefore, for the higher bulk traps density, the bigger drain bias is needed to achieve the pinch-off voltage. Then the increase of V_{knee} is induced when the bulk trap density is increased.

When such a device is operated as an amplifier, the maximum output power is given by[32]

$$P = [(V_{\text{breakdown}} - V_{\text{knee}}) \times I_{\text{sat}}]/8, \tag{12}$$

where $V_{\text{breakdown}}$ is the breakdown voltage. Experimentally, it is observed that the output power measured at the frequencies of interest (4–18 GHz) is well below that calculated using Eq. (12). This reduction in output power from its expected value based on the simulated results (as shown in Figs. 2 and 5) is caused by a decrease of saturation drain current together an increase of the knee voltage. This degra-

dation in device performance has been the main obstacle to obtaining the high power output at microwave frequencies and has been called as the current collapse.[28,38,39] The simulation results confirm that a low defect of GaN-based MOS-HEMT can dramatically reduce current collapse. A possible approach for minimizing the current collapse is the quantum-well MOS-HEMT, as shown in next section.

V. OPTIMIZATION OF GAN-BASED MOS-HEMTS

The current collapse effect under a radio frequency operation, which has been attributed to the surface charge[32] and charge trapping in the GaN bulk,[37] limits the output microwave power. The low resistance of the GaN bulk layer introduces a parasitic current, which degrades the device performance and, in the worst case, does not allow the transistor to be pinched off. Although growth at low pressure by introducing more defects or antidoping by carbon may be used to increase the resistivity of GaN, the dopants also increase the defects density in the GaN bulk, which has been shown to further enhance the current collapse effect.[28] To minimize the drain current collapse effect and the parasitic conduction, a quantum-well MOS-HEMT structure is proposed and demonstrated on the basis of the simulations. Since hot electron plays an important role in the vertical real space charge transfer and subsequent capture in bulk traps, carrier temperature in the small active region is calculated by the hydrodynamic transport model available in Sentaurus Device Simulator.[40]

Since AlN with a band gap of 6.1 eV is highly resistive, high-quality AlN epilayers can be grown, and bulk AlN substrates are also available, we substitute the GaN bulk layer with highly resistive AlN bulk layer[41] to build the AlGaN/GaN/AlN quantum-well MOS-HEMTs (QW-MOS-HEMT). The GaN channel layer with a thickness of 50 nm, which is much larger than the critical thickness of GaN/AlN heterostructure, is treated as fully relaxed, and only spontaneous polarization charges appear at the GaN/AlN interface.[41] The net spontaneous polarization charges at the GaN/AlN interface (as calculated in Sec. III) could possibly deplete the 2DEG. A backside-doping scheme is adopted to overcome the depletion. Figure 6 shows the simulated electron density as a function of the distance from AlGaN/GaN with and without the backside doping for the proposed QW-MOS-HEMT. Comparing the electron density with and without the backside doping, our simulations indicate that the electron density without the backside doping is about 80% lower, which is clearly not acceptable. The simulations demonstrate that a 5×10^{18} cm^{-3} backside doping in the QW-MOS-HEMT has the similar sheet electron density as the conventional structure. An excess backside doping causes an undesired backside electron density in the GaN channel as shown in the inset of Fig. 6. This backside electron density can significantly increase the parasitic conduction in GaN. Taking consideration the parasitic conduction in the bulk, we get an optimal backside doping value of 4×10^{18} cm^{-3}.

Generally, a QW HEMT on an AlN substrate forms a double-heterostructure with a narrow band gap GaN channel between a wide-band gap AlN buffer layer and an AlGaN

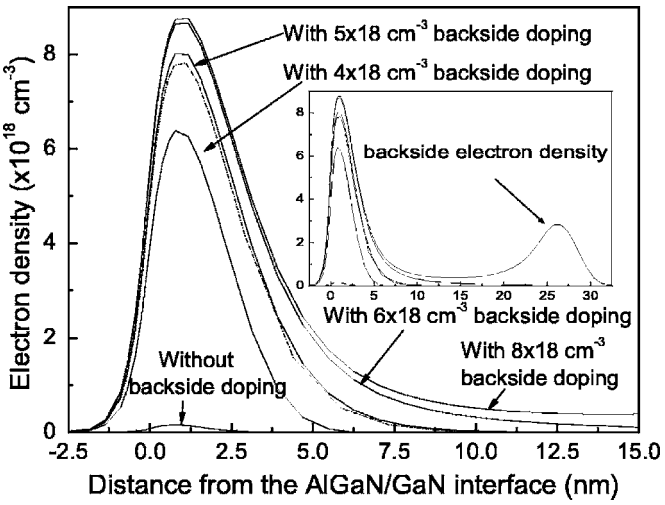

FIG. 6. The simulated electron density as a function of distance from AlGaN/GaN (cut at $x=0$ μm) with different backside doping for the proposed QW-MOS-HEMT. The dashed line shows the electron density for the conventional MOS-HEMT under the same condition. The inset shows the whole electron density throughout the device.

barrier layer. Our simulation of the QW-MOS-HEMT coherently grown on an AlN buffer layer, similar to that reported in Ref. 42, shows that in addition to the 2DEG formed at the AlGaN/GaN interface, a 2DHG (as shown in Fig. 7) is induced at the negatively charged GaN/AlN interface, as discussed in Refs. 42 and 43.

If the GaN layer is thick enough, the 2DHG avoids the shunting of the 2DEG by background electrons in the structure bulk. In this case, a reduction in the channel thickness can improve the electron confinement and prevent the electron spillover toward the bulk. However, the coexistence of the 2DEG and 2DHG in a thin GaN channel may affect negatively the QW-MOS-HEMT performance. Indeed, the ohmic source and drain contact regions formed by annealing may overlap both the 2DEG and 2DHG channels. This is expected to result in shunting the electron conductivity by the parasitic holes. In addition, the electrons heated in the electric field induced by the drain-source voltage are capable of penetrating into the 2DHG region, leading to carrier losses through the electron-hole recombination.[43] Finally, the existence of the 2DHG at the GaN/AlN interface makes the application of our backside-doping concept necessary. Figure 7

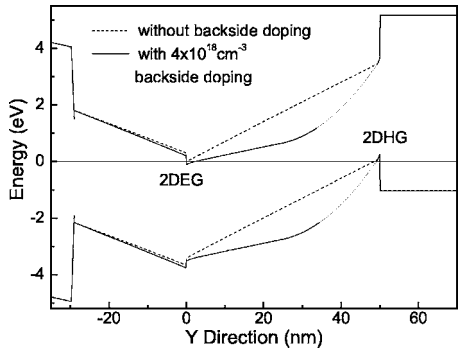

FIG. 7. The simulated band diagram as a function of distance cut at $x=0$ μm with backside doping (solid line) and without backside doping (dashed line) for the proposed QW-MOS-HEMT.

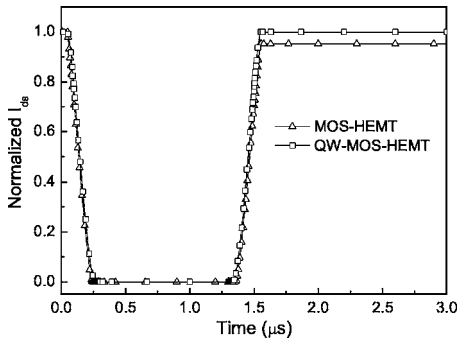

FIG. 8. The drain current as a function of time for MOS-HEMT (triangles) and QW-MOS-HEMT (squares) at $V_{ds}=15$ V.

shows that a backside doping of 4×10^{18} cm^{-3} can significantly screens the depletion effect of the 2DHG and increases concentrations of the 2DEG.

To verify the advantage of our proposed QW-MOS-HEMT, we perform transient simulations for the current collapse effect. The gate pulse as transient signal is such that the minimum gate voltage is close to threshold, and the maximum is at zero. The gate voltage is held at 0V for 0.1 μs, and is changed to −5 V (pinch-off voltage) for 1 μs pulse width, with the fall and rise time of 250 ns, and then is left at 0 V for the rest of the simulation. Figure 8 shows the simulated time dependency of I_{ds} for the conventional MOS-HEMT and QW-MOS-HEMT at $V_{ds}=15$ V. Notice that a collapse of about 15% is observed for the conventional MOS-HEMT under the pulse driving. Compared with the conventional MOS-HEMT, the proposed QW-MOS-HEMT shows a negligible current collapse. The AlGaN/GaN/AlN quantum-well has the large band edge discontinuity and effective quantum confinement, which limit the electron spillover into the bulk, resulting in a reduction of the drain current collapse.

VI. CONCLUSION

High performance GaN-based MOS-HEMTs have been fabricated with Al_2O_3 gate dielectrics. We have accurately simulated the output characteristics of the GaN-based MOS-HEMTs with the field-dependent drift velocity model. The simulation results are found to be in good agreement with the experimental data for ALD Al_2O_3/AlGaN/GaN MOS-HEMTs on a sapphire substrate with a 5 μm gate length. A developed model, taking into account the polarization-induced charges and defect-induced traps at all of the interfaces and process-related trap-levels of bulk traps measured from experiments, is built. The simulation results reveal that the drain current is suppressed by approximately 10.2% due to the velocity saturation of carriers when the field-dependent drift velocity model is chosen. The simulation results confirm that the reduction in the output power from the expected value is caused by a decrease of the saturation drain current together with an increase of the knee voltage. AlGaN/GaN/AlN QW-MOS-HEMTs have been demonstrated based on numerical simulations. The simulations indicate that the QW-MOS-HEMT has the similar sheet electron density as the conventional structure with an optimal backside doping value of 4×10^{18} cm^{-3} taking into consideration the negligible parasitic conduction in the bulk. The AlGaN/GaN/AlN quantum-well has the large band edge discontinuity and effective quantum confinement, which limit the electrons spillover into the bulk, resulting in the reduction of the current collapse. Our simulation results have provided guidance for the device structural optimization.

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[1] S. N. Mohammad, A. A. Salvador, and H. Morkoc, Proc. IEEE **83**, 1306 (1995).
[2] U. K. Mishra, P. Parikh, and Y. F. Wu, Proc. IEEE **90**, 1022 (2002).
[3] M. A. Khan, X. Hu, G. Sumin, A. Lunev, J. Yang, R. Gaska, and M. S. Shur, IEEE Electron Device Lett. **21**, 63 (2000).
[4] M. A. Khan, X. Hu, A. Tarakji, G. Simin, J. Yang, R. Gaska, and M. S. Shur, Appl. Phys. Lett. **77**, 1339 (2000).
[5] G. Simin, X. Hu, N. Ilinskaya, A. Kumar, A. Koudymov, J. Zhang, M. A. Khan, R. Gaska, and M. S. Shur, Electron. Lett. **36**, 2043 (2000).
[6] A. Koudymov, X. Hu, K. Simin, G. Simin, M. Ali, J. Yang, and M. Asif Khan, IEEE Electron Device Lett. **23**, 449 (2002).
[7] G. Simin, A. Koudymov, H. Fatima, J. Zhang, J. Yang, M. Asif Khan, X. Hu, A. Tarakji, R. Gaska, and M. S. Shu, IEEE Electron Device Lett. **23**, 458 (2002).
[8] G. Simin, X. Hu, N. Ilinskaya, J. Zhang, A. Tarakji, A. Kumar, J. Yang, M. Asif Khan, R. Gaska, and M. S. Shur, IEEE Electron Device Lett. **22**, 53 (2001).
[9] X. Hu, A. Koudymov, G. Simon, J. Yang, M. Asif Khan, A. Tarakji, M. S. Shur, and R. Gaska, Appl. Phys. Lett. **79**, 2832 (2001).
[10] S. Ootomo, T. Hashizume, and H. Hasegawa, Phys. Status Solidi B **1**, 90 (2002).
[11] T. Hashizume, S. Ootomo, and H. Hasegawa, Appl. Phys. Lett. **83**, 2952 (2003).
[12] R. Mehandru, B. Luo, J. Kim, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton, D. Gotthold, R. Birkhahn, B. Peres, R. Fitch, J. Gillespie, T. Jenkins, J. Sewell, D. Via, and A. Crespo, Appl. Phys. Lett. **82**, 2530 (2003).
[13] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, Appl. Phys. Lett. **86**, 063501 (2005).
[14] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, "GaN MOS-HEMT using atomic layer deposition A1203 as gate dielectric and surface passivation," in Proceedings of the 2004 IEEE Lester Eastman Conference on High Performance Devices, 2004, pp. 24–25.
[15] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H. J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. K. Ng, and J. Bude, IEEE Trans. Electron Devices **24**, 209 (2003).
[16] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
[17] S. W. Huang and J. G. Hwu, IEEE Trans. Electron Devices **50**, 1658 (2003).
[18] N. Braga, R. Gaska, R. Mickevicius, M. S. Shur, X. Hu, M. A. Khan, G. Simin, and J. Yang, Appl. Phys. Lett. **85**, 4780 (2004).
[19] N. Braga, R. Gaska, R. Mickevicius, M. S. Shur, X. Hu, M. A. Khan, G. Simin, and J. Yang, J. Appl. Phys. **95**, 6409 (2004).
[20] Y. F. Wu, B. P. Keller, S. Keller, D. Kapolnek, S. P. Denbaars, and U. K. Mishra, IEEE Electron Device Lett. **17**, 455 (1996).
[21] J. D. Albrecht, P. P. Ruden, S. C. Binari, and M. G. Ancona, IEEE Trans. Electron Devices **47**, 479 (2001).
[22] I. Ahmad, V. Kasisomayajula, M. Holtza, J. M. Berg, S. R. Kurtz, C. P.

Tigges, A. A. Allerman, and A. G. Baca, Appl. Phys. Lett. **86**, 173503 (2005).
[23]J. M. Tirado, J. L. Sanchez-Rojas, and J. I. Izpura, Semicond. Sci. Technol. **20**, 864 (2005).
[24]P. B. Klein, S. C. Binari, K. Ikossi-Anastasiou, A. E. Wickenden, D. D. Koleske, R. L. Henry, and D. S. Katzer, Electron. Lett. **37**, 661 (2001).
[25]S. C. Binari, P. B. Klein, and T. E. Kaziort, IEEE MTT-S Int. Microwave Symp. Dig. **11**, 1823 (2002).
[26]W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, IEEE Electron Device Lett. **52**, 159 (2005).
[27]X. H. Wu, L. M. Brown, D. Kapolnek, S. Keller, B. Keller, S. P. DenBaars, and J. S. Speck, J. Appl. Phys. **80**, 3228 (1996).
[28]P. B. Klein, S. C. Binari, K. Ikossi, A. E. Wickenden, D. D. Koleske, and R. L. Henry, Appl. Phys. Lett. **79**, 3527 (2001).
[29]A. Bykhovski, B. Gelmont, and M. S. Shur, J. Appl. Phys. **74**, 6734 (1993).
[30]F. Bernardini, V. Fiorentini, and D. Vanderbilt, Phys. Rev. B **56**, R10024 (1997).
[31]O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, J. Appl. Phys. **85**, 3222 (1999); O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, and M. Stutzmann, *ibid.* **87**, 334 (2000).
[32]R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, IEEE Trans. Electron Devices **48**, 560 (2001).
[33]I. P. Smorchkova, C. R. Elsass, J. P. Ibbetson, R. Vetury, B. Heying, P. Fini, E. Haus, S. P. DenBaars, J. S. Speck, and U. K. Mishra, J. Appl. Phys. **86**, 4520 (1999).
[34]J. Kotani, T. Hashizume, and H. Hasegawa, J. Vac. Sci. Technol. B **22**, 2179 (2004).
[35]P. B. Klein, J. A. Freitas, Jr., S. C. Binari, and A. E. Wickenden, Appl. Phys. Lett. **75**, 4016 (1999).
[36]P. B. Klein, S. C. Binari, J. A. Freitas, Jr., and A. E. Wickenden, J. Appl. Phys. **88**, 2843 (2000).
[37]S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, IEEE Trans. Electron Devices **48**, 465 (2001).
[38]C. Nguyen, N. X. Nguyen, and D. E. Grider, Electron. Lett. **35**, 1380 (1999).
[39]A. Koudymov, G. Simin, M. A. Khan, A. Tarakji, R. Gaska, and M. S. Shur, IEEE Electron Device Lett. **24**, 680 (2003).
[40]Device simulator Sentaurus Device (former ISE-DESSIS) Ver. X-2006. 06 Sentaurus Device Manual Synopsys Inc. (2005).
[41]Z. Y. Fan, J. Li, M. L. Nakarmi, J. Y. Lin, and H. X. Jiang, Appl. Phys. Lett. **88**, 073513 (2006).
[42]X. Hu, J. Deng, N. Pala, R. Gaska, M. S. Shur, C. Q. Chen, J. Yang, G. Simin, M. Asif Khan, J. C. Rojo, and L. J. Schowalter, Appl. Phys. Lett. **82**, 1299 (2003).
[43]V. F. Mymrin, K. A. Bulashevicha, N. I. Podolskaya, and S. Y. Karpova, J. Cryst. Growth **281**, 115 (2005).