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Selective Contact Anneal Effects on Indium Oxide Nanowire Transistors using Femtosecond Laser

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ABSTRACT: Nanowire materials have gained great interest as promising candidates for high-performance logic devices to sustain the progress in device scaling. However, little research has been conducted to investigate the role of contacts on the device performance accompanied by an appropriate physical model in nanodevices, although effects of the contacts will prevail as the channel scales. In this study, we investigate the effect of annealing using a femtosecond-laser focused at the contact region between the source-drain electrodes and the nanowire. On the basis of the direct comparison of device characteristics before and after annealing, a contact model is introduced, which could be generally applicable to nanowire transistors with overlap between gate region and source-drain regions. Low-frequency noise measurements in the devices reveal that the I_d^2 normalized noise spectrum and Hooge's constant are reduced following laser annealing.
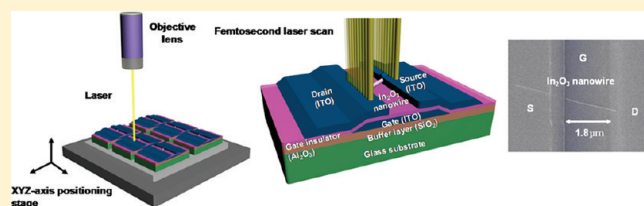
INTRODUCTION

Recent advances in nanowire-based electronics include integration of optically transparent and mechanically flexible circuitry, which could enable easy-to-read, lightweight, transparent, flexible, and unbreakable electronics technologies. Among various nanowire materials, oxide nanowires, such as ZnO, SnO_2, and In_2O_3, are attractive candidate for next-generation nanoelectronics because of their high mobilities, high currents, low-power consumption, nanoscale integration, and compatibility with low-temperature processes.[1−5] Recent studies have demonstrated the use of wide band gap oxide nanowires and low-leakage high-k gate insulators for the realization of transparent thin film transistors (TFTs) with performance far surpassing that of poly/amorphous Si TFTs or organic TFTs.[6−8] However, to move toward future commercial nanoelectronics, there are several challenges to overcome. It is necessary to understand the mechanisms responsible for the current−voltage relationships in nanostructures. Most of the studies on nanowire transistors to date demonstrated source-drain (S-D) current with high drain conductance in the high V_{ds} region, although highly saturated current is very important in implementing practical switching devices.[6−11] Various researchers also reported instability and degradation of threshold voltages (V_{th}) in oxide-based TFTs due to ambient moisture, photons, and bias stress.[12−14] Because it is very important for practical nanowire devices to maintain the initial electrical properties in ambient normal humidity, the recovery of threshold voltages under normal ambient conditions and full trimming capability of the threshold voltages of nanowire transistor is essential. To resolve these issues, our research group and Lee et al. have recently demonstrated control of current saturation and threshold voltage shifts in In_2O_3 nanowire transistors (NWTs) using femtosecond laser annealing focused at the contact regions and shown that switching threshold voltages can be shifted in NMOS-based inverters by annealing the contacts.[15] However, the physics behind the improvement in the semiconductor characteristics following contact modification were not clear. Understanding how to realize contacts suitable for high-performance devices and the role of contacts in the current saturation, threshold voltage, and apparent mobility is important for optimizing device performance and projecting scaling with channel length. However, to the best of our knowledge, little research has been conducted to investigate the role of contacts on the device performance accompanied by an appropriate physical model in nanodevices.

In this Article, we investigate the effects of annealing of the indium tin oxide (ITO) contact regions within In_2O_3 nanowire transistor structures using femtosecond laser pulses selectively focused on the contact regions. On the basis of the direct comparison of device characteristics before and after annealing, we introduce a contact model that is generally applicable to nanowire transistors with overlap between gate region and S-D regions. The contact region annealing induces changes in nanowire transistor characteristics, including early onset of
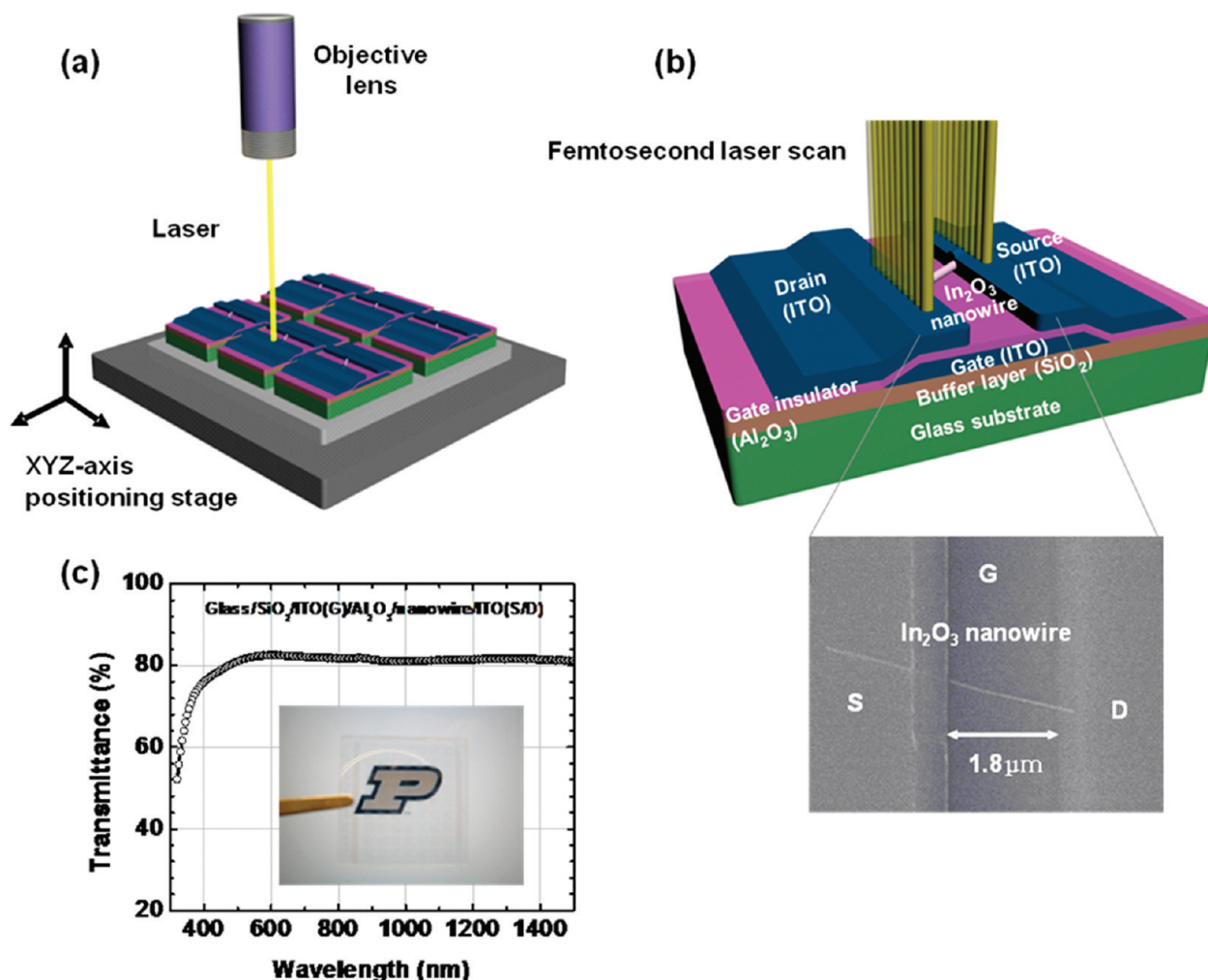
Figure 1. In$_2$O$_3$ NWT structure. (a) The schematic diagram of femtosecond laser process. (b) Cross-sectional view of the fully transparent nanowire device structure. The femtosecond laser pulses are focused and scanned along the S-D region after metallization process. Exposed nanowire channel is not directly exposed to laser irradiation. The inset shows the top view FE-SEM image of the channel region with a single In$_2$O$_3$ nanowire (scale bar = 1.8 μm). (c) Optical transmission spectrum of a 1.5 × 1.5 cm glass substrate (i) before (black square) and (ii) after (red triangle) processing of In$_2$O$_3$ NWTs is complete. The inset shows the optical image of fully transparent NWTs held over a sheet of paper containing a printed image.

current saturation, large improvement in the low-field channel conductance, increased field-effect mobility, improvements in the subthreshold slopes, and increased self-gain, along with significant reduction of the drain conductance in the saturation region and permanent positive shifts in the threshold voltage. Low-frequency (1/f) noise measurements in the devices reveal that the I_d^2 normalized noise spectrum and Hooge's constant are reduced following laser annealing. The improvements of the device performance following laser annealing were analyzed by modeling a parasitic transistor operating in the linear region in series with the nanowire channel, with the conductance of the parasitic transistor improving upon annealing.

■ **EXPERIMENTAL METHODS**

Figure 1a,b shows the schematic diagram of a femtosecond laser process and a nanowire transistor (NWT) with ITO as the S-D contact metal and individually addressable bottom gate structure. The NWTs are fabricated on a glass substrate coated with a 500 nm SiO$_2$ layer deposited by plasma-enhanced chemical vapor deposition, which serves as a buffer and planarization layer. ITO gate electrodes (~100 nm thick) were deposited by RF magnetron sputtering and subsequently patterned by UV photolithography and etching. A thin layer of high-k Al$_2$O$_3$ gate dielectric (thickness, $d_{ox} \approx$ 30 nm) was then deposited by atomic layer deposition at 300 °C using an ASM microchemistry F-120 ALCVD reactor. The structure provides excellent electrostatic modulation of the channel potential without degrading the transport property of the 1-D nanowire channels.[16,17] Single-crystalline In$_2$O$_3$ nanowires were synthesized by a pulsed laser ablation method that was reported by C. Li et al.,[18] with diameters of 20−30 nm and lengths of 5−10 μm. The In$_2$O$_3$ nanowires are not intentionally doped but are believed to be lightly n-type. The nanowires were suspended in isopropanol solution and then deposited onto the patterned substrates. Finally, the ITO for the S-D electrodes was deposited by RF magnetron sputtering (thickness ~100 nm, sheet resistance ~60 Ω/□) and patterned by UV photolithography, with the spacing between contacts (2 μm) defining the channel lengths. The insert of Figure 1b shows a field-emission scanning electron microscope (FE-SEM) image of a representative single
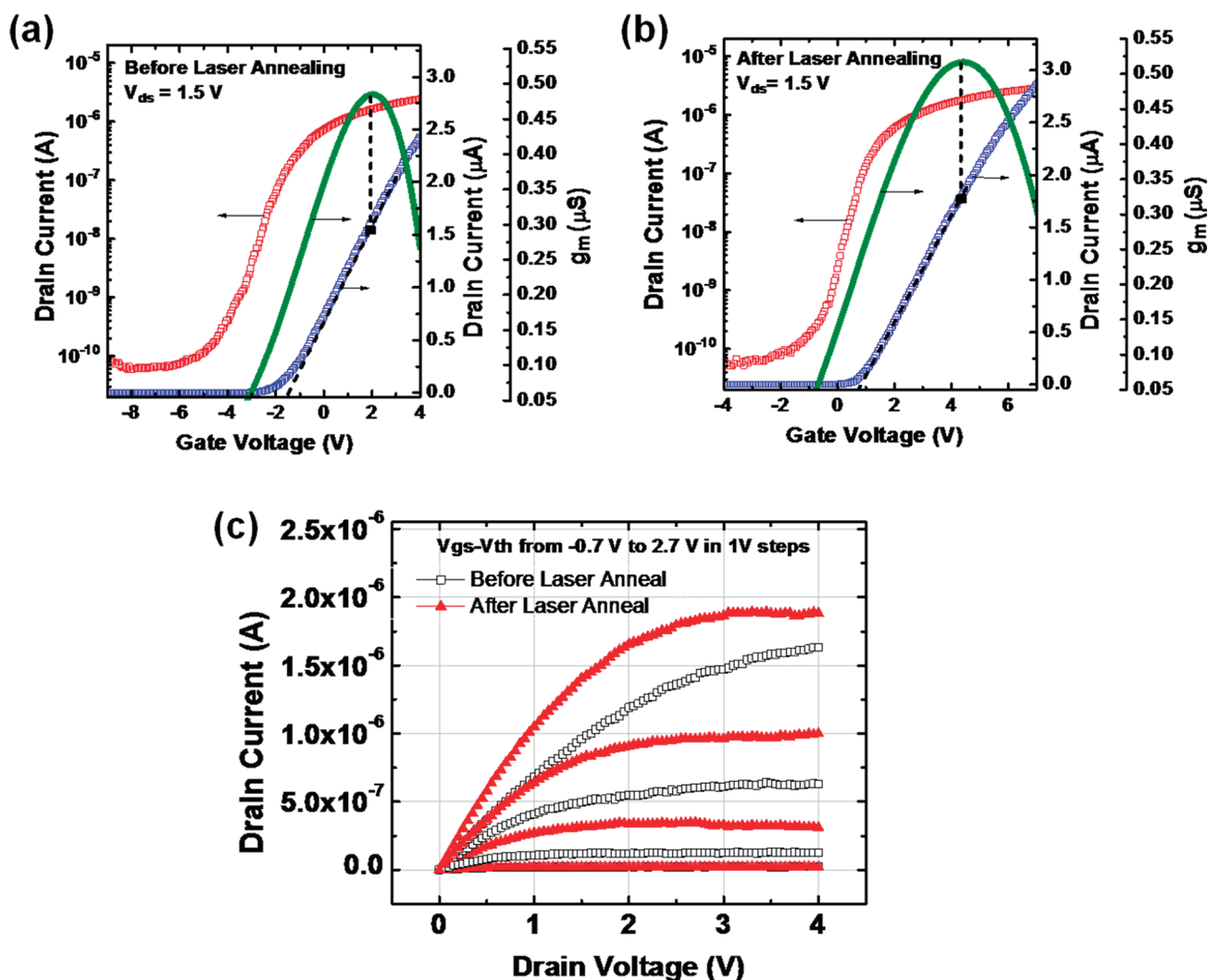
Figure 2. Electrical characteristics of fully transparent In_2O_3 NWT utilizing ITO S-D contacts and glass substrates. The $I_{ds}-V_{gs}$ characteristics of a representative device (a) before and (b) after laser annealing (laser fluence $\sim$0.71 J/cm^2) at V_{ds} = 1.5 V. Blue, red, and green data points correspond to linear—scale $I_{ds}-V_{gs}$ and log-scale $I_{ds}-V_{gs}$ and g_m, respectively. Arrows indicate the appropriate axis. (c) $I_{ds}-V_{ds}$ characteristics for $V_{gs}-V_{th}$ (−0.7 to 2.7 V in 1.0 V steps) for a representative In_2O_3 nanowire transistor before (black square) and after (red triangle) laser annealing.

nanowire transistor. The optical transmission spectrum (Figure 1c) shows transparency >80% in the 350—1500 nm wavelength range through a 1.5 cm × 1.5 cm glass substrate with 20 000 NWT patterns. The inset of Figure 1c shows an optical image of a glass substrate with ~1000 patterned fully transparent NWTs. The image behind the sample is clearly visible. Following initial electrical characterization of the devices, a commercial amplified femtosecond laser system from Spectra-Physics (laser pulse width = 50 fs centered at 800 nm, repetition rate = 1 kHz, objective lens = 100×, NA 0.8, and beam diameter = 1.22 μm) was used to anneal selectively the contact regions of the NWTs. As shown in Figure 1b, a high-precision, three-axis computer-controlled positioning stage was used to move the sample with respect to the laser beam. The sample is scanned at a speed of 1 μm/s under laser energy fluences (LF) varying from 0.14 to 1.08 J/cm^2 (laser transmitted power from 10 to 75 μW), as measured by a power meter. The surface of the sample is monitored in real time using the same objective that focuses the laser beam. Compared with continuous or nanosecond Q-switched lasers, a femtosecond pulse laser provides an ultrashort

pulse-width, extremely high peak power, and capability to produce highly confined heating. Therefore, the femtosecond laser annealing method is expected to control precisely the heating process and selectively anneal the contact regions of the NWTs without significant transfer of heat to unwanted regions. It has also been reported that laser annealing permits localized energy input without affecting the underlying substrates and overcome the incompatibility of thermal annealing to glass and plastic substrates.[19,20]

RESULTS AND DISCUSSION

To investigate the effects of postmetallization source and drain annealing on representative In_2O_3 nanowire transistors, the device electrical characteristics were measured before and after the laser-annealing as shown in Figure 2. Laser fluence (LF) was varied from 0.14 to 0.80 J/cm^2 to illustrate the potential for tuning the device performance metrics. NWTs with ITO contacts irradiated at LF <0.14 J/cm^2 showed negligible changes in the device performance. LF >0.80 J/cm^2 showed evidence of

ITO etching, which is not of our particular interest in this context. Following laser annealing, the transistor characteristics, including on−off current ratio (I_{on}/I_{off}), subthreshold slopes (SS), transconductances (g_m), field-effect mobility (μ_{eff}), low-field channel conductance (G_{ch}), output resistances (r_O), and self-gain (A_v) were improved along with positive shifts in threshold voltages (V_{th}). The transfer characteristics ($I_{ds}-V_{gs}$) for a representative transistor with and without laser annealing ($LF \approx 0.71$ J/cm^2) at $V_{ds} = 1.5$ V are shown in Figure 2a,b. The devices fabricated without laser annealing exhibit on-current (I_{on}) of $\sim$2.43 μA, off-current (I_{off}) of $\sim$58.6 pA, $I_{on}/I_{off} \approx 4.1 \times 10^4$, $V_{th} \approx -1.2$ V, $SS \approx 823$ mV/dec, maximum $g_m \approx 510$ nS, and $\mu_{eff} \approx 95$ cm^2 V^{-1} s^{-1}. After laser annealing treatment, the devices show $V_{th} \approx 0.8$ V, $I_{on} \approx 3.09$ μA, $I_{off} \approx 46.5$ pA, $I_{on}/I_{off} \approx 6.7 \times 10^4$, $SS \approx 624$ mV/dec, maximum $g_m \approx 570$ nS, and $\mu_{eff} \approx 106$ cm^2 V^{-1} s^{-1}. The threshold voltage was obtained by extrapolating the linear portion of the $I_{ds}-V_{gs}$ to zero drain current curves from the point of maximum slope where the transconductance ($g_m = dI_{ds}/dV_{gs}$) is maximal.[21] The μ_{eff} given by the MOSFET model

$$\mu_{eff} = \frac{dI_{ds}}{dV_{gs}} \times \frac{L_{ch}^2}{C_i} \times \frac{1}{V_{ds}} \tag{1}$$

is extracted from the low-field region using a cylinder-on-plate model with gate-to-channel capacitance C_i of

$$C_i = \frac{2\pi\varepsilon_{ox}k_{eff}L_{ch}}{\cosh^{-1}(1 + d_{ox}/r_{nw})} \tag{2}$$

The parameter values were chosen as $k_{eff} \approx 9$, the effective dielectric constant of ALD Al$_2$O$_3$, $L_{ch} \approx 2\,\mu$m, the channel length, and $r_{nw} = 10$ nm, the radius of In$_2$O$_3$ NW. Whereas previous studies reported a temporary shift in threshold voltage of oxide nanowire transistors upon UV or O$_2$ exposure,[22] in the present experiment, a permanent shift in V_{th} is observed after laser annealing.

Figure 2c shows the output characteristics ($I_{ds}-V_{ds}$) of a representative In$_2$O$_3$ nanowire transistor, measured in the as-fabricated state and following laser annealing ($LF \approx 0.71$ J/cm^2). To compare directly the low-field channel conductance and output resistance, we plotted $I_{ds}-V_{ds}$ characteristics at $V_{gs}-V_{th} = -0.7, 0.7, 1.7,$ and 2.7 V for both cases (Figure 2c). Note that the use of $V_{gs}-V_{th}$ adjusts for the positive V_{th} shift ($\sim$2 V) following laser annealing. The $I_{ds}-V_{ds}$ curves of as-fabricated devices deviate significantly from the expected response of a long-channel transistor even at V_{ds} values expected to be in the saturation region ($V_{ds} \geq V_{gs}-V_{th}$). In the as-fabricated state, the device showed a low-field channel conductance (G_{ch}) of $\sim$747 nS at $V_{gs}-V_{th} = 2.7$ V and output resistance of (r_O) ≈ 8.33 MΩ at $V_{gs}-V_{th} = 2.7$ V and $V_{ds} = 4$ V, corresponding to a significant output conductance (g_{ds}) of $\sim$120 nS. G_{ch} was directly measured from the slope of $I_{ds}-V_{ds}$ at small V_{ds}, whereas r_O was measured at large V_{ds}. For low V_{ds}, the measured G_{ch} increases approximately linearly with V_{gs} from V_{th} up to 3.5 V, with no clear sign of saturation due to series resistance (R_s). On the basis of this, an upper bound for R_s ($R_{s,upper}$) ≈ 500 kΩ can be estimated. After annealing, the $I_{ds}-V_{ds}$ curves exhibit a sharper onset of saturation at a lower V_{ds}, increased current and higher r_O in the saturation region, and increased source-drain conductance at low V_{ds}. Note that the onset of current saturation is observed at V_{ds} values close to $V_{gs}-V_{th}$ following laser annealing, consistent with saturation due to pinch-off at the drain end of the channel.

Following laser annealing, G_{ch} increased to 1330 nS at $V_{gs}-V_{th} = 2.7$ V, r_O increased to 14.60 MΩ at $V_{gs}-V_{th} = 2.7$ V and $V_{ds} = 4$ V, and corresponding g_{ds} decreased to 69 nS. The measured G_{ch} again increases with V_{gs} without saturation. Following laser anneal, self-gain ($A_v = g_m r_O$) increased significantly from 4.31 to 8.22 due to improvement in r_O and g_m. Self-gain of $\sim$8.22 obtained in our experiment is comparable to the value reported in 45 nm SOI technology.[23]

$1/f$ noise measurements of the In$_2$O$_3$ nanowire transistors were carried out to study the effect of laser annealing ($LF \approx 0.71$ J/cm^2) on current fluctuations in single-nanowire devices. Measurement of the $1/f$ noise spectrum of the NWTs can derive important information about current transport and fluctuations in the nanowire devices.[24,25] The drain bias was kept at 1.5 V, and the frequency range was varied from 1 Hz to 1.6 kHz. On the basis of the measured $1/f$ noise, one can construct a noise model as follows. According to Hooge's empirical law, the $1/f$ current noise amplitude can be written as

$$\frac{S_I(f)}{I_d^2} = \frac{A}{f^\gamma} = \frac{\alpha_H}{Nf^\gamma} \tag{3}$$

where A is the noise amplitude, $N = LC_i(V_{gs} - V_{th})/q$ is the total number of carriers in NWT channel, α_H is the Hooge's constant, and frequency exponent γ is ideally 1. As derived in Figure 3b, In$_2$O$_3$ NWT before and after contact annealing exhibited $1/f$ noise behavior with the exponent γ values in the range of 0.98 to 1.21, which were extracted from the linear fit of the spectrum. Figure 3b shows the I_d^2 normalized $1/f$ noise spectrum of a single In$_2$O$_3$ NWT biased at $V_{gs}-V_{th} = 3.5$ V prior to and after contact laser annealing. Following laser annealing, the $1/f$ noise spectrum is approximately one order of magnitude smaller than as-fabricated NWTs. The $1/f$ noise in an NWT may contain contributions from (i) excess noise in the metal-nanowire Schottky barrier and (ii) interaction of carriers with charges associated with oxide charges, interface traps, and mobile ions, which can be modified by ambient conditions. In the first case, the room-temperature charge-transport mechanism is governed by thermionic emission, tunneling through the source contact, or both. For our back-gated transistor structure, the barrier is primarily modulated by gate voltage but can also be modulated by the fluctuation of surface charge near the interface and charge density of trap centers located in the space charge region. The resulting fluctuations in the barrier lead to a fluctuation in the current flowing in the channel. To investigate the source of the $1/f$ noise, we plot S_I at 100 Hz and the normalized square of the drain current versus the gate voltage before and after laser annealing in Figure 4b,c. The amplitude of the current noise spectrum (S_I) is found to be proportional to $I_d^2/|V_{gs}-V_{th}|$ in the transistor operating regime, which is similar to that reported in thermionic-emission-dominated devices such as ZnO/SnO$_2$ NWTs and single-walled carbon nanotube (SW−CNT) transistors.[26−28] This proportionality can be expressed as

$$S_I = \frac{AI_d^2}{f} = \frac{\alpha_H I_d^2}{Nf} = \frac{q\alpha_H}{C_i f} \frac{I_d^2}{|V_{gs} - V_{th}|} \tag{4}$$

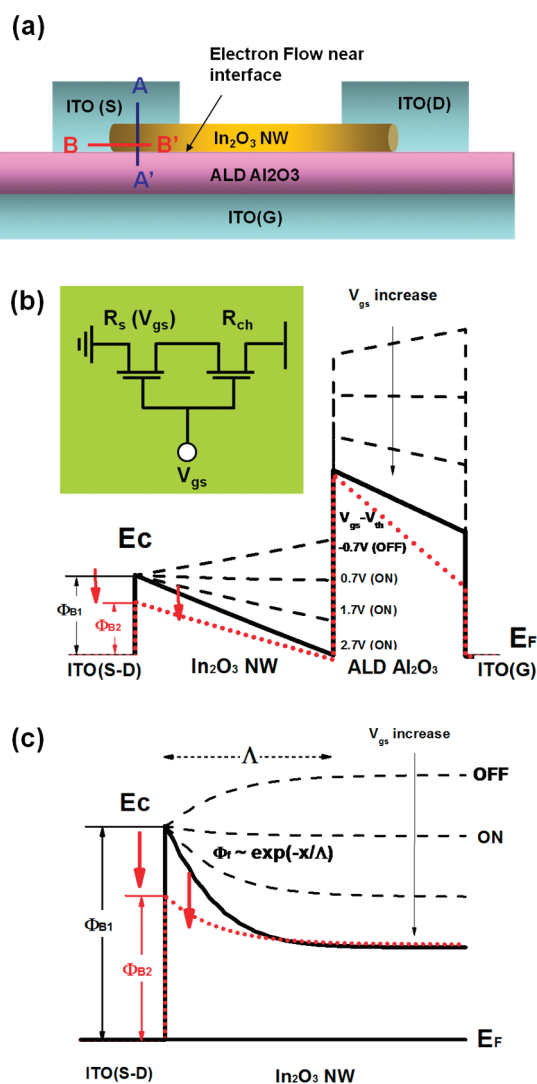The extracted Hooge's constant (α_H) values obtained from eq 4 were $\sim$1.11 $\times$ 10^{-2} and $\sim$6.47 $\times$ 10^{-3} for as-fabricated and laser annealed devices, respectively. The reduction of α_H after laser annealing on the contacts implies that surface charge near the interface and trap centers located in the space charge region is modified, consequently lowering the Schottky barrier height,
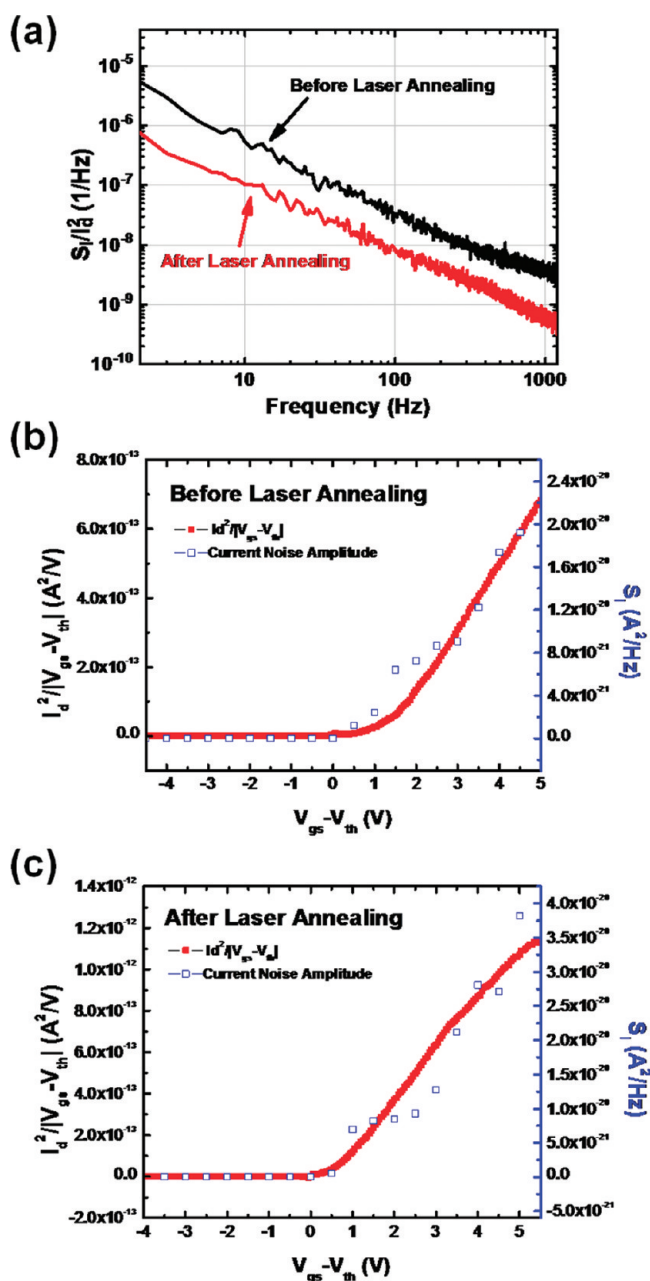
Figure 3. Low-frequency noise measurements. (a) Normalized current noise power as a function of frequency for $(V_{gs}-V_{th}) = 3.5$ V before and after laser annealing. Measured $I_d^2/|V_{gs}-V_{th}|$ and the amplitude of current noise spectrum (at 100 Hz) are plotted as a function of gate bias (b) before and (c) after laser annealing for drain bias of 1.5 V.

Figure 4. Energy band diagram. (a) Cross-sectional view of an In_2O_3 NWT is shown. (b) Band diagram in (b) vertical (A−A′) and (c) horizontal (B−B′) cross sections of both as-fabricated (black solid line) and laser annealed (red dotted line) In_2O_3 NWTs at $V_{gs}-V_{th} = 2.7$ V is drawn using MEDICI. Black dashed lines show the band diagram of as-fabricated NWT for $V_{gs}-V_{th} = -0.7$, 0.7, and 1.7 V. Schottky barrier heights Φ_{B1} and Φ_{B2} are indicated for cases before and after annealing respectively, and the arrows in the band diagrams represent the direction of band bending after annealing.

which is expected to be one of the dominant sources of $1/f$ noise.[28] Despite the high surface-to-volume ratio of nanowires, the obtained value α_H is comparable to the one reported with CMOS FETs using HfO_2 gate insulator.[29,30] This supports the conclusion that optimizing the contact region in NWTs through laser annealing can raise the possibilities of NWTs to be used as the device components beyond the conventional CMOS applications in the point of view of device noise properties.

For conventional Schottky barrier field-effect transistors, thermal annealing is an effective method not only to improve the gate modulation in a transistor by reducing the trap densities and fixed charges at the channel−insulator interface but also to achieve electronic transparent contact by reducing the contact resistance and contact barrier height. It is shown from previous reports that lowering the Schottky barrier height (Φ_B) through removing the voltage−variable interface trap densities and modifying the fixed negative charge densities of nanowire surface between the metal (Al) and nanowire (In_2O_3) interface only at the contact region induces positive shift in V_{th}, reduces SS, and improves on-current of the NWTs.[31] Selective contact laser annealing treatment in the current study is presumably expected to modify the surface structure of nanowires at the contact region to reduce the trap densities, modify the fixed charge densities, and lower Φ_B. Reduction of electron acceptor traps in the source and drain region after laser annealing is presumably the dominant factor responsible for the modest improvement in subthreshold slopes and positively shifted threshold voltages. Furthermore,

reduction in magnitude of Φ_B and increased electronic transparency of the contact region after contact laser annealing appears to be the primary mechanism responsible for the reduction of improvement in on-current, and reduced $1/f$ noise spectrum.

For metal contacts to semiconductor nanowires, the quasi-1D electrostatics in structures with overlaps between the back-gate and contact electrodes can yield a relatively thin barrier where the barrier thickness is determined by the characteristic length given by

$$\Lambda = \sqrt{\frac{\varepsilon_{nw}}{\varepsilon_{ox}} \times d_{nw} \times d_{ox}} \qquad (5)$$

for band bending at the metal—nanowire interface, as illustrated in Figure 4c.[32] In eq 5, d_{nw} is the nanowire diameter and ε_{nw} and ε_{ox} are the dielectric constants of the nanowire and gate dielectric, respectively. For material parameters and dimensions in the current study, Λ is estimated to be ~20 nm. For this range of barrier thicknesses, it is expected that the contact behavior would be dominated by thermionic-field emission,[33] which can yield a relatively linear current—voltage characteristic and relatively high low-field conductance for the M-S contacts. As shown in Figure 4c, the energy band bending at the metal—nanowire junction, near the dielectric interface can be written as

$$\Phi_f(x) = [\Phi_B - q(V_{gs} - V_{ref})]e^{(-x/\Lambda)} + q(V_{gs} - V_{ref}) \qquad (6)$$

where Φ_B is the Schottky barrier height and x is the distance measured from the metal semiconductor interface.[34] This relationship is valid as long as the bands move one-to-one with V_{gs}, which occurs in the subthreshold region and above the threshold when operating in the quantum capacitance limit regime. Because the band-bending at the source/channel (or drain-channel) contact is dependent on the gate potential, the conductance of a contact is expected to vary with gate potential (and perhaps with drain potential), resulting in a voltage-dependent contact conductance. Hence, an NWT with the gate overlapping the S-D contacts (Figure 4a) can be modeled as a transistor in series with a voltage-dependent resistor, effectively a series parasitic transistor operating in the linear region, rather than a simple series resistor or a diode, as shown in the insert of Figure 4b. Assuming a relatively large Φ_B in the as-fabricated device, the contact conductance would be relatively small at a given bias point, resulting in a significant voltage drop across the contact region. Such a voltage drop would decrease the V_{ds} as well as V_{gs} for the main transistor, resulting in a decrease in G_{ch} and an increase in saturation voltage ($V_{D,sat}$), as well as decreases in on current and transconductance. For the annealed device, a lower Φ_B would yield a larger conductance for the parasitic transistor and therefore a larger fraction of the applied drain bias across the nanowire channel. The associated characteristics would correspond more closely to those of the main nanowire channel, and saturation would occur at $V_{ds} = (V_{gs} - V_{th})$.

It is well known that an ultrafast phase transition takes place before the electronic system has time to thermally equilibrate with the lattice when semiconductors are exposed to intense femtosecond laser irradiation due to its ultrashort laser pulse width. The excitation of a critical density of valence band electrons destabilizes the covalent bonding in the crystal, resulting in a structural phase transition.[35,36] Laser fluence in the current study was chosen to be close to the ITO ablation level; therefore, we expect the lattice temperature of the In_2O_3 nanowire to increase up to few hundred Kelvin (lower than the ITO melting

point ~1800 K) upon laser annealing, possibly forming an improved single-crystalline In_2O_3 nanowire structure at the contact regions. Various research groups have reported the Sn doping effect on indium oxide films. The short pulse duration in the current study is also expected to activate Sn from the ITO to create a Sn—O bond with the oxygen at the In_2O_3 nanowire surface, creating oxygen vacancies and modifying the effective doping in the nearby semiconducting channel to form a high conductivity nanowire region at the contacts, consequently lowering the Φ_B along with increased electronic transparency of the contact region.[37] The high peak intensity of the femtosecond laser can induce nonlinear absorption in materials. Because the device structure in the current study consists of materials with band gap (E_G: In_2O_3 nanowire = 2.9 eV, ITO = 4.0 eV, ALD Al_2O_3 = 9.0 eV) larger than the single photon laser energy (~1.55 eV), the contact annealing effect may require nonlinear absorption of the laser (two- or multiphoton absorption). Annealing of these materials with a continuous, nanosecond excimer or picosecond laser would likely require either a shorter wavelength or a much higher power to induce similar effects.

Most of the nanowire transistors reported to date exhibit high drain conductance in the high V_{ds} region. The low r_O makes the devices poorly suited for implementing practical memory/display switching devices because linear regime operation often results in unstable current—voltage relation, leading to inaccurate switching characteristics. Additionally, the higher V_{ds} required for current saturation ($V_{D,sat}$) is not appropriate for low-power applications. Hence, highly saturated currents with earlier onset of saturation in nanowire-based transistors are key elements in implementing practical low-power integrated analog and digital circuitry. Furthermore, to achieve a successful analog circuit application such as RF operation, obtaining high device performance along with high gain (A_v) are major concerns. Our experiment suggests that femtosecond laser-annealing focused at the contact region is a promising tuning method to optimize the device performance, especially in terms of r_O, $V_{D,sat}$, G_{ch}, and A_v suitable for low-power transparent digital and analog circuit applications. The reduction in SS after annealing also suggest that femtosecond laser-annealing selectively focused at the contact region can be useful to trim and tune the SS accompanied by other methods related to channel modification such as ozone treatment and surface passivation.[38]

■ CONCLUSIONS

In conclusion, single In_2O_3 nanowire transistors in which the S-D regions are selectively annealed utilizing femtosecond laser after ITO deposition exhibit significant improvements in performance parameters, especially reduction in $V_{D,sat}$, significant improvement in G_{ch}, improved SS, increased g_m, increased μ_{eff}, improved A_v, along with significant increase in r_O and permanent positive shifts in V_{th}. $1/f$ noise studies reveal that the improvements in device performance are explained in terms of reduction in interfacial traps and corresponding reduction in Schottky barrier height fluctuation at the contacts. Furthermore, femtosecond laser annealing at the contact region shows that low noise densities can be achieved by reducing the interface traps near the contact region. Femtosecond laser annealing is a promising optimization technology for the realization of low-noise and low-power transparent/flexible circuits in terms of both digital and analog applications, which allow low thermal budget processing and drastically reduced processing time. Direct comparison

of device characteristics before and after anneal serves as the basis for a model that is generally applicable to NWTs with overlap between gate region and S-D region. The observed changes in transistor performance, nominally without modifying the channel region, shed light on contact-dominated effects in nanowire transistors.

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