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Materials Science and Engineering B 135 (2006) 282–284

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# GaN metal-oxide-semiconductor field-effect-transistor with atomic layer deposited Al<sub>2</sub>O<sub>3</sub> as gate dielectric

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## Abstract

We report on a GaN metal-oxide-semiconductor field-effect-transistor (MOSFET) using atomic-layer-deposited (ALD) Al<sub>2</sub>O<sub>3</sub> as the gate dielectric. Compared to a GaN metal-semiconductor field-effect-transistor (MESFET) of similar design, the MOSFET exhibits several orders of magnitude lower gate leakage and near three times higher channel current. This implies that the ALD Al<sub>2</sub>O<sub>3</sub>/GaN interface is of high quality and the ALD Al<sub>2</sub>O<sub>3</sub>/GaN MOSFET is of interest and potential for high-power RF and digital applications. In addition, the channel mobility of *n*-GaN layer is ~414 cm<sup>2</sup>/V s, which has not been degraded by ALD Al<sub>2</sub>O<sub>3</sub> growth and device fabrication.

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**Keywords:** Aluminium oxide; Gallium nitride; Metal-oxide-semiconductor structures

## 1. Introduction

GaN is a promising semiconductor electronic material for applications in high-temperature, high-speed and high-power electronics due to its fundamental physical properties such as a wide bandgap and high saturation velocity. Recently, there is a growing interest in exploring GaN metal-oxide-semiconductor field-effect-transistors (MOSFETs) for very large scale integrated circuit (VLSI) or digital applications because GaN devices could provide low off drain currents, excellent transport properties, high-quality epi-layers on Si and material compatibility for Si process temperatures. Furthermore, GaN based electronic devices could find wide applications by integrating with GaN optoelectronic devices. From literatures, there are few works on studying formation of high-quality gate dielectrics on GaN and making high-performance GaN MOSFETs, though significant progress has been made on GaN metal-insulator-semiconductor high-electron-mobility-transistors (MIS-HEMTs) and GaN metal-oxide-semiconductor high-electron-mobility-transistors (MOS-HEMTs) using SiO<sub>2</sub> [1–5], Si<sub>3</sub>N<sub>4</sub> [6,7], Al<sub>2</sub>O<sub>3</sub> [8–10], and other oxides [11,12]. The major motivation on GaN MOSFET research is to realize high-performance enhancement mode or even inversion-type devices with scalable gate dielectrics. Atomic layer deposition

(ALD) is a surface controlled layer-by-layer process for the deposition of thin films with atomic layer accuracy. Each atomic layer formed in the sequential process is a result of saturated surface controlled chemical reactions. The thickness control of the ALD films thus scalability is much superior than those of the plasma-enhanced-chemical-vapor-deposition (PECVD) grown SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub>. The quality of the ALD Al<sub>2</sub>O<sub>3</sub> is also much higher than those deposited by other methods, i.e., sputtering and electron-beam deposition, in terms of uniformity, defect density and stoichiometric ratio of the films. Al<sub>2</sub>O<sub>3</sub> offers additional advantages of a large bandgap (9 eV), high dielectric constant ( $k \sim 8.6$ –10), high breakdown field (10–30 MV/cm), thermal stability, and chemical stability against GaN. Furthermore, ALD is the most promising approach to high-*k* dielectrics (i.e., HfSiON) and given Si industry's familiarity with ALD for frontend processes, the transition to ALD GaN MOSFETs integrated on Si must be easier. The ALD equipment for Al<sub>2</sub>O<sub>3</sub> has demonstrated low defect density, high uniformity, and nanometer scalability. The ALD Al<sub>2</sub>O<sub>3</sub> process is *ex situ*, robust and highly manufacturable. We reported earlier excellent performance of GaAs and InGaAs MOSFETs with ALD Al<sub>2</sub>O<sub>3</sub> [13–15]. We now report similar performance advantages of a depletion-mode Al<sub>2</sub>O<sub>3</sub>/GaN MOSFET.

## 2. Experiments

Fig. 1(a) shows the cross sections of an ALD Al<sub>2</sub>O<sub>3</sub>/GaN MOSFET. A 40 nm undoped AlN buffer layer, a 3 μm undoped

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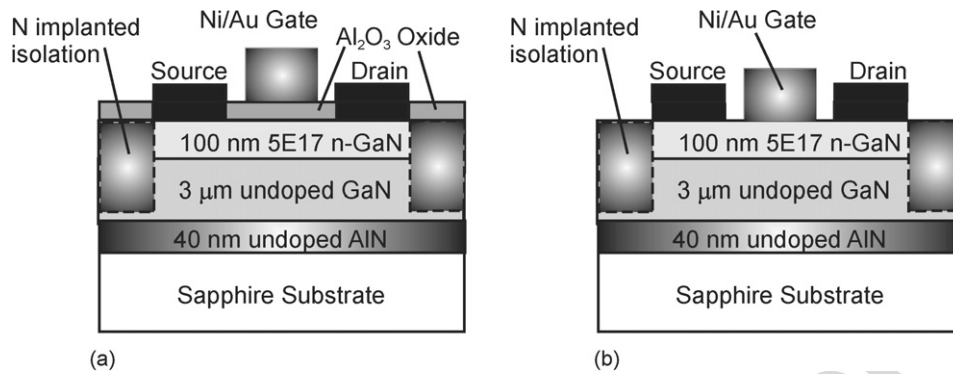


Fig. 1. Cross sections of (a) an ALD  $\text{Al}_2\text{O}_3/\text{GaN}$  MOSFET and (b) a conventional GaN MESFET of similar design.

GaN layer, and a  $100 \text{ nm } 5 \times 10^{17}/\text{cm}^3$  Si-doped GaN layer were sequentially grown by metal-organic chemical vapor deposition on a 2 in. sapphire substrate. After these layers were grown, the wafer was transferred via room ambient to an ASM Pulsar2000<sup>TM</sup> ALD module. A 8 nm-thick  $\text{Al}_2\text{O}_3$  layer was deposited at  $300^\circ\text{C}$  then followed by annealing at  $600^\circ\text{C}$  for 60 s in oxygen ambient. Device isolation was achieved by nitrogen implantation. Using a wet etch in diluted HF, the oxide on the source and drain regions was removed while the gate region was protected by photoresist. Ohmic contacts were formed by electron-beam deposition of Ti/Al/Ni/Au and a lift-off process, followed by an  $850^\circ\text{C}$  rapid thermal annealing (RTA) in a nitrogen ambient, which also activated the previously implanted nitrogen. Finally, Ni/Au metals were e-beam evaporated and lifted off to form the gate electrodes. All four levels of lithography (alignment, isolation, ohmic, and gate) were done by using a contact aligner. The sheet resistance of the source/drain regions of MOSFET and MESFET were measured to be 5300 and 7500  $\Omega/\text{sq}$ , respectively. The gate lengths,  $L_g$ , of the measured devices are 1, 2, 4, 8 and 20  $\mu\text{m}$ . The gate width,  $W_g$ , is 100  $\mu\text{m}$ . The relatively long gate length (i.e., 8 and 20  $\mu\text{m}$ ) is necessary for accurate characterization of the channel mobility, in order to reduce the error in extracting the series resistance. The source-to-gate and the gate-to-drain spacings are 1–2  $\mu\text{m}$ . GaN metal-semiconductor field-effect-transistors (MESFETs) of similar design were also fabricated without ALD insulator formation as shown in Fig. 1(b).

### 3. Results and discussions

Fig. 2 shows the well-behaved  $I$ - $V$  characteristics of a typical GaN MOSFET with a drain bias  $V_{ds}$  of 0–20 V and a gate bias  $V_{gs}$  of –10 to 4 V. The oxide is as thin as 8 nm with the equivalent oxide thickness (EOT) of 3.6 nm. The pinch-off voltage is around –10 V. The maximum drain current density  $I_{ds}/W_g$  at  $V_{gs} = 4 \text{ V}$  is approximately 180 mA/mm, which is about one order of magnitude higher than previously reported  $\text{Gd}_2\text{O}_3/\text{GaN}$  MOSFET. [12] The results indicate that ALD  $\text{Al}_2\text{O}_3$  is an effective gate dielectric for GaN MOSFET. The typical leakage current density for an 8 nm thick ALD  $\text{Al}_2\text{O}_3$  is less than  $10^{-6} \text{ A}/\text{cm}^2$  under gate bias less than 4 V. The process, in particular, the

high temperature ohmic contact annealing at  $850^\circ\text{C}$ , degrades the insulator quality. For a  $1 \times 100 \mu\text{m}^2$  device, the typical gate leakage current is less than  $1 \mu\text{A}$ . It is about four orders of magnitude smaller than drain current and unobservable in the  $I$ - $V$  characteristic as shown in Fig. 2. Using Mo/Al/Mo/Au ohmic contacts with annealing temperature of  $500^\circ\text{C}$  [16] or deposition of ALD insulating films after Ti/Al/Ni/Au ohmic contact formation, it is possible to achieve much less gate leakage current.

Fig. 3 illustrates the saturated ( $V_{ds} = 16 \text{ V}$ ) drain current density and extrinsic transconductance  $g_m$  as a function of gate bias for the GaN MOSFET and the GaN MESFET of similar design. The drain current density of the GaN MESFET (grey line) is limited to 70 mA/mm at  $V_{gs} = 1 \text{ V}$ . The gate leakage current of GaN MESFET becomes unmanageable once the gate bias sweeps above 1 V due to low Ni/n-GaN Schottky barrier. By contrast, the drain current density of the GaN MOSFET (black squares) is 180 mA/mm at  $V_{gs} = 5 \text{ V}$  and can be further increased under higher  $V_{gs}$ . The combination of higher breakdown voltage due to the wide bandgap of GaN and higher drain current by employing gate oxide implies that the output power of the MOSFET can be much higher than that

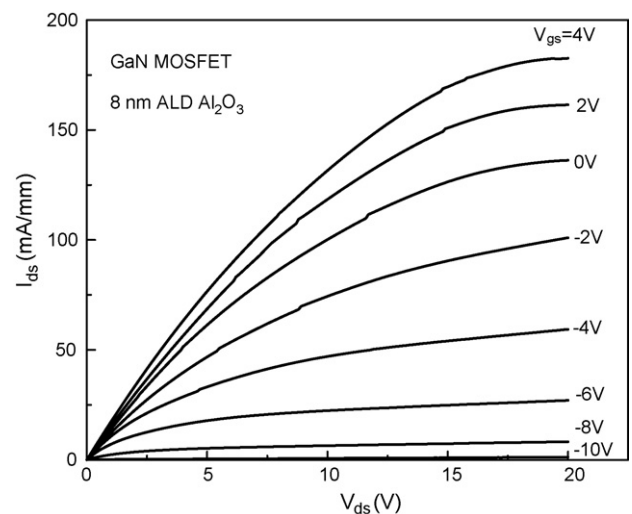


Fig. 2. Measured  $I$ - $V$  characteristics of the GaN MOSFET with 8 nm ALD  $\text{Al}_2\text{O}_3$  as the gate dielectric. The gate length  $L_g = 1 \mu\text{m}$  and the gate width  $W_g = 100 \mu\text{m}$ .

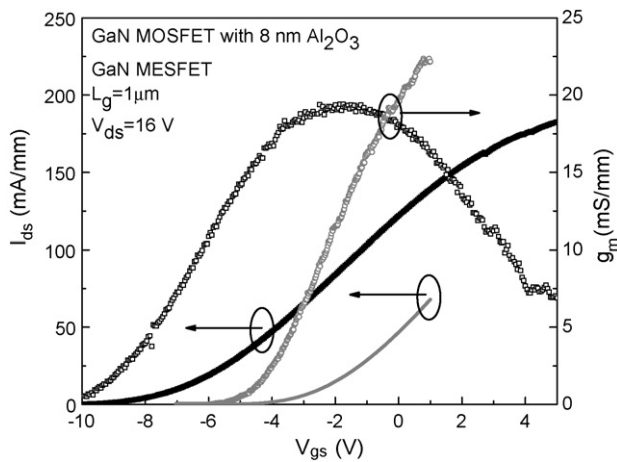


Fig. 3. The transfer and transconductance characteristics measured with the GaN MOSFET ( $I_{ds}$ : solid squares;  $g_m$ : empty squares) and GaN MESFET ( $I_{ds}$ : grey line;  $g_m$ : grey empty circles) in saturation ( $V_{ds} = 16$  V).

of the MESFET. Using  $I_{ds}/W_g = en_s v_{sat} = 200$  mA/mm and the sheet carrier density  $n_s$  of  $5 \times 10^{12}/\text{cm}^2$ , we obtain the saturated velocity  $v_{sat} = 2.5 \times 10^6$  cm/s, which is within the range of values commonly observed for doped GaN bulk channel. Fig. 3 shows that the extrinsic peak  $g_m$  is 20 and 22.5 mS/mm for the MOSFET and the MESFET, respectively. The intrinsic peak  $g_m$  could be calculated from the measured extrinsic transconductance by accounting for the parasitic source resistance  $R_s$  of 33 and 20  $\Omega$  mm for the MOSFET and the MESFET, respectively. The  $R_s$  values were measured on test structures fabricated alongside the MOSFET and the MESFET according to the transmission line method (TLM) or the mobility region of  $I$ - $V$  characteristics of these devices. The peak intrinsic  $g_m$  is about 59 mS/mm for MOSFET and 52 mS/mm for MESFET. The  $g_m$  value for MOSFET is in agreement with theoretical estimation according to  $g_m = v_{sat} C_{MOSFET}$ . Using  $v_{sat} = 2.5 \times 10^6$  cm/s,  $C_{MOSFET} = 18$  pF,  $g_m$  was estimated to be 58 mS/mm for the MOSFET, which is very near the measured value of 59 mS/mm. This also indicates that the interface trap capacitance  $C_{it}$  is very small or near negligible. ALD process enables us to grow high-quality  $\text{Al}_2\text{O}_3$  on GaN with excellent interface quality or low interface trap density  $D_{it}$ .  $C$ - $V$  measurements at 1 MHz on MOS capacitors further confirm the above statement, which shows negligible hysteresis in the loop as the gate bias sweeps between  $-15$  and  $0$  V. Only small hysteresis, less than 150 mV, exhibits when the gate bias sweeps near the flat-band condition (not shown).

Maximum intrinsic  $g_m$  for the long-channel depletion mode MOSFET is given by  $g_m = (W_g/L_g)\mu_n N_d t$ , where  $N_d$  and  $t$  are the doping and thickness of the channel layer,  $\mu_n$  is the channel mobility. For the long-channel devices, i.e.,  $8 \mu\text{m}$ -gate-length and  $100 \mu\text{m}$ -gate-width device, the maximum intrinsic  $g_m$  is obtained to be 4.1 mS. The calculated channel mobility  $\mu_n$  is  $\sim 414 \text{ cm}^2/\text{V s}$ , which is consistent with the recommended value from the GaN epi-vendor. No any significant mobility degradation is observed by ALD  $\text{Al}_2\text{O}_3$  growth and device fabrication.

#### 4. Conclusions

In conclusion, ALD  $\text{Al}_2\text{O}_3$  was proven to be an excellent gate dielectric for GaN MOSFET. The present depletion-mode GaN MOSFET exhibits favorable characteristics when compared to GaN MESFET. The present MOSFET shows low leakage current, high drain current density, high intrinsic transconductance and high channel mobility, compared to previous work reported in literatures. These characteristics imply that ALD is an enabler for high-quality dielectrics on GaN wide-bandgap material and it has excellent potential for high-power RF applications. By realizing enhancement-mode GaN MOSFET using ALD dielectrics, it could open up the new opportunity to explore GaN MOSFETs integrated on Si for digital applications.

#### Acknowledgements

The authors would like to thank H.-J.L. Gossmann and J.C.M. Hwang for helpful discussions and GaN division of Cree Inc. (formerly Advanced Technology Materials, Inc.) for GaN growth.

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