Modulation of the high mobility two-dimensional electrons in Si/SiGe using atomic-layer-deposited gate dielectric

K. Lai[a)]
Department of Electrical Engineering, Princeton University, Princeton, New Jersey 08544

P. D. Ye[b)]
School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907

W. Pan
Sandia National Laboratories, P.O. Box 5800, MS 0601, Albuquerque, New Mexico 87185

D. C. Tsui and S. A. Lyon
Department of Electrical Engineering, Princeton University, Princeton, New Jersey 08544

M. Mühlberger and F. Schäffler
Universität Linz, Institut für Halbleiterphysik, A-4040 Linz, Austria

(Received 21 April 2005; accepted 5 August 2005; published online 28 September 2005)

Metal-oxide-semiconductor field-effect-transistors using atomic-layer-deposited (ALD) Al_2O_3 as the gate dielectric are fabricated on the $Si/Si_{1-x}Ge_x$ heterostructures. The low-temperature carrier density of a two-dimensional electron system (2DES) in the strained Si quantum well can be controllably tuned from 2.5×10^{11} to 4.5×10^{11} cm^{-2}, virtually without any gate leakage current. Magnetotransport data show the homogeneous depletion of 2DES under gate biases. The characteristic of vertical modulation using ALD dielectric is shown to be better than that using Schottky barrier or the SiO_2 dielectric formed by plasma-enhanced chemical-vapor-deposition. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2076439]

Atomic layer deposition (ALD) is a surface controlled layer-by-layer process for the deposition of thin films with atomic layer accuracy. A variety of ALD oxides, such as Al_2O_3, has been intensively studied as high-k gate dielectrics for microelectronic device applications.[1] Similar to SiO_2 and Si_3N_4, Al_2O_3 can significantly reduce the gate leakage current of metal-oxide-semiconductor field-effect-transistors (MOSFETs). Al_2O_3 offers additional advantages of a large band gap (9 eV), high dielectric constant ($k\sim8.6-10$), high breakdown field (10^7 V/cm), and thermal stability (amorphous up to at least 1000 °C). Furthermore, it can be easily removed by wet etching and is robust against interfacial reactions and moisture absorption. On the other hand, the research of ALD Al_2O_3 as the gate dielectric on high mobility two-dimensional electron systems (2DES) has been sparse. A device using the ALD Al_2O_3 as gate dielectric, taking full advantage of its high permittivity, low defect density, high uniformity, conformal step coverage, and moderate growth conditions, can be expected to cause least degradation on the quality of the 2DES and provide physical conditions to study yet unexplored low-temperature two-dimensional (2D) electronic phenomena. Therefore, work combining ALD and high mobility 2DES would fill the existing gap in ALD applications between basic physics research and state-of-the-art microelectronic device research.

Among the various high mobility 2DESs, the system of electrons confined to the strained Si quantum well in the Si/SiGe heterostructure has emerged as a promising system for the study of 2D electron physics due to its increasing sample quality.[2] Very high electron mobility ($\sim500\,000$ cm^2/V s) was reported in this system and strong electron-electron interaction physics phenomena, such as the fractional quantum Hall effect (Refs. 3 and 4) and the 2D metal-insulator transition,[5–7] have been observed. However, the vertical modulation on high mobility n-type Si/SiGe proves to be a formidable task due to the difficulty of fabricating a functional field-effect transistor on the heterostructure material. Schottky gate suffers large gate leakage current and only a limited density tuning range can be achieved.[8,9] At first glance, SiO_2 is the best choice for the gate dielectric. Unfortunately, conventional high-temperature oxidation is not amenable to grow SiO_2 on modulation doped heterostructures, which are grown at much lower temperatures. Low-temperature PECVD grown SiO_2 has relative poor quality, i.e., a large amount of traps in bulk SiO_2 and at the SiO_2/Si interface, compared to thermally oxidized SiO_2. In a previous study, a layer of PECVD oxide with thickness less than 100 nm cannot prevent a leakage path from the gate to the 2D plane.[6] The low quality of this dielectric, mainly due to the large amount of charged traps inside the SiO_2, results in a slow response of the 2DES to the gate bias. As a result, a new gate dielectric material with better electrical properties is needed to modulate the high mobility 2DES in the strained Si quantum well.

In this letter, we report a novel Si/SiGe field-effect transistor (FET) structure using 100 nm ALD Al_2O_3 as the gate dielectric. The low-temperature magnetotransport data show that the 2D carrier density n can be homogeneously depleted from $\sim4.0\times10^{11}$ cm^{-2} to below 2.5×10^{11} cm^{-2} with a few volts of gate bias (V_G) and virtually zero-gate leakage current (I_{leak}). The observed instantaneous response of the 2DES to the change of V_G at $T=0.3$ K and a linear n versus V_G relation manifests the high quality of the ALD dielectric. Results from similar FET structures—using either the Pd Schottky gate or the PECVD SiO_2 as the gate oxide—are listed for

[a)]Electronic mail: klai@princeton.edu
[b)]Electronic mail: yep@purdue.edu

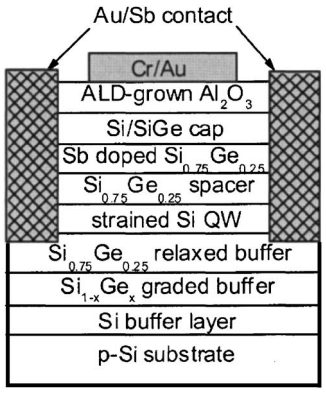

FIG. 1. Schematic view of an *n*-channel Si/SiGe MOSFET with ALD-grown Al_2O_3 as gate dielectric. The thickness of the oxide layer is 100 nm.

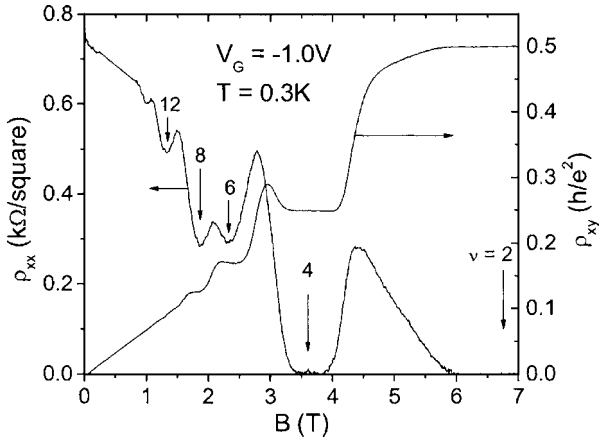

FIG. 2. Longitudinal resistivity ρ_{xx} and Hall resistivity ρ_{xy} as a function of magnetic field at $T=0.3$ K, with an applied front gate voltage $V_G=-1.0$ V. The electron density and mobility are 3.4×10^{11} cm^{-2} and 2.5×10^4 cm^2/V s, respectively. Major integer Quantum Hall states are indicated by arrows. The excitation current I_{ds} is 10 nA.

comparison and the advantage of employing the ALD Al_2O_3 as a gate dielectric is demonstrated.

Figure 1 shows the device structure of the fabricated *n*-Si/SiGe MOSFET. The starting material (with an as-grown electron density $n=4.4\times10^{11}$ cm^{-2} and mobility $\mu=8.0\times10^4$ cm^2/V s) is a modulation doped *n*-type $Si/Si_{1-x}Ge_x$ heterostructure grown by molecular-beam epitaxy. On top of the 100 nm Si buffer grown on a *p*-Si substrate, the relaxed SiGe buffer is realized by a graded layer of 0.5 μm $Si_{1-x}Ge_x$ with the Ge mole fraction x varying from 0 to 0.27. A layer of 2.5 μm thick $Si_{0.75}Ge_{0.25}$ is then grown, followed by a 15 nm strained Si channel, a 12 nm intrinsic $Si_{0.75}Ge_{0.25}$ spacer, a 20 nm doping layer, a 45 nm $Si_{0.75}Ge_{0.25}$, and a 10 nm Si cap layer. After being etched into a 100 μm$\times$320 μm Hall bar, the sample was transferred *ex situ* to an ASM Pulsar2000™ ALD module. A 100 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C, using alternately pulsed chemical precursors of $Al(CH_3)_3$ (the Al precursor) and H_2O (the oxygen precursor) in a carrier N_2 gas flow. The time for one complete Al_2O_3 ALD cycle was typically 12 s with 1 s each reactant exposure and 5 s N_2 purge in between. Each precursor undergoes a self-limiting reaction at the surface, and the Al_2O_3 film is thereby grown with excellent thickness precision and uniformity. The oxide on the contact regions was removed by diluted HF and Ohmic contacts were formed by thermal evaporation of 1% Sb-doped Au and 370 °C anneal in a forming-gas ambient. The front gate was then formed by thermal evaporation of a Cr/Au layer and lift-off process. After FET fabrication, the sample density and mobility were degraded to $n=3.9\times10^{11}$ cm^{-2} and $\mu=5.7\times10^4$ cm^2/V s at zero gate bias. The sample was mounted in a pumped He3 refrigerator at the base temperature of $T=0.3$ K. Standard low-frequency ($\sim$7 Hz) lock-in techniques were employed to measure the diagonal resistivity ρ_{xx} and the Hall resistance ρ_{xy}. A low excitation current, 10 nA, was used throughout the experiments.

Figure 2 shows a low-temperature magnetotransport trace taken at $V_G=-1.0$ V ($n=3.4\times10^{11}$ cm^{-2} and $\mu=2.5\times10^4$ cm^2/V s). The appearance of integer quantum Hall states at Landau level filling factors $\nu=2,4,6,8\ldots$ as both minima in ρ_{xx} and plateaus in ρ_{xy} demonstrates the high quality of the 2DES under gating. The fact that ν changes by an even number is due to the remaining two-fold valley degeneracy in the strained Si system, with a valley-valley splitting too small to be resolved here in the presence of disorder broadening.

Figure 3 illustrates the excellent performance of the ALD Al_2O_3 as a gate dielectric. As the gate voltage is swept from -2.5 V to 2.5 V, virtually no leakage current is detected and no hysteresis for up and down gate sweeps. However, when the 2DES was depleted into the insulating regime (for $V<-2.5$ V and $\rho\geqslant h/e^2$), hysteresis in the gate sweep was seen, presumably due to the breakdown of screening. More remarkably, as shown in the inset of Fig. 3, the 2DES responses to the applied V_G instantaneously and ρ stays constant as the gate bias stops sweeping. As a comparison, when the low-quality PECVD SiO_2 is used as the gate dielectric (see below), the resistance slowly relaxes in a long time scale after V_G stops sweeping.[6]

To further compare the property of the ALD dielectric to that of other gating materials on Si/SiGe, samples with either a Pd Schottky gate or a PECVD SiO_2 gate dielectric

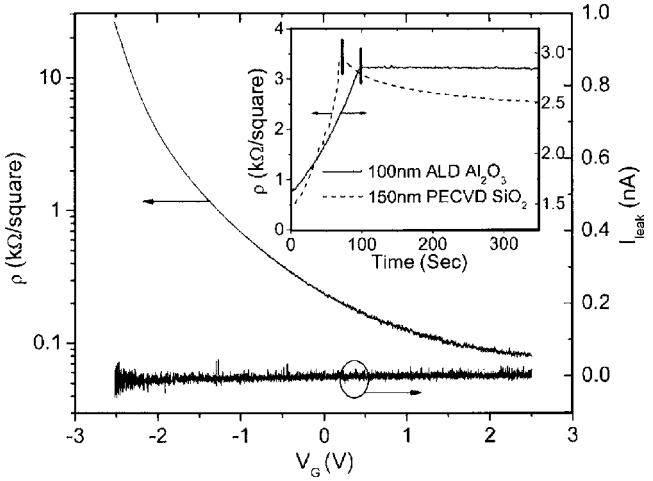

FIG. 3. Four-terminal resistance and the gate leakage current as a function of the gate bias. In the inset, the response of the 2DES to V_G is shown for two metal-oxide-semiconductor devices. For the device with 100 nm ALD Al_2O_3 gate (solid line), V_G sweeps from -1.6 V to -1.9 V in $\sim$100 s and stays -1.9 V afterward. For the device with 150 nm PECVD SiO_2 as gate dielectric (dashed line), V_G sweeps from -8 V to -10 V in $\sim$70 s and keeps constant afterward. The vertical bars show the time when V_G stops sweeping.

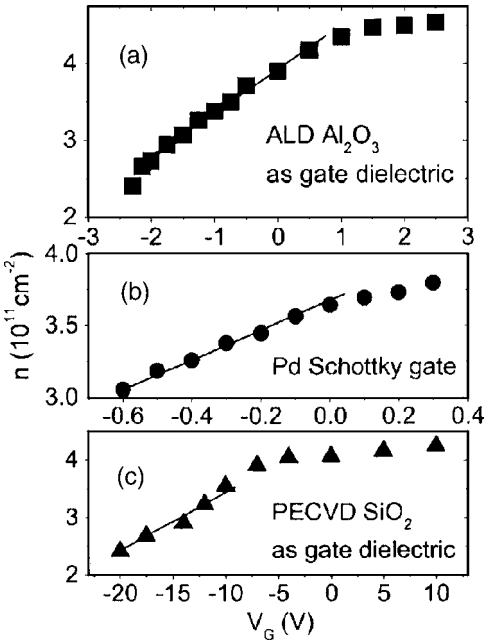

FIG. 4. Carrier density n vs V_G for (a) the 100 nm ALD Al_2O_3 gate, (b) the Pd Schottky gate, and (c) the 150 nm PECVD SiO_2 gate. Straight lines are linear fits to the measured data in the depletion region.

(deposited at 250 °C) were fabricated. Figure 4 shows the n versus V_G relation for the three different gating schemes, in which the carrier densities are determined by both the quantum oscillations of ρ_{xx} and the low-field Hall slopes at 0.3 K. As shown in Fig. 4(a), the carrier density in the ALD sample can be depleted from 4.1×10^{11} cm^{-2} to below 2.5×10^{11} cm^{-2} as a linear function of the applied gate voltage. A slope as high as 0.6×10^{11} cm^{-2}/V is extracted in the linear region, even though the device had not received special surface cleaning before the ALD growth or postgrowth oxide annealing as in the standard ALD MOSFET process.[10] Further experiments are needed in order to understand the interface property between the Si and the ALD Al_2O_3, and it is expected that devices with improved interfaces will bring the capacitance closer to the slope expected of an ideal two-plate capacitor—in this case, $\sim2.8\times10^{11}$ cm^{-2}/V. When the device operates in the accumulation regime with $V_G>0$ V, the data deviate from the linear n versus V_G relation observed for $V_G\leqslant0$ V. This deviation is probably due to the accumulation of charges in the doping layer. For the Pd Schottky gate [Fig. 4(b)], a gate leakage current in the order of 100 pA is detected when $V_G<-0.7$ V and the density can only be reduced to about 3.0×10^{11} cm^{-2}. The data shown in Fig. 4(c) were taken from a similarly fabricated device structure, where a 150 nm PECVD SiO_2 layer was deposited as the gate dielectric instead of 100 nm ALD Al_2O_3. Although the gate leakage current is negligible and the 2D density modulation could also be achieved, the gate oxide shows an inferior characteristic compared to the ALD Al_2O_3. First, a gate bias voltage as high as ±20 V is needed to tune the similar density range, presumably due to the thicker gate oxide, the lower dielectric constant for $SiO_2(\varepsilon_{SiO2}/\varepsilon_{Al2O3}=0.39)$ and much higher trap density in bulk SiO_2 and at the interface. Second, the n versus V_G relation is highly nonlinear even in the depletion side, especially for $-10\text{ V}<V_G<0$ V. A possible origin of this nonlinearity in gate performance is the traps inside the PECVD oxide and at the interface, which screens the electric field from the metallic gate to the 2D plane.

In summary, we have demonstrated a working FET using ALD Al_2O_3 as gate dielectric on a Si/SiGe heterostructure. The electron density in the strained Si quantum well can be tuned linearly and instantaneously by applying a gate voltage. Neither leakage current nor hysteresis for up and down gate sweeps was observed. Similar FET structures using the Schottky barrier or the gate dielectric formed by PECVD SiO_2 are also discussed for comparison and the ALD sample shows the best performance. The experimental technique described above opens up a way to implement ALD oxide as gate dielectrics on high mobility modulation-doped heterostructures and to explore 2D physics in previously inaccessible regimes.

The authors thank J. J. Wang and G. D. Wilk for technical support on ALD growth, and K. Yao and X. Bo for PECVD SiO_2 growth. The work at Princeton University was supported by the AFOSR under Grant No. 0190GFB463 and the NSF under Grant No. DMR0352533. The part of the work carried out in Linz was supported by GMe and FWF under Grant No. P16223–N08.

[1] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
[2] For a recent review of high mobility Si and Ge structures, see, for example, F. Schäffler, Semicond. Sci. Technol. **12**, 1515 (1997).
[3] R. B. Dunford, R. Newbury, F. F. Fang, R. G. Clark, R. P. Starrett, J. O. Chu, K. E. Ismail, and B. S. Meyerson, Solid State Commun. **96**, 57 (1995).
[4] K. Lai, W. Pan, D. C. Tsui, S. A. Lyon, M. Mühlberger, and F. Schäffler, Phys. Rev. Lett. **93**, 156805 (2004).
[5] E. B. Olshanetsky, V. Renard, Z. D. Kvon, J. C. Portal, N. J. Woods, J. Zhang, and J. J. Harris, Phys. Rev. B **68**, 085304 (2003).
[6] K. Lai, W. Pan, T. C. Tsui, and Y. H. Xie, Appl. Phys. Lett. **84**, 302 (2004).
[7] K. Lai, W. Pan, D. C. Tsui, S. A. Lyon, M. Mühlberger, and F. Schäffler, Phys. Rev. B **72**, 081313 (2005).
[8] K. Ismail, M. Arafa, F. Stern, J. O. Chu, and B. S. Meyerson, Appl. Phys. Lett. **66**, 842 (1995).
[9] R. B. Dunford, N. Griffin, D. J. Paul, M. Pepper, D. J. Robbins, A. C. Churchill, and W. Y. Leong, Thin Solid Films **369**, 316 (2000).
[10] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.-J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. K. Ng, and J. Bude, IEEE Electron Device Lett. **24**, 209 (2003).