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Electronic transport in InGaAs/Al_2O_3 nFinFETs

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Abstract

Based on the multiple subbands quasi-ballistic transport theory, we investigate the electronic transport of nano size $In_{0.53}Ga_{0.47}As$ nFinFETs with Al_2O_3 gate dielectric, emphasizing the saturation current region. 1D mobile charge density and gate capacitance density are introduced for the first time to describe the nano-FinFET transport property under volume inversion. With the extracted effective channel mobility of electrons in the linear region from our experiments, the electron mean free path λ in the channel with the value of 5–9 nm is obtained. With only one fitting parameter $\alpha = 0.31$ for the critical length $l = L\left(\frac{kT/q}{V_d}\right)^{\alpha}$ in the quasi-ballistic transport theory, the calculated drain current can fit all experimental data for various gate voltage V_g, source–drain voltage V_d, and temperature (240–332 K) in overall very good agreement. The backscattering coefficient r in the saturation region is larger than 0.8, indicating a large room for improvement for the present InGaAs FinFET technology and performance.

Keywords: $In_{0.53}Ga_{0.47}As$ nFinFET, quasi ballistic transport, quantum capacitance, back-scattering coefficient, critical length

(Some figures may appear in colour only in the online journal)

1. Introduction

InGaAs compound semiconductor as a promising candidate to replace silicon as channel material in n-MOSFETs has attracted great attention recently due to its high electron mobility [1–8]. The new FinFET structure demonstrates its excellent gate control capability which suppresses the short channel effect effectively [9]. However, only few works have been reported on the electrical characteristics of InGaAs FinFET [2, 7, 8, 10].

This paper is an extension of [10] to investigate the transport property of $In_{0.53}Ga_{0.47}As$ nFinFET with fin width $W_{Fin} = 40$ nm, fin height $H_{Fin} = 40$ nm, channel length $L = 100$ nm, Al_2O_3 gate dielectric thickness of 5 nm, in the high V_d (saturation) region. Based on the quasi-ballistic transport theory [11, 12] and the extracted electron channel mobility from our experimental data in the linear region, the electron mean free path, the backscattering coefficient, and the critical length of the InGaAs nFinFETs are discussed. The calculated drain currents are in good overall agreement with the experimental results for various V_g and V_d, and at different temperatures (240–332 K). The details on the device structure and fabrication process can be found in [7].

2. The characterization methodology

2.1. General considerations

The following points should be considered for our specific InGaAs nFinFET devices. (1) The conventional drift-diffusive transport model is not a rational starting point to characterize high mobility short channel InGaAs FETs. The quasi-

ballistic transport theory developed by Lundstrom *et al* is a good starting point [11, 12] to be used in this work. (2) For Fin body of $W_{Fin} = 40$ nm, $H_{Fin} = 40$ nm, and electron effective mass of $In_{0.53}Ga_{0.47}As$, $m^* = 0.043\ m_o$ [13], electron quantum confinement effect should be considered. However, the quantized energy splitting is small and multiple subbands rather than one subband should be considered in the model. (3) The gate capacitance C_G cannot be measured accurately due to the high density of interface traps [14] and very small gate area of the FinFET. The C_G consisting of the oxide capacitance C_{OX} and quantum capacitance C_Q is estimated by careful simulation. (4) For nano FinFET under volume inversion, 1D line densities of mobile charge Q_n and gate capacitance C_G along the channel direction are introduced [10]. They are more appropriate than the 2D surface density of mobile charge and gate capacitance used in the conventional MOSFET modeling to describe nano InGaAs FinFET devices.

2.2. Electron quantization, volume versus surface inversion

Two methods have been used for the electron quantization calculations.

(1) Flat bottom well (FBW) with infinitely high barrier approximation, the quantized energies E_i can be expressed by [15]:

$$E_i = \frac{i^2\pi^2\hbar^2}{2m^*L^2},\ i = 1,2,3... \tag{1}$$

(2) Numerical solution of Schrödinger equation with the bent bottom of conduction band (BBB) obtained by Synopsys Sentaurus Device simulation tool for the FinFET structure. This method is denoted by BBB method.

Figure 1(a) shows the geometry of the FinFET with 40 nm fin width, 40 nm fin height and 100 nm fin length. Figure 1(b) shows the bottom of the conduction band $E_C(Z)$ profile in the FinFET channel. Using this $E_C(Z)$ with infinitely high barrier approximation at two interface sites Z = 0 and 40 nm, the quantized energies E_i and the wave functions $\psi_i(Z)$ can be obtained by numerical solution of the Schrödinger equation. The wave functions shown in figure 1(c) indicate volume inversion in the channel. The quantized energies obtained by BBB method are quite close to the E_i obtained by the FBW approximation as shown in figure 2. Both methods obtain very close results of calculations in the following sections.

2.3. The cyclic coupled equations loop

Denote $Q(0)$ as the 1D line density of mobile charge along the channel length at the top of the source–channel barrier. Modifying the equation of $Q(0)$ in [12] for one subband 2D surface mobile charge density to multiple subbands 1D line mobile charge density, $Q(0)$ can be expressed by:

$$\begin{aligned} Q(0) &= \sum_{i=1}^{\infty} Q_i(0) \\ &= \frac{1}{2} qH_{Fin}N_{2D} \\ &\times \sum_{i=1}^{\infty} \left((1+r)\mathcal{J}_0\left(\eta_F^i\right) + (1-r)\mathcal{J}_0\left(\eta_F^i - \frac{qV_d}{k_BT}\right)\right) \end{aligned} \tag{2}$$

$$N_{2D} = \frac{m^*k_BT}{\pi\hbar^2} \tag{2a}$$

here $\eta^i_{\ F} = \left(E_f - E_i\right)/k_BT$, E_f is the Fermi level, E_i is the bottom energy of the ith subband. $\mathcal{J}_j(\eta_F)$ is the jth Fermi–Dirac integral [16]. The drain current I_d in [12] can be modified to:

$$\begin{aligned} I_d &= \left\langle v_{thermal}\right\rangle \left(\frac{1-r}{1+r}\right) \\ &\times \sum_{i=1}^{\infty} \left[Q_i(0) \cdot \frac{\mathcal{J}_{1/2}\left(\eta^i_{\ F}\right)}{\mathcal{J}_0\left(\eta^i_{\ F}\right)} \right] \\ &\times \left[\frac{1 - \dfrac{\mathcal{J}_{1/2}\left(\eta^i_{\ F} - qV_d/k_BT\right)}{\mathcal{J}_{1/2}\left(\eta^i_{\ F}\right)}}{1 + \left(\dfrac{1-r}{1+r}\right)\dfrac{\mathcal{J}_0\left(\eta^i_{\ F} - qV_d/k_BT\right)}{\mathcal{J}_0\left(\eta^i_{\ F}\right)}} \right] \end{aligned} \tag{3}$$

where $<v_{thermal}>$ is the electron thermal velocity

$$\left\langle v_{thermal}\right\rangle = \sqrt{\frac{2k_BT}{\pi m_n^*}}$$

r is the back scattering coefficient which is defined as [11, 12]

$$r = \frac{l}{l+\lambda} \tag{4}$$

with l the critical length:

$$l = Min\left[L, L\left(\frac{k_BT/q}{V_d}\right)^{\alpha}\right] \tag{5}$$

α is a fitting parameter related to the potential variation profile along the channel direction [12], and λ is the electron mean free path [10]:

$$\lambda = \frac{(2kT/q)\tilde{\mu}_n}{\left\langle v_{thermal}\right\rangle} \frac{\sum_{i=1}^{\infty} \mathcal{J}_0\left(\eta_F^i\right)}{\sum_{i=1}^{\infty} \mathcal{J}_{-1/2}\left(\eta_F^i\right)} \tag{6}$$

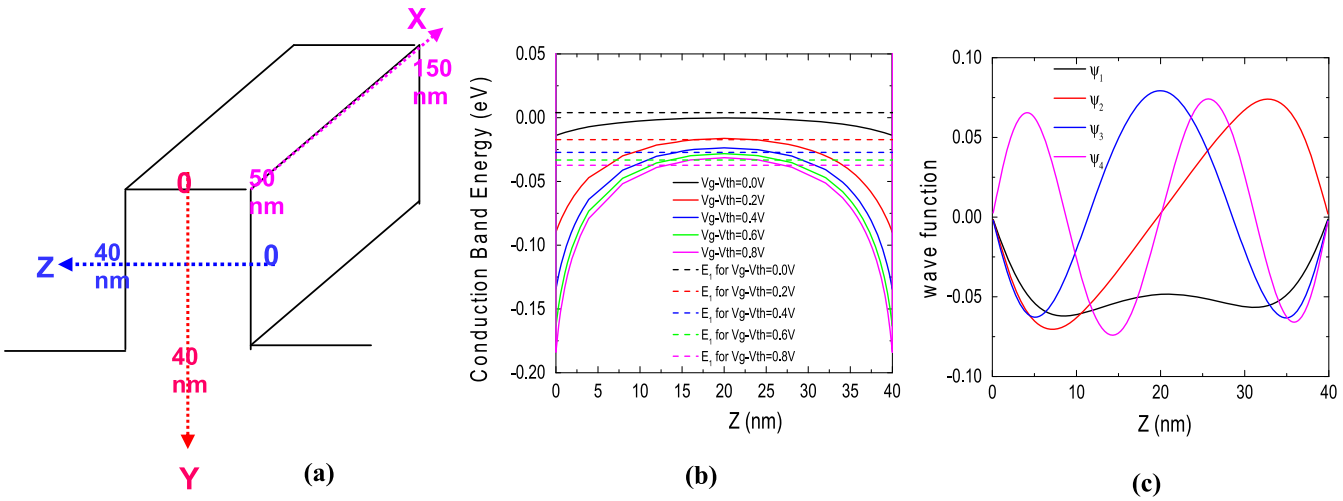

Figure 1. (a) The FinFET geometry, (b) the bottom of the conduction band $E_C(Z)$ profile extracted at $Y = 20$ nm, $X = 60$ nm, by Synopsys Sentaurus Device simulation at $V_d = 0.1$ V, and different V_g–V_{th}. The lowest quantized energy E_1 at different V_g bias is also shown. (c) The wave function distribution of the lowest 4 subbands for V_g–$V_{th} = 0.8$ V, indicating volume inversion rather than surface inversion in the channel.

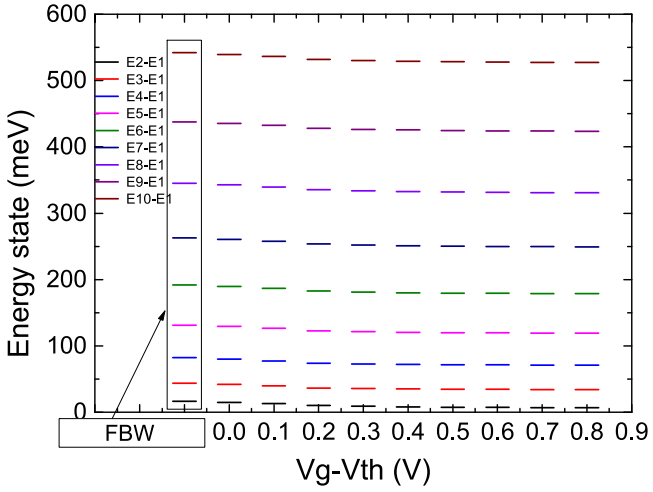

Figure 2. Comparison of quantized energies E_i calculated by FBW and BBB methods, respectively. FBW method is very simple, however, with reasonable accuracy.

In the saturation region $I_{d,saturation}$ in (3) is reduced to

$$I_{d,\text{saturation}} \approx \langle v_{\text{thermal}} \rangle \left(\frac{1-r}{1+r}\right) \sum_{i=1}^{\infty} \left(Q_i(0) \frac{\mathcal{J}_{1/2}(\eta^i_F)}{\mathcal{J}_0(\eta^i_F)} \right)$$
$$= \frac{(1-r)}{2} q N_{2D} H_{\text{Fin}} \langle v_{\text{thermal}} \rangle \sum_{i=1}^{\infty} \mathcal{J}_{1/2}(\eta^i_F) \quad (3S)$$

To compare I_d calculated by (3) with the experimental data of I_d as functions of V_g and V_d, the relationship between V_g and η_F^1 can be obtained by using the following procedure. Since a change in the gate voltage dV_g induces a change in the Fin inversion potential dV_Q by

$$dV_Q = (C_G/C_Q)\, dV_g, \quad (7)$$

here C_G is the line density for the 1D gate capacitance which consists of two components in series:

$$C_G(V) = \frac{C_{OX} C_Q}{C_{OX} + C_Q} \quad (8)$$

The line density for the 1D oxide capacitance C_{OX} with Al_2O_3 of thickness $t_{OX} = 5$ nm and dielectric constant $\varepsilon_{Al_2O_3} = 8$ [17] is

$$C_{OX} = \frac{\varepsilon_{Al_2O_3}\varepsilon_0 (W_{\text{Fin}} + 2H_{\text{Fin}})}{t_{ox}}$$
$$= (14 fF/\mu m^2)(W_{\text{Fin}} + 2H_{\text{Fin}}) = 1.70 fF/\mu m \quad (9)$$

The line density for the 1D quantum capacitance C_Q shown in (7) and (8) is the derivative of 1D charge density in the channel with respect to surface potential V_Q. By (2), we have

$$C_Q = \frac{q^2 m^*}{2\pi h^2} H_{\text{Fin}}$$
$$\times \sum_{i=1}^{\infty} \left((1+r)\mathcal{J}_{-1}(\eta^i_F) + (1-r)\mathcal{J}_{-1}\left(\eta^i_F - \frac{qV_d}{k_B T}\right) \right)$$
$$= (1.15 \text{fF}/\mu\text{m})$$
$$\times \sum_{i=1}^{\infty} \left((1+r)\mathcal{J}_{-1}(\eta^i_F) + (1-r)\mathcal{J}_{-1}\left(\eta^i_F - \frac{qV_d}{k_B T}\right) \right) \quad (10)$$

Note that when V_d is high, the surface inversion potential V_Q and charge density Q are not uniform along the channel. Therefore in (2) and (10), Q(0) and $V_Q(0)$ represent respectively the 1D charge density and the surface potential at the channel locating at the top of the source-channel barrier. Integrating (7) in both sides, we obtain

$$V_g(\eta_F^1) - V_{\text{th}} = \int_{\eta^1_{Fth}}^{\eta^1_F} \frac{C_Q kT}{qC_G} d\eta_F \quad (11)$$

where η^1_{Fth} represents the η^1_F when the gate voltage equals the

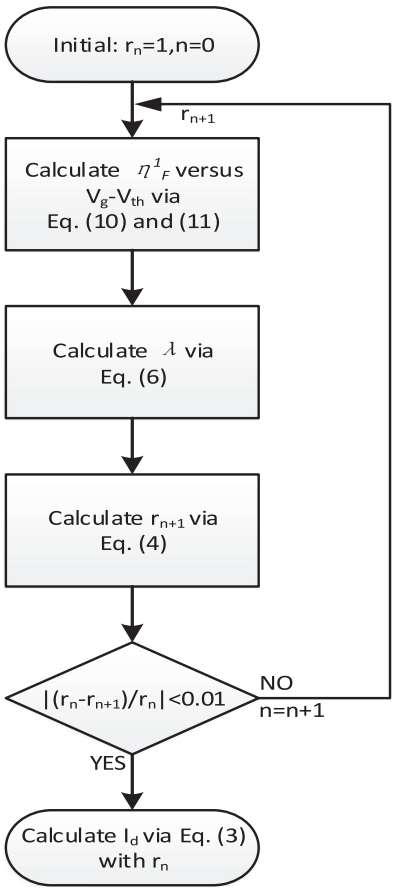

Figure 3. The flow diagram of calculation of equations (3), (4), (6), (10), and (11).

threshold voltage V_{th} and the electron 2D density in the channel is about $10^{11}\,\text{cm}^{-2}$ [18].

Equations (4), (6), (10), and (11) are cyclic coupled. They can be solved by iteration procedure with the initial condition $r = 1$, with very rapid convergence. The converged r and η_F^i values are substituted into (3) to calculate the I_{d}. Figure 3 shows the calculation flow diagram of the iteration procedure.

3. Calculation results compared with our experiments

Figure 4 shows the 1D charge density $Q(0)$ calculated by traditional method in Si MOSFETs [19],

$$Q\,(0) = C_{\text{OX}}\left(V_{\text{g}}–V_{\text{th}}\right), \tag{12}$$

and by our model of equations (2), (8), (9), (10), and (11). The large difference between two methods is due to the small effective mass and therefore small quantum capacitance of the InGaAs channel. Figure 3 indicates a heavy overestimation of the channel mobile charge density and therefore an underestimation of the extracted channel mobility using (12).

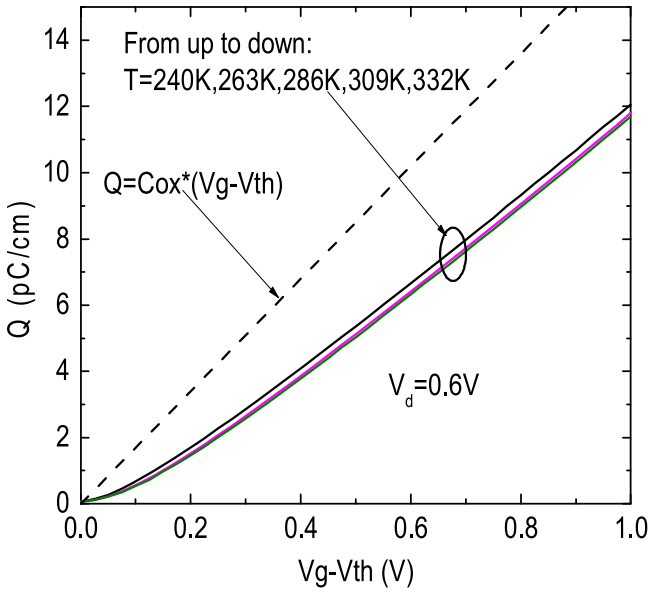

Figure 4. Comparison of 1D charge density calculated by $C_{\text{OX}}(V_{\text{g}}–V_{\text{th}})$ (dashed line) and our model (solid lines). $W_{\text{Fin}} = 40$ nm, $H_{\text{Fin}} = 40$ nm, $L = 100$ nm, and $t_{\text{OX}} = 5$ nm.

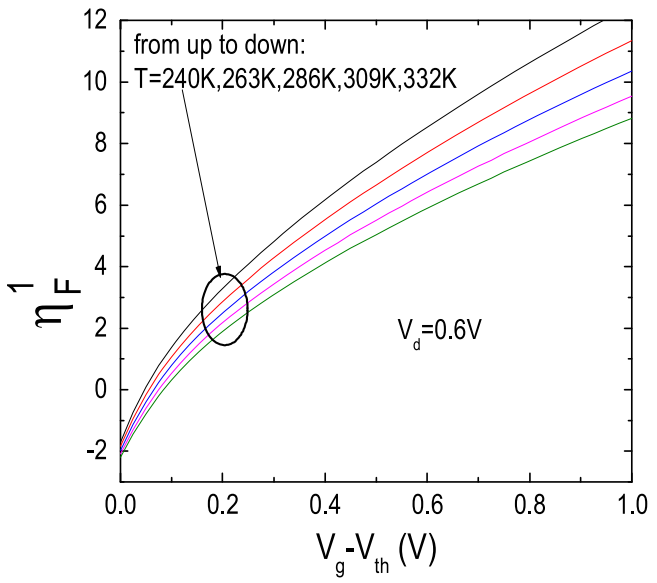

Figure 5. The calculated η_F^I at different gate voltage and temperature using (10) and (11).

3.1. The cyclic coupled equations loop solved by iteration

Figure 5 shows the calculated Fermi level η_F^I versus $(V_{\text{g}}–V_{\text{th}})$ at different temperature. The η_F^I increases more slowly with V_{g} when V_{g} is larger. This reflects that when V_{g} increases, more subbands are occupied and the quantum capacitance increases. The electron mean free path λ can be calculated by (6) using the μ_{n} values obtained in [10]. The results are shown in figure 6.

3.2. Comparison with the experiments—the DIBL effect

To compare with experimental $I_{\text{d}}–V_{\text{d}}$ curve with fixed V_{g}, DIBL effect must be considered since the threshold voltage

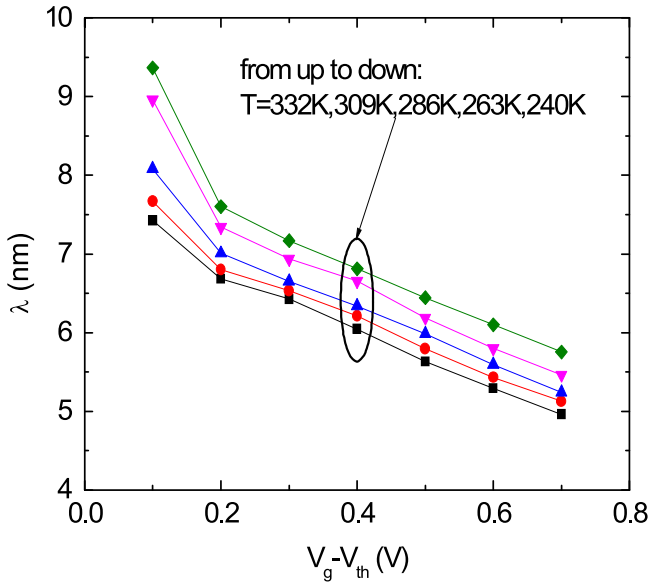

Figure 6. The electron mean free path λ in the $In_{0.53}Ga_{0.47}As$ nFinFET channel calculated by (6) and the channel mobility μ_n obtained in [10]. $V_d = 0.6$ V.

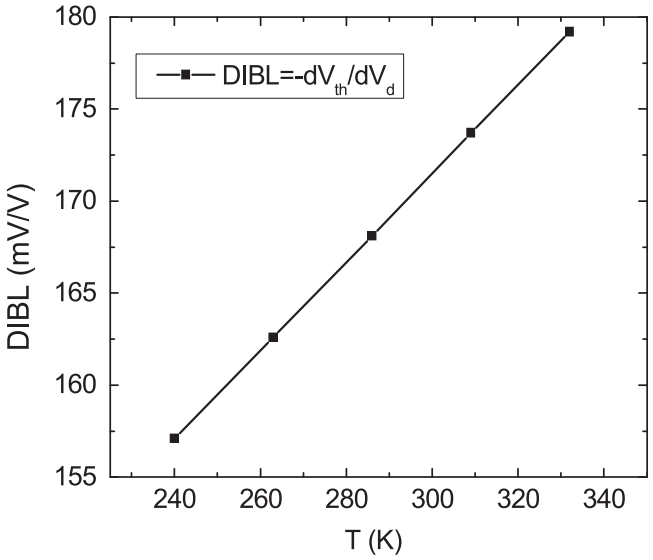

Figure 7. $DIBL = -dV_{th}/dV_d$ extracted from I_d–V_g curves of $In_{0.53}Ga_{0.47}As$ nFinFET with $L = 100$ nm at different temperatures.

V_{th} decreases with increasing V_d. Figure 7 shows the DIBL as a function of temperature extracted from the measured I_d–V_g data with different V_d. Consequently, in the conventional I_d–V_d plot, each measured I_d–V_d curve with fixed V_g has larger V_g–V_{th} value when V_d is larger. Correspondingly, η_F^l is larger, while λ is smaller. On the other hand, parameter α in (5) is adjusted to fit all calculated I_d at different V_g, V_d, and temperature T to get an overall agreement with experimental data. When $\alpha = 0.31$, the calculated I_d using (3) and the measured I_d curves are shown in figures 8(a) and (b). The calculated results show overall good agreement with experimental I_d for various V_g, V_d, and temperature.

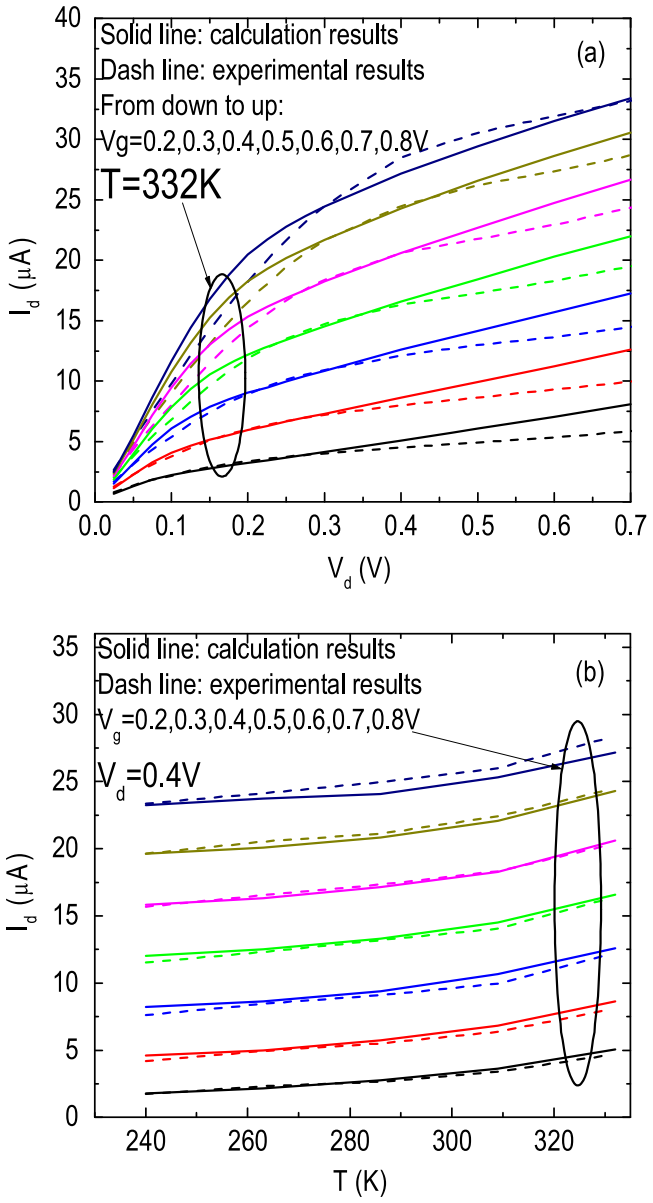

Figure 8. Comparison of calculated drain current I_d (solid lines) and experimental results (dashed lines) of $In_{0.53}Ga_{0.47}As$ nFinFET with $W_{Fin} = 40$ nm, $H_{Fin} = 40$ nm, $L = 100$ nm, $t_{OX} = 5$ nm. The experimental results are measured by Agilent 4156C and after source-drain resistance correction [20]. (a) I_d–V_d curves at $T = 332$ K. (b) I_d at $V_d = 0.4$ V at different V_g and different temperatures.

3.3. Back-scattering coefficient in the saturation region

Figure 9 shows the backscattering coefficient r and the critical length in the saturation region. In the present $In_{0.53}Ga_{0.47}As$ nFinFET with 100 nm channel length, the r is higher than 0.8, indicating a large potential of improvement can be made for the $In_{0.53}Ga_{0.47}As$ nFinFET technology and performance.

4. Discussion

The short mean free paths and the abnormal phenomenon that λ increases with increasing temperature, as indicated in

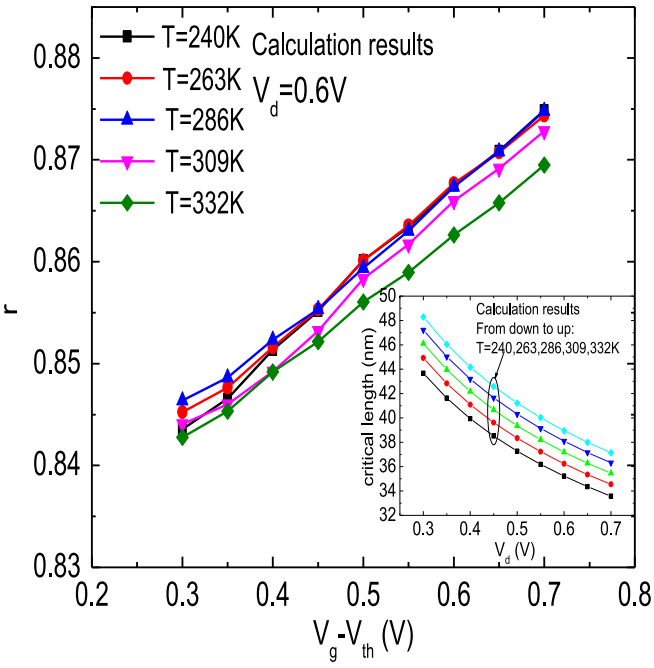

Figure 9. The calculated backscattering coefficient r defined in (4), (5) with $V_d = 0.6$ V, using the experimental mean free path λ in figure 6, the critical length $l = L\left(\frac{k_B T/q}{V_d}\right)^{0.31}$ and channel length $L = 100$ nm. The inset is the critical length versus V_d and T.

figure 6, are probably due to the existence of a high density of acceptor interface traps and border oxide traps in the conduction band of $In_{0.53}Ga_{0.47}As$ in the $InGaAs/Al_2O_3$ interface. The high density of traps in the $InGaAs/Al_2O_3$ interface has been reported by many researchers reflecting in dispersion of C–V curves [14, 21], larger than ideal subthreshold slope [14, 22], Fermi pinning and mobility degradation [23] or directly measurements by charge pumping [14, 22] or C–V [24] methods. There are two effects of these traps to the mobility or mean free path assessment: (1) the high density of traps may respond to the charge density induced by V_g. As a result, the real mobile charge density and therefore the measured I_d are reduced. Zhu *et al* [25] have developed a method of correction to estimate the real mobile charge density out of high density of interface trap charge. (2) The charged traps induce additional Coulomb scattering mobility component $\mu_{Coulomb}$, which increases with increasing temperature [19]. It is consistent with our experimental result. Therefore, the method stated in this paper underestimates the real mobility and mean free path since we have not considered the trap effect. We would not follow the method in [25] since we cannot measure the gate capacitance, and higher real mobility is actually not beneficial to higher I_d. We would rather follow the conventional mobility studies [26–28], and ascribe the degraded effective mobility to the existence of high acceptor trap density. The results shown in this work indicate that there is a large room to improve the present InGaAs n-FinFET fabrication technology by improving the InGaAs/dielectric interface to reduce the acceptor like interface trap and border trap energy densities in the InGaAs conduction band.

The agreement between calculated and experimental I–V curves in figure 8 is not perfect at higher V_d. This may reflect that introducing a critical length with only one parameter α in (5) is not accurate enough and could be further improved. On the other hand, the DIBL constants shown in figure 7 are sensitive to the slope of the curves at high V_d range, but may introduce some errors or uncertainty by different methods to extract the V_{th} from the I–V curves.

5. Conclusion

The multiple subbands quasi-ballistic transport theory is used to characterize the nano $In_{0.53}Ga_{0.47}As/Al_2O_3$ nFinFET, emphasizing the saturation region. 1D mobile charge density and gate capacitance density are adopted to describe the electron transport property in the channel under volume inversion. The quantum capacitance, which plays a more important role in estimating the mobile charge density than in Si MOSFET with the same scaling geometry, due to much smaller electron effective mass in InGaAs, is carefully modeled. The electron mean free path in the channel is in the range of 5–9 nm. The critical length, and the backscattering coefficients in the saturation region are evaluated. The calculated drain currents I_d with only one fitting parameter $\alpha = 0.31$ for the critical length $l = L\left(\frac{kT/q}{V_d}\right)^{\alpha}$ are in overall good agreement with all experimental data with various V_g, V_d, and temperature. The backscattering coefficient at the saturation region is larger than 0.8, indicating large room for improvement for InGaAs nMOSFETs technology and performance.

Acknowledgement

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