High-Performance In_2O_3-Based 1T1R FET for BEOL Memory Application

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***Abstract*— In this article, we report high-performance one-transistor-one-resistor (1T1R) FETs for nonvolatile memory application based on nanometer-thick indium oxide (In_2O_3) as channel material deposited by atomic layer deposition (ALD). ALD grown hafnium oxide (HfO_2) and aluminum oxide (Al_2O_3) are used as gate dielectrics as well as insulator in resistive part. Two nonvolatile states with different threshold voltages are realized. High $I_{ON}/I_{OFF} > 10^{10}$ at $V_{GS} = 0$ V, large memory window (MW) exceeding 10 V, and deep sub-60-mV/dec subthreshold slope (SS) are achieved on ALD In_2O_3 1T1R FETs. Channel length (L_{ch}) and channel thickness (T_{ch}) dependence of device properties are systematically investigated. Optimized In_2O_3 thickness is determined to 1.2 nm, balancing I_{ON}/I_{OFF}, MW, device variation, and stability. The fabrication process has a low thermal budget below 225 °C. Thus, these 1T1R FETs are back-end-of-line (BEOL) compatible and promising for monolithic 3-D integration to realize near-/in-memory computing.**

***Index Terms*— Atomic layer deposition (ALD), back-end-of-line (BEOL), indium oxide, nonvolatility, one-transistor-one-resistor (1T1R) FET.**

I. Introduction

TRADITIONAL von Neumann computer architecture, where data shuttle between different memory hierarchies is costly in terms of time and energy, is limiting explosive development of data-centric applications, such as artificial intelligence [1]–[7]. This memory bottleneck results in high latency, low bandwidth, and high energy consumption as memory and logic circuits keeping scaling down. Among several solutions, near-/in-memory computing, where certain computation tasks are performed in logic units physically near or directly in memory units, are promising [5]–[9]. On the other hand, resistive memory, featuring low static power consumption and nonvolatility, is attracting tremendous attention in the past decade as a potential alternative to mainstream memory in the market [10]–[13]. Among various types of resistive memory, one-transistor-one-resistor (1T1R) array, which is CMOS compatible, has been demonstrated to be eligible to perform near-/in-memory computing [4], [14]–[19]. However, to achieve high-performance and high-density near-/in-memory computing chips, monolithic 3-D integration using back-end-of-line (BEOL) compatible logic and memory devices is highly preferred. Therefore, BEOL compatible memory devices are highly demanded.

High drive current, low leakage, and low thermal budget (<400 °C) are required for BEOL transistors. Besides, scalability, high uniformity, reliability, and wafer-scale process are other basic requirements [20], [21]. One promising semiconductor for BEOL 3-D integration is amorphous oxide semiconductor [17], [22]–[29], primarily due to its high electrical performance as well as low thermal budget. Recently, atomic layer deposition (ALD) In_2O_3 has been demonstrated as an encouraging candidate for BEOL transistors, mainly attributed to several critical merits, including low-temperature budget (<225 °C), wafer-scale homogeneousness, atomically smooth surface, and high drive current over 2 A/mm [24], [25]. In addition, the ALD technique offers these oxide semiconductor devices with possibility to integrate with high aspect ratio structures, such as FinFET, gate-all-around (GAA) transistor, nanosheet transistor, and 3-D NAND, enabling 3-D structures with tremendous opportunities in logic-memory integration applications.

In this work, we report high-performance 1T1R FETs based on ALD grown In_2O_3. The gate and the insulator in resistive part are connected in series, similar to [30], to achieve two nonvolatile memory states. ALD deposited high-k dielectric hafnium oxide (HfO_2) and aluminum oxide (Al_2O_3) stack are chosen as the gate-stack and insulator in resistive part. High uniformity, nonvolatility, high $I_{ON}/I_{OFF} > 10^{10}$ at $V_{GS} = 0$ V, large memory window (MW) > 10 V, and deep sub-60-mV/dec subthreshold slope (SS) are achieved. In addition, devices show good immunity to short-channel effects (SCEs). Low thermal budget below 225 °C is realized. Channel thickness (T_{ch}) and channel length (L_{ch}) dependence of device properties are systematically investigated with optimal T_{ch} determined to be as thin as 1.2 nm balancing I_{ON}/I_{OFF}, MW, output performance, and device variation.

II. Experiments

Fig. 1(a) shows the schematic of an ALD In_2O_3 transistor. It has a buried gate structure with 40-nm W as gate metal, 10-nm HfO_2, and 1-nm Al_2O_3 as gate-stack,

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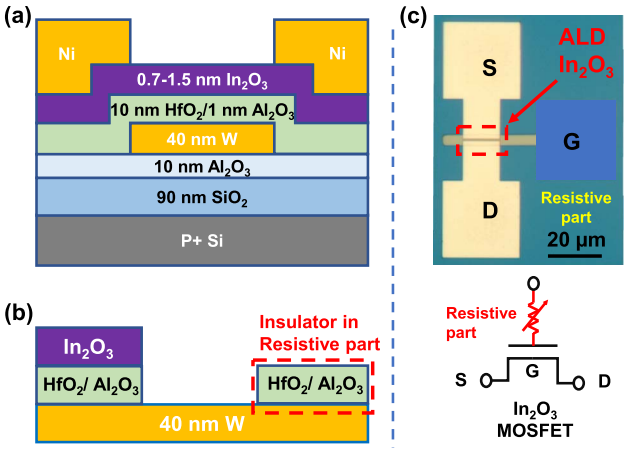

Fig. 1. (a) Schematic of an In_2O_3 transistor with 10-nm HfO_2/1-nm Al_2O_3 as gate dielectrics. (b) Gate-stack and the insulator in resistive part are connected in series. (c) Photograph image and circuit diagram of an ALD In_2O_3-based 1T1R FET. Insulator in resistive part is directly fabricated on top of gate pad, as marked by blue area.

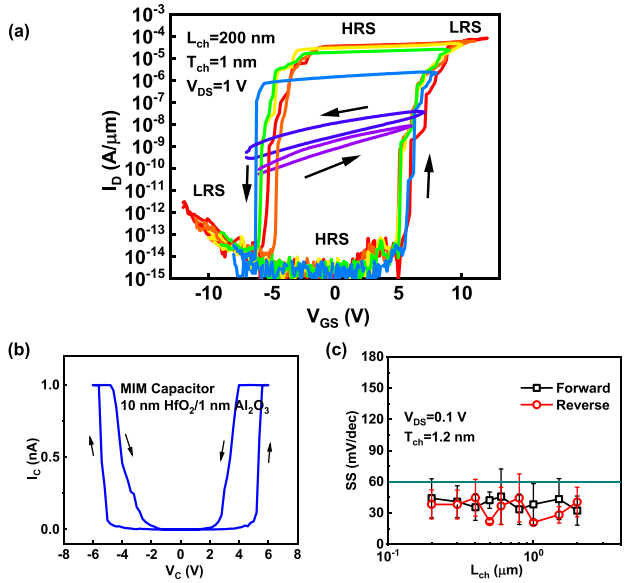

Fig. 2. (a) I_D–V_{GS} characteristics of an In_2O_3 1T1R FET with L_{ch} = 200 nm, T_{ch} = 1 nm, V_{DS} = 1 V, and different sweep ranges. Sweep directions of all curves are labeled by arrows. Resistive states in different regions are labeled. (b) I_C–V_C plots of an MIM capacitor of the same insulator as in resistive part in linear scale. I_C and V_C stand for measured current and applied voltage of the MIM capacitor, respectively. (c) SS versus L_{ch} of an In_2O_3-based 1T1R FET with T_{ch} of 1.2 nm. SS is extracted at V_{DS} = 0.1 V and highest transconductance point.

0.7-/1-/1.2-/1.5-nm In_2O_3 as channel semiconductor, and 40-nm Ni as source/drain (S/D) contacts. The insulator in resistive part and gate-stack are connected in series, forming a 1T1R FET, as shown in Fig. 1(b). The insulator in resistive part has a resistive switching property, as shown in Section III. Fig. 1(c) shows a photographic image and the electrical diagram of a 1T1R FET. The dark blue area in Fig. 1(c) highlights the resistive part. Metal electrode was not fabricated on top of the resistive part. Instead, the metal tip functions as the top metal electrode during measurements. In_2O_3 channel thickness can be precisely controlled by tuning ALD cycles and determined via transmission electron microscopy (TEM), atomic force microscopy (AFM), and ellipsometry, as reported in our previous work [24], [25].

The device fabrication process started with solvent cleaning of p+ Si substrate with 90-nm thermally grown SiO_2 on top. Then, 10-nm Al_2O_3 was deposited by ALD at 175 °C, using $Al(CH_3)_3$ (TMA) and H_2O as Al and O precursors, as W etching stop layer. Next, 40-nm W was sputtered by physical vapor deposition (PVD) followed by inductive coupled plasma (ICP) etching to pattern buried gate of MOSFET with sharp edges; 10-nm HfO_2 was then deposited by ALD at 200 °C using $[(CH_3)_2N]_4Hf$ (TDMAHf) and H_2O as Hf and O precursors, followed by 1-nm Al_2O_3 grown by ALD using the same recipe mentioned before. Gate dielectrics and the insulator in resistive part are deposited simultaneously. In_2O_3 thin films with thicknesses of 0.7/1/1.2/1.5 nm were then deposited by ALD at 225 °C using $(CH_3)_3$ In (TMIn) and H_2O as In and O precursors. Details about ALD In_2O_3 recipe can be found in our previous work [24], [25]. Concentrated hydrochloric acid was then applied as etchant to isolate In_2O_3 channel. In_2O_3 on top of insulator in resistive part was also removed; 40-nm Ni was then deposited by e-beam evaporation as S/D contacts, patterned by electron beam lithography. The fabrication process has a low thermal budget of 225 °C. Electrical characterization was done at room temperature with Keysight B1500A semiconductor device parameter analyzer.

III. Results and Discussion

Fig. 2(a) shows the I_D–V_{GS} characteristics of an $In_2O_3$1T1R FET with L_{ch} = 200 nm and T_{ch} = 1 nm at V_{DS} of 1 V and V_{GS} sweep range from ±6 to ±12 V. High ON-current, low OFF-current, and large counterclockwise hysteresis loop ($\Delta V_{th} \approx 10$ V) are observed when sweep range is wider than ±7 V. Below this threshold value, the device has weak electrostatic control with I_{ON}/I_{OFF} less than 10^2 and low ON-current below 10^{-7} A/μm. The cause of this phenomenon lies in resistive part's behavior under insufficient bias voltage. In this case, when the bias magnitude is below 7 V, the applied gate voltage is insufficient to trigger the soft breakdown of the insulator, rendering it staying in originally high-resistance state (HRS). As a result, the insulator always absorbs a considerably large portion of voltage drop. Thus, voltage drop across gate-stack is much smaller than the applied bias, and therefore, the electrostatic control of In_2O_3 channel is less effective.

Beyond this threshold value, the transfer properties, especially with large counterclockwise hysteresis loop [Fig. 2(a)], should be interpreted with the assistance of I–V characteristics of a metal–insulator–metal (MIM) capacitor (I_C–V_C) with the same insulator as resistive part in devices, as shown in Fig. 2(b). Arrows are presented in figure for clarity. The compliance current of 1 nA and sweep range of ±6 V are set to protect devices. Started with far negative bias, large voltage across insulator causes conductive filament formation, making the initial state of the insulator low-resistance state (LRS). As the magnitude of bias decreases, the conduction filament dissolves. Hence, LRS quickly decays to HRS. It is until the voltage across the insulator approaches the transition point in positive polarity that it switches from HRS to LRS

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again. Similar things happen in the negative polarity region. However, the resistive switching behavior in gate dielectric during the operation of a 1T1R FET is less obvious because of the asymmetric structures of two dielectric stacks, as shown in Fig. 2(a) with low I_{OFF}. The voltage drop on the gate dielectric is much smaller than that in the resistive part due to the voltage drop on the channel.

For transfer curves, different from the scenario with sweep range $< \pm 7$ V, started with far negative V_{GS}, the insulator in resistive part is in LRS. Therefore, voltage drops mostly in gate-stack since insulator in resistive part has minor voltage drop. Therefore, In_2O_3 channel can be fully depleted by field effect, resulting in a low OFF-current. Since the insulator quickly decays from LRS to HRS when continuing sweeping forward, highly resistive insulator blocks the increase of voltage drop on gate dielectric, rendering the In_2O_3 transistor locked in OFF-state, which should turn on approximately at $V_{th} = 0$ V at $T_{ch} = 1$ nm as reported previously [24], [25]. Similarly, the insulator in resistive part starts in LRS and then quickly switches into HRS as bias sweeps reversely. Therefore, the transistor is locked in ON-state that ON-currents decrease slowly. Resistive states in different regions are labeled in Fig. 2(a).

When bias goes far positive/negative in forward/reverse sweep, the insulator switches from HRS to LRS again, and the voltage drop in HRS has to apply to gate-stack since LRS cannot withhold such high voltage any more, resulting in steep switching with deep sub-60-mV/dec SS at all channel lengths. Note that in phenomenon wise, the I–V characteristic of 1T1R FET is very similar to that of ferroelectric FET in terms of counterclockwise hysteresis for n-channel and bi-directional steep slope less than 60 mV/dec. However, device physics is totally different. Ferroelectric FET is based on ferroelectric switch of ferroelectric dielectric, while 1T1R FET is based on resistive switch of Al_2O_3/HfO_2 gate-stack in this work. Fig. 2(c) shows extracted SS values at $V_{DS} = 0.1$ V of $T_{ch} = 1.2$ nm In_2O_3-based 1T1R FETs with L_{ch} ranging from 2 μm down to 200 nm. At least five devices at every channel length are measured and averaged with error bars shown in this figure. SSs in both forward and reverse sweep directions are presented. The average SS at all L_{ch} lies below 45 mV/dec. In addition, since this switching mechanism has minor dependence on the transistor itself, the SS versus L_{ch} characteristics demonstrates a good immunity to SCEs. Stepwise turning is observed in both sweep directions, as shown in Fig. 2(a). This is due to the instability in the beginning of resistive switching and relatively slow measurement speed unable to screen this instability.

From the analysis above, it is concluded that the 1T1R transistor that turns on and off mostly depends on where the insulator in resistive part undergoes HRS to LRS transition. Also, based on that the LRS-to-HRS switching mechanism makes the device being locked in the states as in LRS, these 1T1R FETs here naturally have two V_{th}'s, close to HRS-to-LRS transition points in two polarities, and counterclockwise hysteresis loops. Define MWs as MW $= \Delta V_{th} = V_{th,for} - V_{th,rev}$, where $V_{th,for}$ and $V_{th,rev}$ are V_{th}'s of forward and reserve sweeps, respectively, extracted at $V_{DS} = 0.1$ V by linear extrapolation.

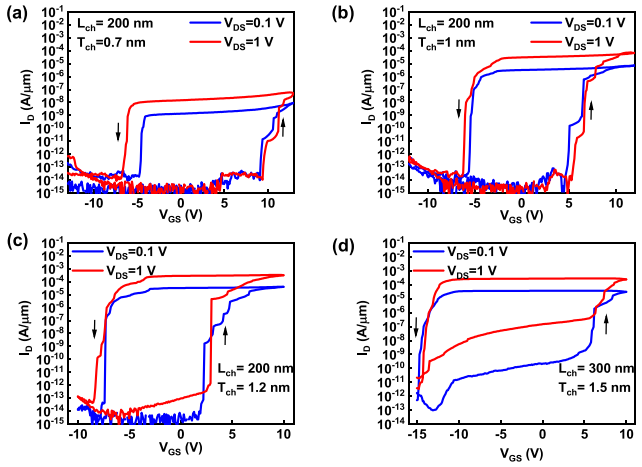

Fig. 3. (a)–(d) I_D–V_{GS} characteristics of In_2O_3 1T1R FETs with $T_{ch} = 0.7$ nm/1 nm/1.2 nm/1.5 nm. L_{ch} is 200 nm except for device with T_{ch} of 1.5 nm, whose L_{ch} is 300 nm.

A large MW larger than 10 V averagely is achieved in an In_2O_3 1T1R FET with T_{ch} of 1 nm. Nonvolatility is also realized in our transistors as a result of insulator's transition from LRS to HRS.

Channel thickness and channel length dependence of device properties are systematically investigated in the following parts. Fig. 3(a)–(d) shows the I_D–V_{GS} curves of 1T1R devices with $T_{ch} = 0.7/1/1.2/1.5$ nm. Sweep directions are marked by black arrows in figures. All present counterclockwise loops with large hysteresis. Fig. 4 summarizes the scaling metrics of In_2O_3-based 1T1R FETs with L_{ch} from 2 μm down to 200 nm and with various T_{ch}'s of 0.7/1/1.2/1.5 nm. Each data point represents the average of at least five devices with error bar presented. Fig. 4(a) and (b) shows the characteristics of maximum I_{DS} (I_{max}) and ON-current (I_{ON}) against L_{ch} at various T_{ch}. I_{max} and I_{ON} are extracted at $V_{DS} = 1$ V. I_{ON} is specified at $V_{GS} = 0$ V. The devices mostly follow a $1/L$ scaling trend. Fig. 4(c) shows the impact of T_{ch} and L_{ch} on OFF-current (I_{OFF}). The OFF-currents of 1T1R FETs with $T_{ch} = 0.7/1/1.2$ nm are suppressed down to 10^{-9} μA/μm ranging from all L_{ch}'s. The real I_{OFF} could be beyond the measurement limit since In_2O_3 has a bandgap larger than 3 eV [24]. Fig. 4(d) shows the calculated I_{ON}/I_{OFF} from experiments. Most of the devices show good uniformity with small error bars. Some large error bars of I_{OFF} and I_{ON}/I_{OFF} of transistors with $T_{ch} = 1.5$ nm are due to logarithm transformation of negative value when the standard deviation is greater than mean. The relatively large standard deviation of I_{OFF} of devices with $T_{ch} = 1.5$ nm results from the sensitivity to measurement range since V_{th} of these devices is close to minimum bias applied.

The 1T1R FET with $T_{ch} = 1.5$ nm presents a different curve shape shown in Fig. 3 with unsuppressed I_{OFF}'s, accompanied by obvious SCE that I_{OFF} increases with shrinking L_{ch}, as shown in Fig. 4(c). These phenomena are because of V_{th} of In_2O_3 transistor with T_{ch} of 1.5 nm that is close to the LRS-to-HRS transition point of the insulator in resistive part. As discussed before, the OFF-state of the 1T1R FET is due to a block of voltage growth caused by HRS. Therefore,

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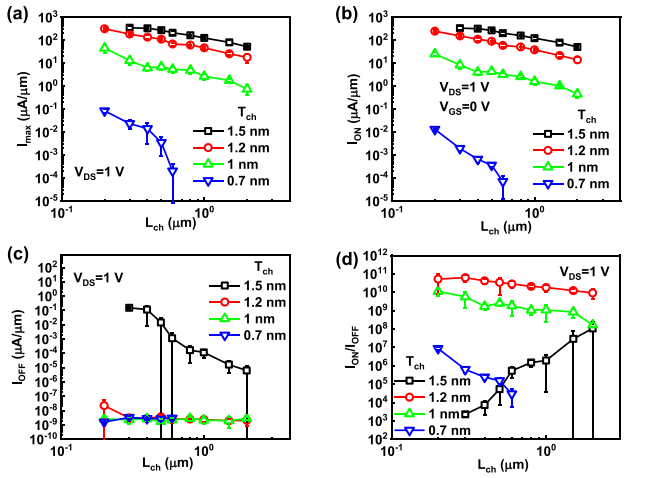

Fig. 4. (a) $I_{D,\,max}$, (b) I_{ON}, (c) I_{OFF}, and (d) I_{ON}/I_{OFF} scaling metrics of In_2O_3-based 1T1R FETs with L_{ch} from 2 μm to 200 nm and T_{ch} from 0.7 to 1.5 nm. All data are extracted at V_{DS} = 1 V unless otherwise specified. I_{ON} is specified at V_{GS} = 0 V. Each data point represents the average of at least five devices with error bars.

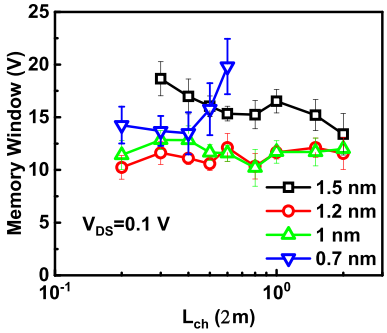

Fig. 5. MW versus L_{ch} of In_2O_3 1T1R FETs with L_{ch} from 2 μm to 200 nm and T_{ch} from 0.7 to 1.5 nm. MWs are calculated at V_{DS} of 0.1 V. Each data point represents the average of at least five devices with error bar presented.

this requires that the bias enabling LRS-to-HRS transition is smaller than V_{th} of the In_2O_3 transistor. Devices with T_{ch} of 0.7/1/1.2 nm are in such cases. However, In_2O_3 transistor with T_{ch} of 1.5 nm has much more negative V_{th}, which is near or smaller than the LRS-to-HRS transition point, resulting in devices not being locked in OFF-states or completely depleted, especially for short-channel devices where V_{th} may be more negative [24], [25]. Therefore, I_{OFF} is larger in short-channel devices, as shown in Fig. 4(c).

Although devices of all four T_{ch}'s show considerable MWs, device with T_{ch} = 0.7 nm/1.5 nm shows larger MWs than the middle two. MW's relationship against L_{ch} is shown in Fig. 5. In_2O_3 1T1R FETs with T_{ch} of 1 nm/1.2 nm show quite the same MWs about 10 V, which are almost independent on L_{ch}. In a short-channel case, a device with T_{ch} = 1.5 nm has the largest MW (larger than 15 V), which decreases to 10 V when L_{ch} increases. Comparing Fig. 3(d) with Fig. 3(b), it is obvious that the extra MW portion mainly comes from a more negative V_{th} in the reserve sweep. This is likely a result of that V_{th} is even more negative than HRS to LRS transition point. The positive V_{th} of the devices with T_{ch} of 0.7 nm is determined by V_{th} of the transistors, rather than the resistive

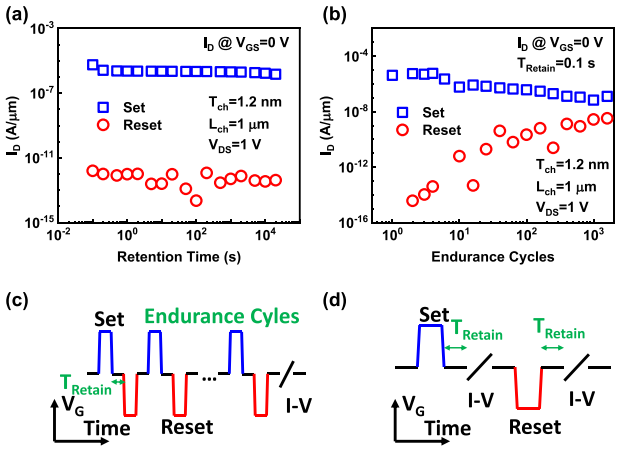

Fig. 6. (a) Retention and (b) endurance performance of In_2O_3-based 1T1R FETs with T_{ch} of 1.2 nm and L_{ch} of 1 μm at V_{DS} of 0.1 V. I_D at V_{GS} of 0 V for both set and reset are shown. (c) and (d) Test sequences of retention and endurance characteristics, respectively.

switching point due to that the former is greater than the latter. As L_{ch} increases, V_{th} of transistors and, thus, positive V_{th} of 1T1R FETs shift positively, resulting in a larger MW. T_{ch} of 1 nm/1.2 nm is preferred to have a stable MW for 1T1R FETs.

The reliability is critical for In_2O_3-based 1T1R FETs toward nonvolatile memory application, as shown in Fig. 6. Fig. 6(a) and (b) shows the retention and endurance performance of devices for both set and reset with T_{ch} of 1.2 nm and L_{ch} of 1 μm at V_{DS} of 0.1 V, respectively. 1T1R FETs show negligible change of I_D at zero gate bias after both set and reset within 20 000 s and thus keep an I_{ON}/I_{OFF} ratio over 10^6, demonstrating ideal retention characteristics toward nonvolatile memory application. For endurance performance, I_D at zero gate bias for reset increases about six orders within 1000 cycles, whereas I_D for set undergoes minor change. Hence, I_{ON}/I_{OFF} shrinks within 1000 endurance cycles. This is likely a result of the degrading quality of resistive part under multiple switches.

By balancing I_{ON}/I_{OFF}, MW, and device variation combined, In_2O_3 1T1R FET with T_{ch} of 1.2 nm is optimal for application, which shows the highest ON/OFF ratio larger than 10^{10} at V_{GS} = 0 V, high ON-current, immunity to SCEs, and a stable MW around 10 V. The device performance still has rooms to boost by further scaling, optimizing dielectrics thickness and process optimization. The device uniformity can be improved by further optimizing ALD processes. The operation voltage can also be scaled down by only selectively scaling down the dielectric thickness at the resistive part to lower the switching voltage while maintaining the high-quality gate dielectric on the transistor. This work is just the first report on BEOL compatible 1T1R FETs for nonvolatile memory applications using ALD In_2O_3 as transistor channels. The reliability performance of In_2O_3-based 1T1R FETs still has room to improve by optimizing interface quality and endurance properties of resistive part under multiple switches. A complete study and optimization are still demanded to qualify In_2O_3-based 1T1R FETs for BEOL compatible logic/memory integration toward near-/in-memory computing.

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IV. Conclusion

In summary, scaled BEOL-compatible ALD In_2O_3-based 1T1R FETs with channel thickness down to 0.7 nm and channel length down to 200 nm are demonstrated. High uniformity, high I_{ON}/I_{OFF} larger than 10^{10} at $V_{GS} = 0$ V, large MW exceeding 10 V, and deep sub-60-mV/dec SS are achieved. Switching between two resistive states offers two different threshold voltages with nonvolatility. Dependence of device characteristics on channel length and thickness is thoroughly analyzed with optimal channel thickness determined to be 1.2-nm balancing multiple factors. ALD processes bring devices with wafer-scale uniformity and atomic-level control of dielectrics and semiconductor thickness. Low thermal budget below 225 °C, combined with high-performance memory characteristics, demonstrates the ALD In_2O_3-based 1T1R FETs a promising candidate for monolithic BEOL logic/memory to realize near-/in-memory computing.

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