Enhancement-Mode Atomic-Layer-Deposited In_2O_3 Transistors With Maximum Drain Current of 2.2 A/mm at Drain Voltage of 0.7 V by Low-Temperature Annealing and Stability in Hydrogen Environment

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***Abstract*—In this article, we demonstrate atomic-layer-deposited (ALD) indium oxide (In_2O_3) transistors with a record high drain current of 2.2 A/mm at V_{DS} of 0.7 V among oxide semiconductor transistors with the enhancement-mode operation. The impact of back-end-of-line (BEOL) compatible low-temperature annealing is systematically studied on these highly scaled In_2O_3 transistors with channel length (L_{ch}) down to 40 nm, channel thickness (T_{ch}) down to 1.2 nm, and equivalent oxide thickness (EOTs) of 2.1 nm, at annealing temperatures from 250 °C to 350 °C in N_2, O_2, and forming gas (FG, 96% N_2/4% H_2) environments. Annealing in all different environments is found to significantly improve the performance of ALD In_2O_3 transistors, resulting in enhancement-mode operation, high mobility, reduced bulk and interface trap density (D_{it} as low as 6.3×10^{11} $cm^{-2} \cdot eV^{-1}$), and nearly ideal subthreshold slope (SS) of 63.8 mV/dec. Remarkably, the ALD In_2O_3 devices are found to be stable in hydrogen environment, being less affected by the well-known hydrogen doping issue in indium–gallium–tin-oxide (IGZO). Therefore, low-temperature ALD In_2O_3 transistors are highly compatible with the hydrogen-rich environment in BEOL fabrication processes.**

***Index Terms*—Annealing, atomic layer deposition (ALD), back-end-of-line (BEOL) compatible, hydrogen, indium oxide, oxide semiconductor, thin-film transistor.**

I. Introduction

OXIDE semiconductors are widely employed in thin-film transistors [1], [2] and are promising channel materials for complementary metal–oxide–semiconductor (CMOS) back-end-of-line (BEOL) compatible transistors for monolithic (3-D) integration. Indium oxide (In_2O_3) [3], [4] or doped-In_2O_3 [5]–[10] are being investigated due to their low thermal budget growth and fabrication, high mobility, atomically smooth surface, and wafer-scale homogenous films. The capability of atomic layer deposition (ALD) to deposit atomically thin and conformal In_2O_3 films on 3-D structures enables tremendous new opportunities toward 3-D device integration [3], [4], [11]–[14]. High-performance scaled In_2O_3 transistors by ALD have been demonstrated with maximum drain current ($I_{D,max}$) exceeding 2.0 A/mm at depletion-mode operation [4]. Enhancement-mode operation with threshold voltage (V_T) above zero was also achieved by decreasing channel thickness (T_{ch}) down to 0.7 and 1 nm by the accurate thickness control of ALD, but also causes the reduction of channel mobility and $I_{D,max}$ down to 1.0 A/mm [3], [4]. Such phenomenon was understood by the impact of quantum confinement on the trap neutral level (TNL) alignment, confirmed by both experiments and *ab initio* density functional theory (DFT) simulation [3].

Meanwhile, stability in hydrogen-rich environment is required and crucial for BEOL compatible process because H_2 is the byproduct during BEOL fabrication [15]. Post-deposition hydrogen doping to amorphous indium–gallium–tin-oxide (IGZO), such as N_2/H_2 annealing and H plasma treatment, was well understood to always increase free electron density up to $\sim 10^{20}$ /cm^3 [16]–[18]. Hydrogen was understood as shallow donor and to form an OH group [17]. Therefore, whether In_2O_3 or doped In_2O_3 can be stable in the CMOS BEOL process becomes a serious concern.

In this article, the impact of post-deposition annealing in various environments, such as O_2, N_2, and forming gas (FG, 96% N_2/4% H_2), at various BEOL compatible low temperatures from 250 °C to 350 °C on ALD In_2O_3 transistors are systematically studied. Annealing in all different environments is found to shift the V_T positively and lead to the enhancement-mode operation, where the physical origin is speculated as the annihilation of oxygen vacancies by excessive oxygen in the as-deposited films. Remarkably,

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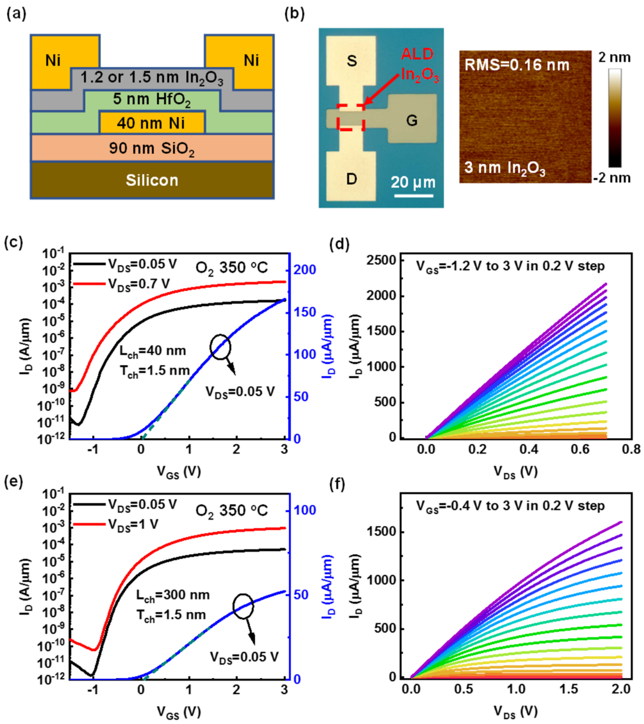

Fig. 1. (a) Schematic and (b) photo image of an In_2O_3 transistor and AFM measurement of the surface roughness on a 3-nm as-deposited ALD In_2O_3 film. (c) I_D–V_{GS} and (d) I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm, T_{ch} of 1.5 nm, and annealed at 350 °C in O_2. (e) I_D–V_{GS} and (f) I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 300 nm, T_{ch} of 1.5 nm, and annealed at 350 °C in O_2.

the ALD In_2O_3 devices are found to be stable in hydrogen environment, being less affected by the well-known hydrogen doping issue in IGZO [16]–[18]. Therefore, ALD In_2O_3 could be highly compatible with hydrogen-rich environment in CMOS BEOL fabrication processes.

High-performance ALD enhancement-mode In_2O_3 transistors are also demonstrated by the optimized post-deposition annealing. Record high drain current of 2.2 A/mm at V_{DS} of 0.7 V with V_T of 0.02 V is achieved on this enhancement-mode In_2O_3 transistor with channel length (L_{ch}) of 40 nm, channel thickness (T_{ch}) of 1.5 nm, and equivalent oxide thickness (EOTs) of 2.1 nm, with 350 °C annealing in O_2. A detailed benchmarking information of the maximum drain currents among oxide semiconductors-based transistors can be found in [5]. A high field-effect mobility (μ_{FE}) of 91.0 cm^2/V·s is achieved. High drain current over 1.0 A/mm is also achieved on enhancement-mode In_2O_3 transistors with L_{ch} of 40 nm, T_{ch} of 1.2 nm, and EOT of 2.1 nm, with low-temperature annealing in O_2, N_2, and FG. Subthreshold slope (SS) as low as 63.8 mV/dec is obtained on In_2O_3 transistors with FG annealing, corresponding to an interface trap density (D_{it}) of 6.3×10^{11} $cm^{-2}{\cdot}eV^{-1}$, indicating FG annealing can effectively passivate the interface trap states at HfO_2/In_2O_3 oxide/oxide interface.

II. Experiments

Fig. 1(a) illustrates the schematic of an In_2O_3 transistor, employing the same structure as previously reported in [4]. The gate-stack includes 40-nm Ni as gate metal, 5-nm HfO_2 as gate dielectric, 1.2 and 1.5 nm In_2O_3 as semiconducting channels, and 80 nm Ni as source/drain electrodes. Fig. 1(b) presents the photo image of a typical fabricated device.

The device fabrication process is similar to [4]. The device fabrication starts with standard cleaning of p+ Si substrate with 90 nm thermally grown SiO_2. 90-nm SiO_2 is used for device isolation. A bi-layer photoresist lithography process (Polymethylglutarimide (PMGI) + AZ1518) was then applied for the sharp lift-off of 40-nm Ni gate metal by e-beam evaporation. Then, 5-nm HfO_2 was deposited by ALD at 200 °C, using $[(CH_3)_2N]_4Hf$ (TDMAHf) and H_2O as Hf and O precursors. 1.2 and 1.5-nm thick In_2O_3 films were then deposited by ALD at 225 °C, using $(CH_3)_3In$ (TMIn) and H_2O as In and O precursors. N_2 is used as the carrier gas. ALD In_2O_3 film has a low surface roughness, as shown in Fig. 1(b), where 3-nm as-deposited In_2O_3 on Si substrate has a surface roughness of 0.16 nm, measured by atomic force microscopy (AFM), indicating ALD In_2O_3 film is atomically smooth. As-deposited ALD In_2O_3 is amorphous [4], further material studies are needed to determine whether annealing at high temperatures changes the phase of ALD In_2O_3. The ALD deposition process may introduce both excessive hydrogen and oxygen into the In_2O_3 film from the water precursor. The ALD temperature at 225 °C may be insufficient to passivate all oxygen deficiencies. Channel isolation was done by wet etching of In_2O_3 using concentrated hydrochloric acid. Hydrochloric acid is another possible hydrogen source. 80-nm Ni was then deposited by e-beam evaporation as S/D contacts, patterned by electron beam lithography, with a minimum L_{ch} of 40 nm. The fabricated devices were annealed in O_2, N_2, or FG for 30 s at different temperatures from 250 °C to 350 °C. Note that the fabrication process may introduce defects into the In_2O_3 channel since it is just nanometer thin, causing a L_{ch} dependent carrier density and V_T, which can be completely removed by annealing. This will be discussed in detail in Section III.

III. Results and Discussion

Fig. 1(c) and (d) presents the representative I_D–V_{GS} and I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm and T_{ch} of 1.5 nm with 350 °C annealing in O_2. Maximum I_D of 2.2 A/mm is achieved at a low V_{DS} of 0.7 V with V_T of 0.02 V. Here, enhancement-mode is $V_T > 0$ V by definition. Note that although $V_T > 0$ V is achieved, a relatively large current at $V_{GS} = 0$ V is still existing, indicating that larger V_T is still needed to achieve low off-current at $V_{GS} = 0$ V. A low ON-resistance (R_{on}) of 0.32 Ω·mm is obtained, suggesting a very low contact resistance (R_C). Fig. 1(e) and (f) presents the I_D–V_{GS} and I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 300 nm and T_{ch} of 1.5 nm, showing well-behaved I_D saturation at high V_{DS} greater than V_{GS}–V_T.

Fig. 2 summarizes the scaling metrics of In_2O_3 transistors with L_{ch} from 0.8 μm down to 40 nm and with T_{ch} of 1.5 nm. The devices with and without O_2 annealing at 350 °C are compared. Each data point represents the average of at least 5 devices. The small error bar in these plots demonstrates

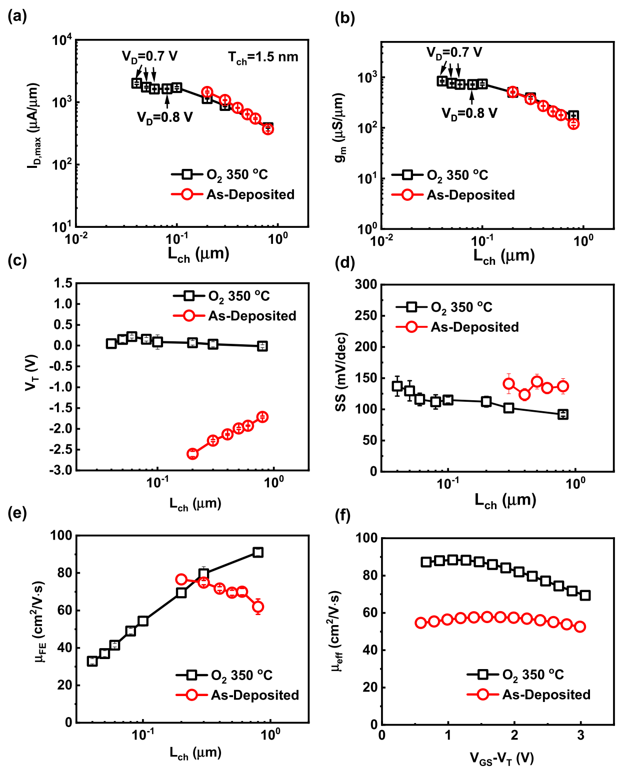

Fig. 2. (a) $I_{D,max}$, (b) g_m, (c) V_T, (d) SS, and (e) μ_{FE} scaling metrics of In_2O_3 transistors with L_{ch} from 0.8 μm to 40 nm and T_{ch} of 1.5 nm. Each data point represents the average of at least 5 devices. The data are from devices with and without 350 °C annealing in O_2. (f) Effective mobility versus V_{GS}–V_T extracted from a device with L_{ch} of 0.8 μm and T_{ch} of 1.5 nm with 350 °C O_2 annealing and from a device with L_{ch} of 1 μm and T_{ch} of 1.5 nm with as-deposited film. $I_{D,max}$ and g_m are extracted at V_{DS} = 1 V unless otherwise specified.

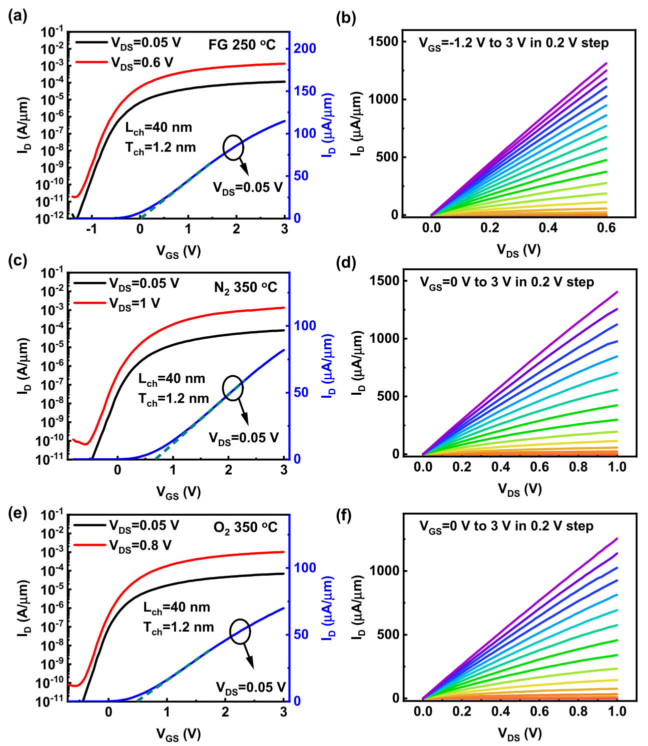

Fig. 3. (a) I_D–V_{GS} and (b) I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm and T_{ch} of 1.2 nm, annealed at 250 °C in FG. (c) I_D–V_{GS} and (d) I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm and T_{ch} of 1.2 nm, annealed at 350 °C in N_2. (e) I_D–V_{GS} and (f) I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm and T_{ch} of 1.2 nm, annealed at 350 °C in O_2.

that the ALD-based In_2O_3 transistors are highly uniform. Fig. 2(a) and (b) shows the $I_{D,max}$ and transconductance (g_m) versus L_{ch} characteristics. $I_{D,max}$ and g_m are extracted at V_{DS} = 1 V unless otherwise specified. A high average $I_{D,max} > 2.0$ A/mm at V_{DS} of 0.7 V is achieved. Low drain voltages are used at shorter channels to avoid the impact of self-heating effect. Fig. 2(c) studies the impact of O_2 annealing on V_T, showing a large positive V_T shift by 350 °C annealing in O_2. Note that the as-deposited In_2O_3 transistors have a clearly L_{ch} dependent V_T even in long channel devices while V_T has negligible L_{ch} dependence after O_2 annealing, suggests such V_T dependence is from the defects introduced during device fabrication and these defects are completely removed by O_2 annealing, such phenomenon is further confirmed by detailed N_2/O_2/FG annealing completely studies in Figs. 4–6. Fig. 2(d) presents the SS versus L_{ch} characteristics at V_{DS} of 0.05 V. Minimum SS of 91.7 mV/dec is achieved. Fig. 2(e) shows the scaling metrics on μ_{FE}. μ_{FE} is extracted from extrinsic maximum g_m at low V_{DS} of 0.05 V. High μ_{FE} of 91.0 cm^2/V·s is achieved at ultrathin T_{ch} of 1.5 nm, which is rather high among amorphous oxide semiconductors, being benefitted from the atomically smooth surface by ALD, which is also consistent with extracted effective mobility (μ_{eff}) as shown in Fig. 2(f). Note that the extracted extrinsic mobilities are still under-estimated without considering the impact from contact resistance R_C, which is generally low at back-gate In_2O_3 transistors studied here. The intrinsic mobility of annealed ALD In_2O_3 can be even higher. The devices exhibit excellent immunity to short channel effects down to 40 nm because of the ultrathin In_2O_3 channel and scaled EOT.

To understand the physics and chemistry of annealing effects on ALD In_2O_3 transistors, a systematic annealing study was conducted at various temperatures from 250 °C to 350 °C in N_2, O_2, and FG environments. Such annealing study was done on In_2O_3 with a thinner channel with T_{ch} of 1.2 nm, because In_2O_3 transistors with T_{ch} of 1.2 nm have a V_T near zero, so that both carrier density enhancement and reduction can be captured.

Fig. 3 shows representative $I - V$ results of short channel ALD In_2O_3 transistors with T_{ch} of 1.2 nm after annealing. Fig. 3(a) and (b) shows the I_D–V_{GS} and I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm and T_{ch} of 1.2 nm, with 250 °C annealing in FG. Maximum I_D of 1.3 A/mm is achieved at V_{DS} of 0.6 V with V_T of 0.01 V. Fig. 3(c) and (d) shows the I_D–V_{GS} and I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm and T_{ch} of 1.2 nm, with 350 °C annealing in N_2. Maximum I_D of 1.4 A/mm is achieved at V_{DS} of 1 V with V_T of 0.7 V. Fig. 3(e) and (f) shows the I_D–V_{GS} and I_D–V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm and T_{ch} of 1.2 nm, with 350 °C annealing in O_2. Maximum I_D of 1.3 A/mm is achieved at V_{DS} of 1 V with V_T of 0.5 V.

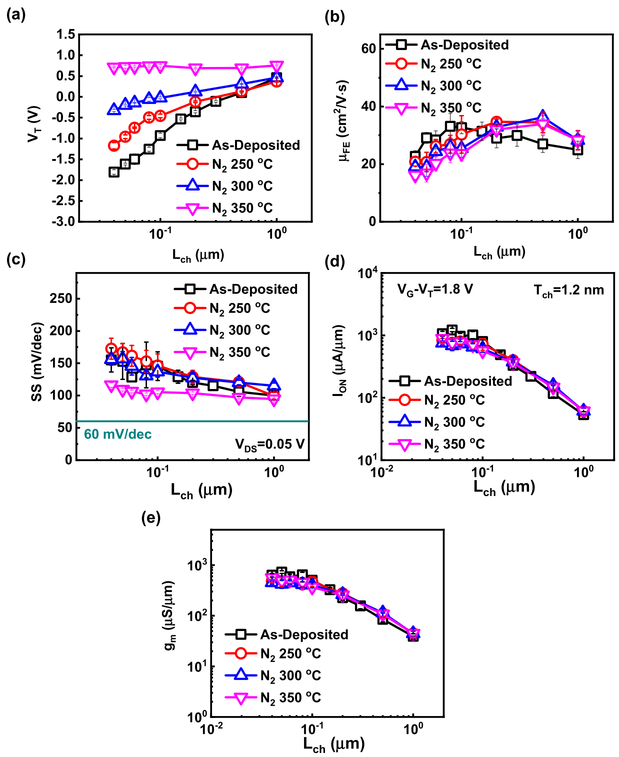

Fig. 4. (a) V_T, (b) μ_{FE}, (c) SS, (d) I_{on}, and (e) g_m scaling metrics of In_2O_3 transistors with L_{ch} from 1 μm to 40 nm and T_{ch} of 1.2 nm. The devices were annealing from 250 °C to 350 °C in N_2 and compared to devices without annealing. I_{on} and g_m are extracted at $V_{DS} = 1$ V unless otherwise specified. I_{on} and g_m at L_{ch} of 80, 60, 50, and 40 nm annealed at 250 °C and 300 °C are extracted at V_{DS} of 0.8, 0.7, 0.7, 0.6 V. Lower voltage at shorter channel devices are used to avoid the impact of self-heating on devices. Each data point represents the average of at least 5 devices.

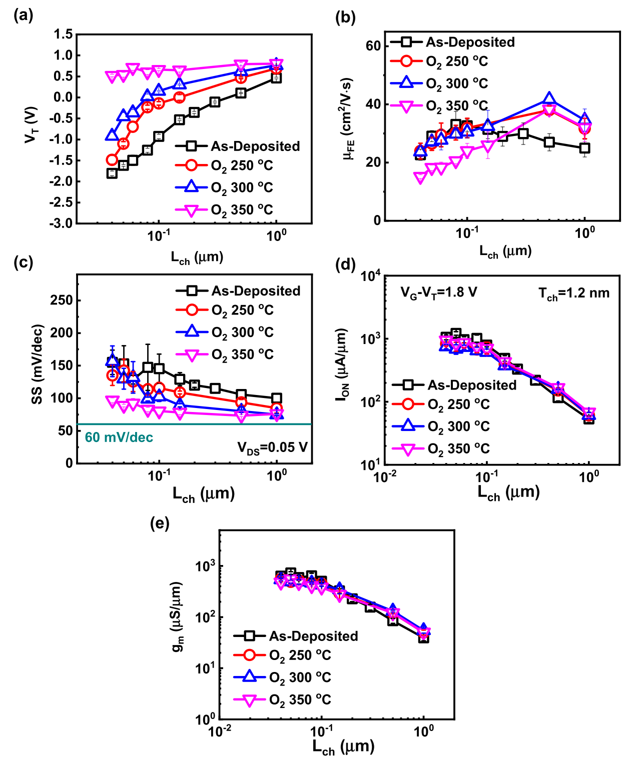

Fig. 5. (a) V_T, (b) μ_{FE}, (c) SS, (d) I_{on}, and (e) g_m scaling metrics of In_2O_3 transistors with L_{ch} from 1 μm to 40 nm and T_{ch} of 1.2 nm. The devices were annealing from 250 °C to 350 °C in O_2 and compared to devices without annealing. I_{on} and g_m are extracted at $V_{DS} = 1$ V unless otherwise specified. I_{on} and g_m at L_{ch} of 100, 80, 60, 50 and 40 nm annealed at 250 °C and 300 °C are extracted at V_{DS} of 0.9, 0.8, 0.7, 0.6, 0.6 V. I_{on} and g_m at L_{ch} of 40 nm annealed at 350 °C are extracted at V_{DS} of 0.8 V. Lower voltage at shorter channel devices are used to avoid the impact of self-heating on devices. Each data point represents the average of at least 5 devices.

Fig. 4 summarizes the scaling metrics of In_2O_3 transistors with L_{ch} from 1 μm down to 40 nm and with T_{ch} of 1.2 nm, annealed from 250 °C to 350 °C in N_2 and compared to devices without annealing. Fig. 4(a) studies the impact of N_2 annealing at different temperatures on V_T, showing a large positive V_T shift by annealing in N_2. Note that the as-deposited In_2O_3 transistors have a clearly L_{ch} dependent V_T even in long channel devices, which is not predicted by semiconductor device physics. V_T has negligible L_{ch} dependence after N_2 annealing at 350 °C, suggesting such V_T dependence is from the defects introduced in device fabrication and these defects are completely removed, as also discussed previously. Fig. 4(b) illustrates the impact of N_2 annealing on extrinsic μ_{FE} extracted from the extrinsic g_m without considering the contact resistance. μ_{FE} increases after annealing at the long channel but μ_{FE} decreases after annealing at short channel, indicating the mobility is enhanced by N_2 annealing but R_C increases due to the reduction of carrier density. Extracted μ_{FE} of In_2O_3 with N_2 annealing at 350 °C will decrease at the short-channel devices, because the V_T shift at short channel by annealing, leading to very different contact resistance due to the different carrier concentration. The extracted μ_{FE} should only be regarded as the lower limit of the intrinsic mobility of the In_2O_3 film. Fig. 4(c) presents the SS versus L_{ch} characteristics at V_{DS} of 0.05 V at different N_2 annealing temperatures. Minimum SS of 97.0 mV/dec is achieved. SS is found to decease with increasing N_2 annealing temperature, suggesting D_{it} can be reduced effectively by N_2 annealing. Fig. 4(d) and (f) shows the ON-current (I_{on}) at V_{GS}–V_T = 1.8 V and transconductance (g_m) versus L_{ch} characteristics. I_{on} and g_m are extracted at V_{DS} = 1 V unless otherwise specified. Lower voltage at shorter channel devices are used to avoid the impact of self-heating on devices since self-heating may induce a similar effect as annealing, as specified in Fig. 4 caption.

Fig. 5 summarizes the scaling metrics of In_2O_3 transistors with L_{ch} from 1 μm down to 40 nm and with T_{ch} of 1.2 nm, annealed from 250 °C to 350 °C in O_2 and compared to devices without annealing. Minimum SS of 73.0 mV/dec is achieved after 350 °C annealing in O_2, suggesting O_2 annealing can more effectively reduce D_{it} than N_2 annealing. Except for the significantly reduced SS, other device performance criteria from devices by O_2 annealing and N_2 annealing are pretty much similar and follow the same trend.

Fig. 6 summarizes the scaling metrics of In_2O_3 transistors with L_{ch} from 1 μm down to 40 nm and with T_{ch} of 1.2 nm, annealed from 250 °C to 350 °C in FG and compared to devices without annealing. Fig. 6(a) shows the I_D–V_{GS} characteristics of an In_2O_3 transistor with L_{ch} of 400 nm and T_{ch}

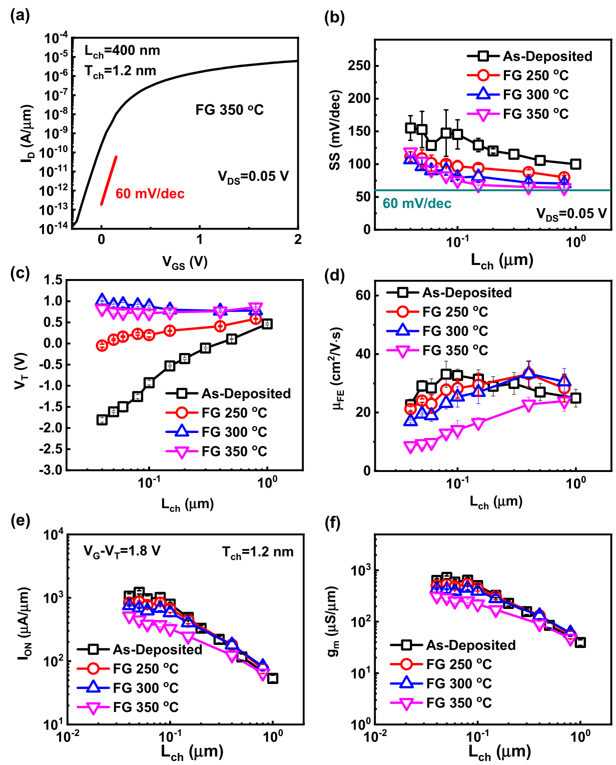

Fig. 6. (a) I_D–V_{GS} characteristics of an In_2O_3 transistor with L_{ch} of 400 nm and T_{ch} of 1.2 nm at V_{DS} of 0.05 V, annealed at 350 °C in FG. (b) SS, (c) V_T, (d) μ_{FE}, (e) I_{on}, and (f) g_m scaling metrics of In_2O_3 transistors with L_{ch} from 1 μm to 40 nm and T_{ch} of 1.2 nm. The devices were annealed from 250 °C to 350 °C in FG and compared to devices without annealing. I_{on} and g_m are extracted at V_{DS} = 1 V unless otherwise specified. I_{on} and g_m at L_{ch} of 60, 50 and 40 nm annealed at 300 °C are extracted at V_{DS} of 0.8, 0.7, 0.7 V. I_{on} and g_m at L_{ch} of 60, 50, and 40 nm annealed at 250 °C are extracted at V_{DS} of 0.8, 0.7, 0.6 V. Lower voltage at shorter channel devices are used to avoid the impact of self-heating on devices. Each data point represents the average of at least 5 devices.

of 1.2 nm at V_{DS} of 0.05 V, with 350 °C annealing in FG, exhibiting a *nearly ideal* SS. Fig. 6(b) presents the SS versus L_{ch} characteristics at V_{DS} of 0.05 V at different FG annealing temperatures. Minimum SS of 63.8 mV/dec (average value) is achieved by FG annealing at 350 °C, corresponding to a low D_{it} of 6.3 × 10^{11} $cm^{-2}\cdot eV^{-1}$, extracted from subthreshold method. It suggests that hydrogen is the most effective way to passivate the interface traps in this HfO_2/In_2O_3 material system. Other device performance criteria from devices by FG annealing follow the similar trend to O_2 and N_2 annealing, suggesting the V_T shift by annealing is the result of annealing temperature instead of the annealing environments.

Oxygen vacancies are known to act as shallow donors and determine the carrier density in doped-In_2O_3 [19]. It is widely reported that the oxygen pressure during film sputter deposition and thermal annealing have significant impact on the electrical conductivity of doped-In_2O_3 films such as IGZO and indium–tin-oxide (ITO) [1], [5], [19]–[21]. It was understood that oxygen vacancies form both a deep localized state and a shallow donor state depending on local atomic configurations by first principle simulation [17], [22]. Therefore, because of the similarity between ALD In_2O_3 and doped-In_2O_3, it is assumed that oxygen vacancies are also shallow donors in ALD In_2O_3 films, such assumption may need further verification by materials analysis and simulation. Based on this assumption, it is speculated that the V_T shift of ALD In_2O_3 transistors by annealing is likely to be the result of oxidization of oxygen deficiencies or vacancies by excessive oxygen inside the In_2O_3 film not from the environment becauseFG, N_2 and O_2 annealing give similar results. The excessive oxygen is likely to come from ALD or other processes during device fabrication. The ALD temperature is not high enough for these excessive oxygens to oxidize the oxygen vacancies, as more than 300 °C is needed to annihilate these defects.

Annealing at 350 °C in all environments causes the slight deteriorate of μ_{FE}, most likely due to the degradation of Ni/In_2O_3 contact resistance because of the reduction of carrier density, which may be further improved by introducing conducting oxide contact such as ITO [5], [6].

As can be clearly seen from Figs. 4–6, devices after 350 °C annealing in O_2, N_2, and FG show similar V_T, suggesting the ALD In_2O_3 is less affected by the widely exhibiting hydrogen doping issue in IGZO [16], [18], [23]–[25]. This result also indicates that the role of hydrogen in ALD In_2O_3 may be different from the hydrogen in sputter IGZO films. This is a strong support that ALD In_2O_3 can be highly compatible with hydrogen-rich environment in CMOS BEOL processes.

The detailed surface chemistry experiments and the complete understanding of the hydrogen chemistry in ALD In_2O_3 are out of the scope of this article. We may give the following two hypotheses to explain the experimental phenomenon. First, all the oxygen bonds in bulk ALD In_2O_3 film may be already passivated by the hydrogen from water precursors, in a hydrogen saturation state. Thus, new hydrogen from the environment has little impact on the doping of ALD In_2O_3 film. Second, hydrogen may not behave like shallow dopant in ALD In_2O_3 due to the possible different electronic structures. As the first work on high-performance enhancement-mode In_2O_3 transistors with different annealing conditions, we wish it can inspire more fundamental studies on surface chemistry and physics research on this novel material system.

The reliability performance of devices is critical for the application of the ALD In_2O_3 technology. A complete understanding and optimization on reliability performance is still required to qualify the ALD In_2O_3 technology for CMOS BEOL transistors for monolithic 3-D integration.

IV. Conclusion

In summary, the impact of post-deposition annealing in various environments, such as O_2, N_2, and FG (96% N_2/4% H_2), at various BEOL compatible low temperatures on ALD In_2O_3 transistors is systematically studied. The optimized annealing conditions are found to enhance the performance of In_2O_3 transistors significantly. Enhancement-mode In_2O_3 transistors with record high drain current of 2.2 A/mm at V_{DS} of 0.7 V with V_T of 0.02 V are demonstrated. SS as low as 63.8 mV/dec is achieved, corresponding to a low D_{it} of 6.3 × 10^{11} $cm^{-2}\cdot eV^{-1}$. The physical origin of the positive threshold voltage shift by annealing is speculated as the passivation of oxygen vacancies by excessive oxygen in as-deposited films. Remarkably, the ALD In_2O_3 devices are found to be stable in hydrogen environment, being less affected by the well-known hydrogen doping issue in IGZO. Therefore, ALD In_2O_3 transistors and its high compatibility with hydrogen-rich CMOS BEOL process suggest ALD In_2O_3 is the promising channel material for BEOL compatible transistors toward monolithic 3-D integration.

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