# Performance Potential of Ge CMOS Technology From a Material-Device-Circuit Perspective

SangHoon Shin, *Student Member, IEEE*, Hai Jiang, *Student Member, IEEE*, Woojin Ahn, *Student Member, IEEE*, Heng Wu, *Member, IEEE*, Wonil Chung, *Student Member, IEEE*, Peide D. Ye, *Fellow, IEEE*, and Muhammad Ashraful Alam, *Fellow, IEEE*

***Abstract*— Recently demonstrated CMOS circuits based on Ge nanowires (Ge-FET) promise sustained technology scaling because higher mobility Ge guarantees target $I_{ON}$ at a lower $V_{DD}$. Unfortunately, this promise is counterbalanced by the fact that Ge is a poor thermal conductor, thus, the thermal confinement of the surround-gate topology may exacerbate self-heating (SHE) and erode the intrinsic performance gain associated with the high channel mobility. In this paper, we use: 1) electrical and optical methods to, respectively, characterize channel and surface SHE of Ge-FET with various channel lengths ($L_{ch}$), widths ($W_{ch}$), and the number of the nanowires (NWs) (#NW); 2) interpret the results obtained by the 3-D thermal modeling, and compare theoretically the SHE in Ge-FET configured in various topologies, such as bulk FinFET, silicon-on-insulator FinFET, and gate-all-around NW-FET; and 3) embed the results in an electrothermal SPICE simulator to compare the performance of ring oscillators based on Ge-FET and Si-FET. Our results show that the existing Ge-FET (with an airgap) is thermally suboptimal, but once optimized, SHE in Ge-FET would be comparable to that of Si-FET. The results encourage sustained development of Ge-FETs.**

***Index Terms*— Digital circuit, floating body transistors, Ge CMOS, nanowire, pulsed *I–V*, self-heating (SHE), thermoreflectance (TR).**

## I. Introduction

ELECTROSTATIC confinement of silicon-on-insulator (SOI)-FET and multigate FET is essential to control short channel effects in sub-10-nm technologies. Since $I_{ON}$ reduces with transistor cross section, it can be restored either by using multiple fins and/or by using higher mobility channels, such as Ge, InGaAs, or carbon nanotube [7]–[13]. Among the channel materials, only Ge has sufficiently high electron and hole mobilities to allow the fabrication of all-Ge CMOS circuit. The technology issues of developing appropriate gate-stack, high-$\kappa$ dielectric integration and thin body issues with Ge p-MOSFET (PFET) have been resolved [14], [15]. Although inversion-mode n-MOSFET (NFET) is still difficult due to Fermi-level pinning at the valence band edge and large source and drain (S/D) contact resistance, the recent demonstration of Ge CMOS with accumulated NFET and inverted PFET, with recessed S/D contacts for reducing Schottky barrier height, has been a welcome and anticipated technical breakthrough [16]–[20]. The technology integrates multiple gate and thin channel body to improve gate controllability with desirable $I_{ON}$ and $I_{OFF}$, with excellent subthreshold slopes. The core technology has advanced sufficiently so that we can now address a set of secondary concerns, such as the performance and reliability implications of self-heating (SHE) in Ge-based CMOS transistors.

Unfortunately, the bulk thermal conductivity of Ge is only half of that of Si [21], [22]; moreover, the thin body limits heat dissipation, and multigate approach increases thermal crosstalk among the nanowires (NWs) [23]–[27]. Given the well-documented challenge of SHE in surround gate Si-FET, one wonders if the advantages of high-mobility will be erased by SHE, making Ge-FET no more scalable than classical Si-FET. In this paper, we will use a combination of experimental analysis and theoretical (material device circuit) modeling to answer this technologically important question.

This paper is organized as follows. We first summarize in Section II the electrical and optical characterization techniques used to quantify the SHE characteristics of Ge transistors. We also explain the thermal and circuit simulation techniques used to evaluate circuit performance for the both Si and Ge CMOS technologies. In Section III, we carefully examine SHE in existing Ge-FETs by electrical (pulsed $I$–$V$) and optical methods (TR) to define the pathways for heat dissipation and time constants for heating and cooling for different geometries. In Section IV, we compare SHE of Si and Ge-FETs configured as a FinFET, SOI FinFET, and gate-all-around (GAA) FinFET to understand the dependence of SHE on transistor topology and channel material. Finally, in Section V, we use a SPICE-based electrothermal circuit simulation of a ring oscillator (RO) to compare that SHE in Ge CMOS with that of Si CMOS technology. Our conclusions are summarized in Section VI of this paper.

## II. Summary of Characterization and Simulation Techniques

### A. Sample Description

In this paper, we will use Ge nanowire CMOS consisting of an inversion mode (IM) PFET and an accumulation

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The authors are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: alam@purdue.edu).

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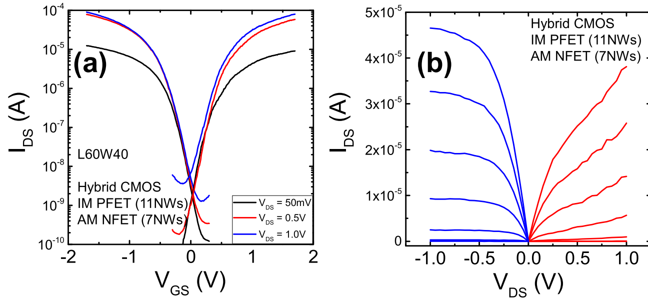

Fig. 1. (a) Transfer characteristics and (b) output characteristic of an IM PFET and an AM NFET transistor.

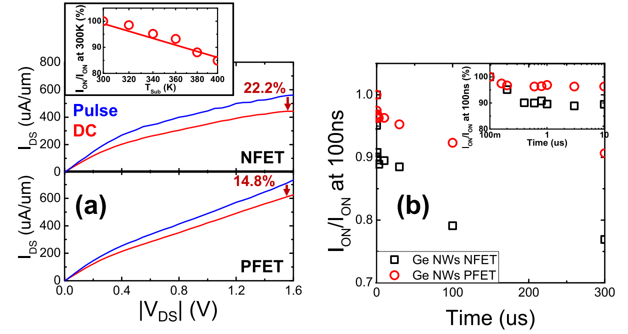

Fig. 2. (a) Output characteristic under dc and pulsed $V_{GS}$ are used to determine the SHE temperature. Inset: precalibration of $I_{ON}$ with chuck temperature. (b) Transient dynamics: $I_{ON}$ normalized at 100 ns. Inset: time axis in log scale [33], [39].

mode (AM) NFET, using the same samples reported in [17]. Unfortunately, CMOS-integrated high-performance IM NFET has not been reported in the literature and thus not available for our study. We used a variety of devices with different channel lengths ($L_{ch}$), widths ($W_{ch}$), and NW number. The devices were fabricated on a GeOI wafer so that the buried oxide (BOX) can be etched to release the NWs. A recessed S/D, formed by dry etching of the contacts, reduce the series resistance significantly. A subsequent dry etching formed the fins. There are 11 fins for PFET versus seven fins for NFET, so as to balance the current in a CMOS circuit. The NWs were suspended by removing BOX underneath the fins with HF solution. This air gap below the NWs is an important feature of these devices. High-quality $GeO_2$ using a postoxidation and $Al_2O_3$ using atomic layer deposition were used as stacked gate oxides ($T_{ox}$ = 10 nm and EOT = 4.5 nm). Highly conducting Ni/Au gate–source, and drain pads facilitate electrical and optical SHE characterizations. Indeed, a highly reflective Au top metal is essential for thermo-reflective imaging of SHE in these transistors. The detailed fabrication process is described in [17]. The specific PFET to NFET NWs ratio (11/7) ensures symmetric transfer and output characteristics [see Fig. 1]. It shows well-behaved gate controllability with subthreshold slope ~60 mV/dec. In addition to the samples just described, we will also investigate thermal performance of hypothetical thin body SOI (ETSOI) NFET and GAA NWs NFET to benchmark relative SHE in Ge CMOS transistors configured in various topologies. Detailed characterization of these floating body technologies have already been discussed in [24] and [28]–[32].

## B. Self-Heating Characterization Methods

SHE of the channel is characterized electrically by the well-known pulsed $I$–$V$ technique [33]. Theoretically, the technique relies on the inability of heat to follow high-frequency electrical pulses; therefore, the difference in drain currents under dc versus high-frequency pulses can be used to calculate channel SHE ($\Delta T_C$).

Similarly, thermoreflectance (TR) imaging has been used to measure spatiotemporal SHE of the channel as well as the width dependent SHE of the transistors. Theoretically, TR imaging monitors the changes in the complex refractive index of a material with differential increase in temperature ($\Delta T$), so that the change in local reflectance of the device surface can be expressed in terms of $\Delta T$ as follows:

$$\frac{\Delta R}{R_0} = \frac{1}{R_0} \cdot \frac{dR}{dT}\bigg|_{T=T_0} \Delta T \equiv C_{TR} \cdot \Delta T$$

where $C_{TR}(K^{-1})$ is the TR coefficient. For a comprehensive analysis of the theory and resolution limits of the TR technique, we refer the readers to [34]–[36].

## C. Simulation Methods

For electrical simulation of the transistors, we use the commercial simulator Senturus. The model was calibrated to reproduce the $I$–$V$ characteristics observed experimentally. For thermal simulation, we used 3-D finite-element method (FEM) simulator, COMSOL. The 3-D thermal simulations, based on Fourier law and standard material parameters are used to interpret the experimental results, identify pathways for heat dissipation, and define the impact of transistor topology (e.g., SOI, SOI Fin, NWs, and GAA) versus channel materials (Si and Ge) of SHE performance of a transistor. The physics of electrothermal coupling has been discussed in detail in [37]. The numerical modeling results are then encapsulated in the thermal circuit parameters ($R_{th}, C_{th}$) and used in a SPICE-based electrothermal simulator to evaluate the SHE in Si and Ge-based digital circuits (RO) [38].

# III. Characterization and Modeling of Self-Heating

## A. Determination of $R_{th}$

To determine channel temperature ($\Delta T_{C,\text{Avg}}$) by the pulsed $I$–$V$ measurements, we precalibrate $I_{ON}$ as a function of $T_{Sub}$ [see Fig. 2(a), inset]. Subsequently, we measure the difference between $I_{ON}$ at dc versus $I_{ON}$ under high-frequency pulses, and translate the difference to $\Delta T_{C,\text{Avg}}$ using the precalibrated curve. For the specific technology, $R_{th}(\equiv \Delta T_C/\text{Power}/\#\text{NW})$ for NFET and PFET are 3521.65 and 1698.59 (K/mW/NW), respectively. The transient response of $I_{ON}$ with pulse time shows that the circuit responds with sub – microsecond time constant [see Fig. 2(b)].

## B. Components of $R_{th}$

To delineate the heat diffusion pathways, we imaged the surface of self-heated transistors by TR measurement. First, the

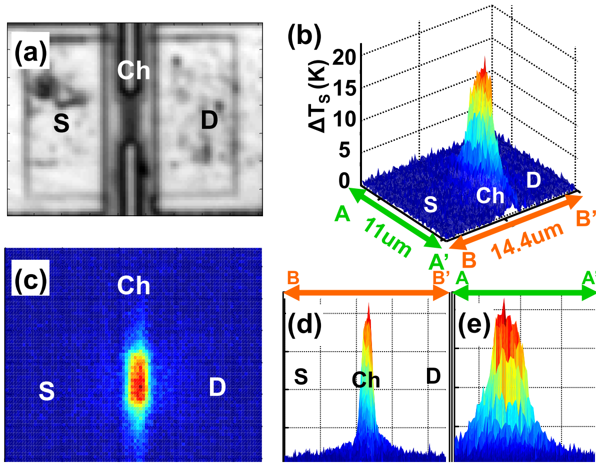


Fig. 3. (a) CCD top-view image of Ge NWs PFETs ($L_{ch}$ = 40 nm). (b) Perspective view. (c) Top view. (d) Front view (A–A'). (e) Cross section view (B–B') of TR images under steady-state SHE for $V_{DS}$ = 1.8 V and $V_{GS}$ = 1 V.

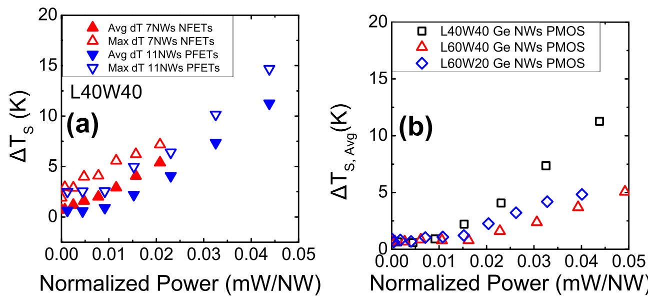


Fig. 4. (a) Steady-state gate surface temperature ($\Delta T_S$) of Ge N and P FETs depending on power dissipation per NWs. (b) Steady-state gate surface averaged temperature ($\Delta T_{S,Avg}$) of PFETs with a different $L_{ch}$ and $W_{ch}$, plotted as a function of power dissipation per NWs.

images in Fig. 3 confirm significant SHE of Ge-FET, consistent with the results from pulsed $I$–$V$ measurement. Second, SHE depends on geometrical parameters ($L_{ch}$, $W_{ch}$, and #NW) and the topology of the transistor. Specifically, Fig. 4(a) shows Ge-NFET (7NWs) has higher $R_{th}$ compared to that of Ge-PFET (11NWs), because Ge-NFET has smaller cross-sectional area to dissipate the heat through the substrate. Similarly, Fig. 4(b) shows how SHE depends on $L_{ch}$ and $W_{ch}$ of the transistor by gate surface temperature ($\Delta T_S$)-Power/NWs. The thermal modeling in Section III-C will demonstrate that transistors with smaller $L_{ch}$ and narrower $W_{ch}$ show steeper slope (higher $R_{th}$) because the reduced cross-sectional area ($A_{ch} = L_{ch} \times W_{ch}$) throttles heat dissipation through the substrate. Also, narrower $W_{ch}$ reduces heat diffusion from the channel to source and drain pads. In essence, the results suggest that heat diffuses first laterally through the channel to the S/D contacts and then vertically from the S/D contacts to the heat sink though the substrate.

## *C. Validation of $R_{th}$*

For a comprehensive understanding of heat diffusion in Ge-FET, we used 3-D COMSOL simulation of various transistor topologies (e.g., FinFET, SOI FinFET, NW-FET with the air gap, and GAA-FET) with various transistor parameters (#Fins or # NWs, $L_{ch}$ and $W_{ch}$) and channel materials (Si and Ge). The simulation parameters are summarized in Table I. Fig. 5(a) and (b) reproduces the $R_{th}$ dependence with $L_{ch}$ and $W_{ch}$ observed in Fig. 4, thereby validating the numerical model. The results show $R_{th}$ is proportional to $1/A_{ch}$. Note that, gate oxide scaling fur sub-10-nm nodes does not play an important role in $R_{th}$ since the thermal resistance offered by the gate oxide constitutes only a small fraction of the overall $R_{th}$. However, the gate oxide is very close to the hot spot so that higher thermal conductivity of the oxide helps in the initial heat dissipation of a transistor [40].

For the substrate heat flux, the Ge-FET sample used in our study included an airgap below the substrate, as a leftover of the NW release process [17]. Thermally, this topology is suboptimal, because the airgap insulates the channel and increases its $R_{th}$. Once the device is optimized and the airgap is

TABLE I
SIMULATION PARAMETERS FOR THERMAL PROPERTIES AND STRUCTURES

| | Parameters | | |
|---|---|---|---|
| Thermal Conductivity (K - W/mK) | Channel | Si | Ge |
| | Bulk | 131 | 60 |
| | Thin | 11.62 | 8.62 |
| Structures | Fin, SOI-Fin, NW with air, GAA NW | | |
| # of NW | 1-11 | | |
| $L_{ch}$ (nm) | 40 | | |
| $W_{ch}$ (nm) | 40 | | |
| $H_{ch}$ (nm) | 10 | | |
| $T_{ox}$ | 10nm $Al_2O_3$ (EOT = 4.5nm) | | |
| $T_{BOX}$ | 150nm $SiO_2$ | | |
| $L_{SD,Ext}$ (nm) | 100 | | |

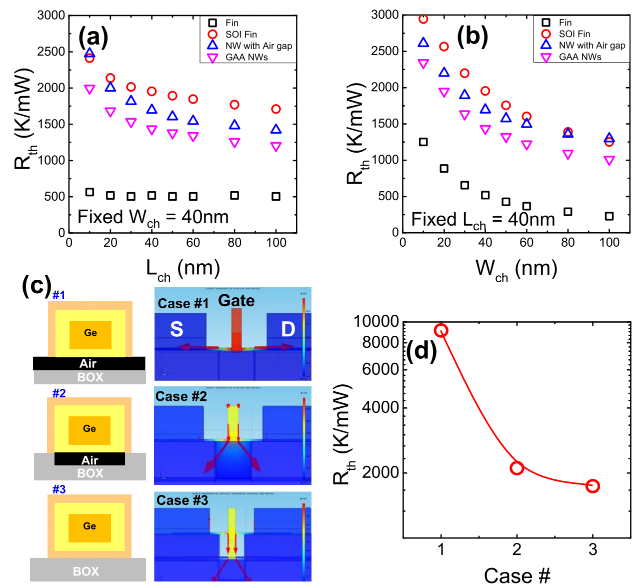


Fig. 5. (a) Plot of $R_{th} = \Delta T_C$/power versus channel length, $L_{ch}$ ( = 10 100 nm). (b) Plot of $R_{th}$ versus channel width, $W_{ch}$ ( = 10–100 nm) for the four structures with a single Fin or NW [Fin, SOI Fin, NW with the air gap (current Ge NWs CMOS), and GAA NWs]. (c) Schematics of cross section of various structures and heat dissipation pathways for various structures. (d) $R_{th} = \Delta T_1$/power for various structures, such as #1: Ge NWs air suspended without touching to BOX, #2: Ge NWs with air (current technology), and #3: Ge GAA NWs (the most electrically confined structure).

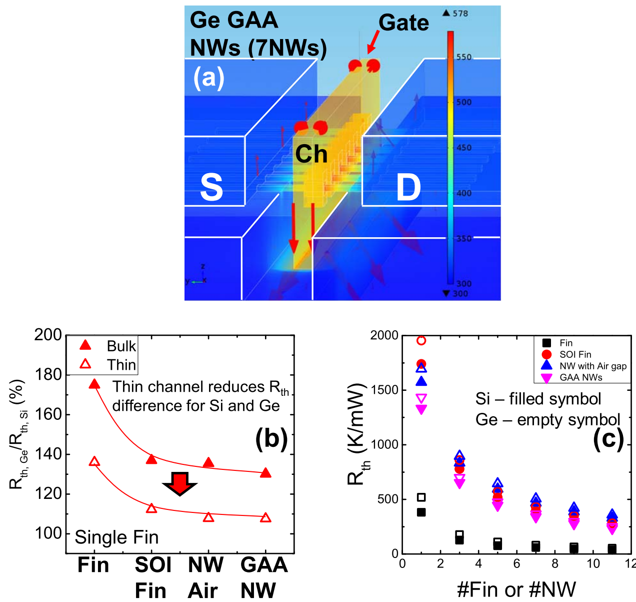


Fig. 6. (a) Example of Ge GAA NWs simulation. GAA NWs structure allows efficient heat dissipation through the substrate. (b) $R_{th,Ge}/R_{th,Si}$ obtained by using bulk versus thin channel thermal conductivity. The thin-channel conductivities of Si and Ge are comparable, resulting in comparable thermal resistances for a given device structure from COMSOL. (c) $R_{th}$ decreases rapidly with the number of NW (or Fins) both for Si and Ge. The difference is thermal resistance is relatively small.

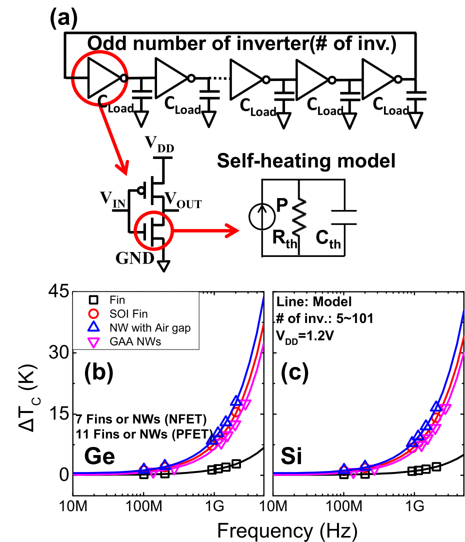


Fig. 7. (a) Schematic of an RO circuit consisting of odd # of inverters. The SHE model of each transistor, consisting of $R_{th}$ and $C_{th}$ obtained from simulation/measurements is also shown. (b) $\Delta T_C$ rises as a function of oscillation frequency for the four device structures [Fig. 7(a)] and channel materials. The oscillation frequency is controlled by changing the number of inverters. The solid lines define the analytical model, $\Delta T_C = P_{Avg} \times R_{th}$. (c) Comparison of thin Si and Ge channels for different device structures for a RO operating at 1 GHz.

removed (cases #2 and #3), $R_{th}$ drops dramatically as expected [see Fig. 5(d)].

## IV. Comparison With Si CMOS

So far, we have investigated area dependence and dominant heat pathways to the heatsink through the substrate. Now, we can couple the parameters obtained experimentally (see Table I) with 3-D COMSOL simulation of the Si and Ge channel configurations to isolate the effects of transistor topology versus channel material. In this regard, it is important to note that the thermal conductivity of thin-film Ge is much lower than that of *bulk* Ge. Equally important, the ratio of the thin-film conductivities of Si and Ge is much smaller than the bulk counterparts. Fig. 6(a) shows the SHE simulation of a hypothetical Ge GAA FET, and Fig. 6(b) shows $R_{th,Ge}/R_{th,Si}$ to assess the relative SHE in these technologies. Even though $R_{th,Si}$ is 40% smaller than $R_{th,Ge}$ for a FinFET, however, this advantage erodes quickly with additional confinement of SOI-FinFET or GAA structures. After all, the heat now must first flow to the S/D pads, and then escape through the thick substrate. Any difference in channel thermal conductivity makes a relatively small contribution (its low thermal conductivity is balanced by relatively short channel length) to the overall thermal conductivity. This conclusion holds for even when #Fins or #NWs is increased [see Fig. 6(c)]. Obviously, a transistor with additional fins or NWs has the larger footprint and reduced thermal resistance, but the difference between Si versus Ge channels is negligible. Based on these results, we reach an important (but somewhat counterintuitive) conclusion that for GAA or SOI FinFET, SHE will be dictated primarily by transistor geometry, S/D contacts, and the substrate, but not by the thermal conductivity of the channel material. The results are explained by the fact that the thin-film conductivities of Si and Ge are comparable [Fig. 6(a)] and the thermal resistance associated rest of the larger transistor structures are identical. Although the results were derived for relatively large pitch (∼200 nm) transistor, the key conclusions are valid for smaller pitch as well. In fact, additional simulations (not shown) demonstrate that $R_{th,Ge}/R_{th,Si}$ is essentially independent of fin-pitch for a multifin device structure. This is because the overall thermal resistance is dictated by the thermal resistance of the channel, with a much smaller contribution from thermal crosstalk between neighboring fins.

## V. Circuit Analysis of Ge CMOS

The SHE modeling of a digital circuit requires two elements: a Berkeley short-channel IGFET model (BSIM)-model for the transistor to calculate the power dissipated ($P$) and a thermal compact model, consisting of thermal resistance ($R_{th}$) in parallel with a thermal capacitance ($C_{th}$), driven by $P$ [see Fig. 7(a)]. The BSIM model parameters were obtained by careful analysis of Ge-FET $I$–$V$ characteristics obtained experimentally, as discussed in Section II. Similarly, $R_{th}$ and $C_{th}$ were obtained experimentally calibrated 3-D COMSOL FEM thermal simulation. To fairly compare the SHE behavior of RO with different channel materials/topologies, we biased the circuit at iso-power points and calculated the temperature rise for the corresponding power dissipation.

Based on the coupled electrothermal SPICE model, we can compare the relative performance of Ge versus Si circuits. Consider a RO with a variable number of inverter stages ($N_{inv}$) loaded by a fixed capacitor $C_{Load} = 20\ fF$ to represent the fan-out. The oscillation frequency is defined as $f = I_d/(C_{Load} \times V_{dd} \times N_{inv} \times 2)$, which means that the larger

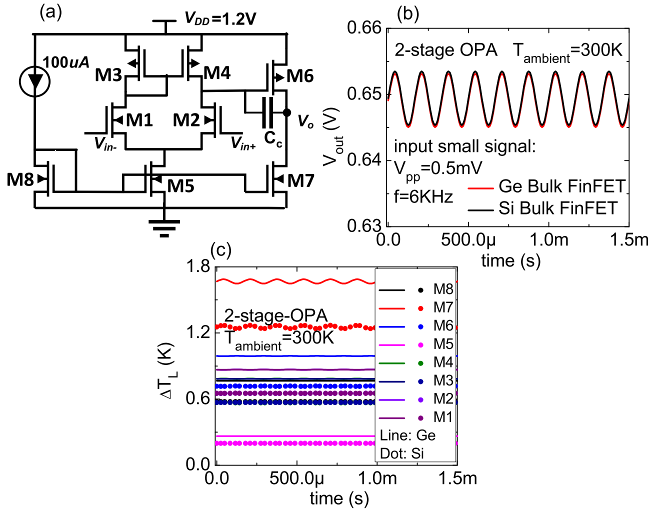


Fig. 8. (a) Schematic of a two-stage OPA. (b) Comparison of the output waveform in two-stage OPA consisting of Ge bulk FinFET and Si bulk FinFET. (c) Lattice temperature rise ($\Delta T_L$) caused by SHE in each transistor of the two-stage OPA.

number of the inverter (stage), the smaller oscillation frequency. Fig. 7(b) and (c) summarizes temperature rise in the channel ($\Delta T_{\text{avg}}$) as a function of oscillation frequency for Ge and Si transistors, respectively. Here, $\Delta T_{\text{avg}}$ increases with oscillation frequency because of the frequency-dependent increase of the average power ($P_{\text{Avg}}$). Thus, the analytical formula of average temperature $\Delta T_C^{\text{avg}} = P_{\text{Avg}} \times R_{\text{th}}$ (solid line) captures SHE well [40].

The results in Fig. 7(b) show that among the various structures, Ge NW FET with air gap has the highest $\Delta T_{\text{avg}}$, followed by SOI-Fin and GAA NW. As expected, the SHE is bulk FinFET is much smaller than other transistor geometries, also expected. Comparing Fig. 7(b) versus Fig. 7(c), however, we find that for Ge and Si transistors of comparable geometries, SHE are essentially identical (within 2–3 C).

Next to explore the importance of SHE in analog circuits, we compared the SHE in a two-stage operational amplifier (OPA) consisting of Ge bulk FinFETs versus Si bulk FinFETs, as shown in Fig. 8. The typical schematic of the two-stage OPA consists of a differential amplifier and a common source amplifier, as shown in Fig. 8(a). The comparisons of the output waveforms with the same input signal in the OPA consisting of Ge and Si bulk FinFETs are demonstrated in Fig. 8(b). The results show that the output waveforms do not differ significantly. The rise in the lattice temperature ($\Delta T_L$) caused by SHE in each transistor is illustrated in Fig. 8(c). Although $\Delta T_L$ in OPA consisting of Ge bulk FinFETs is slightly higher than that of *Si* bulk FinFETs, the maximum $\Delta T_L$ are relatively small (<2 K). This is because the typical quiescent points (Q-point) chosen in the range of 50–200 mV above threshold voltage ($V_{\text{th}}$), which leads to low power consumption in each transistor [41].

The lattice temperature and performance in the RO circuit and the two-stage OPA circuit are benchmarked under different ambient temperatures ($T_{\text{ambient}}$), and the results are illustrated in Fig. 9. Since $\Delta T_L$ is small in all situations (the maximum $\Delta T_L$ is around 3 K), $T_L = \Delta T_L + T_{\text{ambient}}$ is dominated by $T_{\text{ambient}}$ and increases linearly with $T_{\text{ambient}}$. Thus, the difference of $T_L$ between Ge and Si bulk FinFETs in the RO and two-stage OPA can be neglected, which leads to the similarity of gate delay and gain degradation between Ge and Si bulk FinFETs in the RO and two-stage OPA, respectively. Therefore, from the perspective of SHE in the RO and two-stage OPA circuits, Ge CMOS technology is a viable alternative to classical Si CMOS technology.

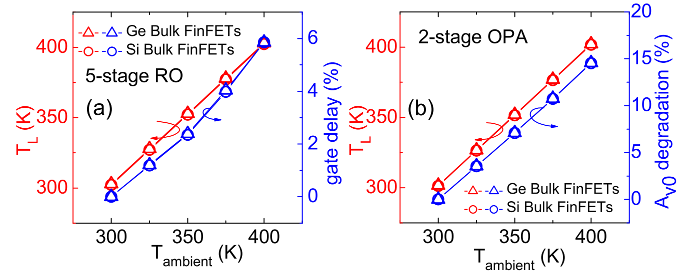


Fig. 9. (a) Lattice temperature ($T_L$) and the gate delay per stage as a function of ambient temperature in five-stage RO consisting of Ge bulk FinFETs and Si bulk FinFETs. (b) Lattice temperature ($T_L$) and the gain degradation as a function of ambient temperature in two-stage OPA consisting of Ge bulk FinFETs and Si bulk FinFETs.

## VI. Conclusion

In this paper, we have systematically characterized the electrothermal performance of recently developed Ge CMOS technology through extensive characterization and the 3-D numerical modeling. The results were then compared with corresponding Si CMOS transistors, configured in a similar topology. Our results show that despite the difference in the bulk thermal conductivities between Si and Ge, the SHE performances are essentially identical at the circuit level. This is because SHE in sub-10-nm technologies with surround-gate topologies (GAA-FET and SOI-FinFET) is in effect dictated by transistor topology and the substrate, and therefore, SHE will be essentially independent of the channel materials. Our results, therefore, encourage a sustained development of Ge-CMOS technologies as a viable alternative to classical Si-CMOS technology.

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