Charge Collection Mechanisms in GaAs MOSFETs

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***Abstract*—Charge collection mechanisms are investigated in surface channel GaAs MOSFETs under broadbeam heavy ion irradiation and pulsed two-photon-absorption laser irradiation. The large barrier between the gate dielectric and GaAs eliminates gate conduction current, but there is significant gate displacement current. Charge enhancement occurs because radiation-generated holes accumulate in the substrate, which increases the local electrostatic potential. The increased potential enhances the source-to-drain current, resulting in excess collected charge. The collected charge increases significantly with gate bias, due to the long tails of the charge waveforms that occur for higher gate bias. The collected charge increases with increasing drain bias.**

***Index Terms*—Charge collection, GaAs, III-V, InGaAs, ion radiation effects, MOSFETs, single-event transient, technology computer-aided design (TCAD), two-photon- absorption (TPA).**

I. Introduction

GAAS, due to its high electron velocity, is a promising channel material for future logic device applications [1]. Most GaAs transistors are MESFETs, but great efforts have been made to grow high quality dielectric layers on GaAs to enable fabrication of MOSFETs [2]. The low-power and high-speed of GaAs MOSFETs make them strong candidates for space applications. Extensive research on radiation effects in GaAs MESFETs/HEMTs and ICs [3]–[20] shows that GaAs MESFETs and HEMTs typically are resistant to total ionizing dose (TID), but relatively vulnerable to single event effects (SEE). On the other hand, transients and charge enhancement have been reported in InGaAs quantum-well MOSFETs [21]. The soft error performance in III-V FinFETs has been compared with Si FinFETs through simulations [22]. This body of research suggests that III-V MOSFETs are relatively susceptible to soft errors.

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In this work, the single event transient response of surface channel GaAs nMOSFETs is characterized and charge collection mechanisms are discussed and compared with other types of GaAs FETs and other III-V HEMTs.

When no gate dielectric exists between the gate electrode and the channel, such as in GaAs MESFETs [4], or when the barrier between the gate dielectric and the channel is small, such as in some GaN MOS HEMTs [23], there can be gate transients caused by conduction current. The gate transients can be eliminated if the barrier between the gate and channel is sufficiently large, which was demonstrated in InGaAs MOSFETs [21]. In this work, experiments and 2D TCAD simulations show that the large conduction band and valence band offsets between the gate dielectric and the GaAs channel eliminate the gate conduction current, but significant gate displacement current is present. This large displacement current differs from the results reported previously for other types of III-V FETs.

Charge enhancement (more charge is collected than deposited) has been observed in different kinds of III-V FETs, including GaAs MESFETs [5]–[7], [19], [20], InGaAs MOSFETs [21], InAs HEMTs [24] and InP HEMTs [25]. Enhancement occurs in *n-channel* devices because radiation-induced holes accumulate beneath the gate, perturbing the local electrostatic potential, lowering the source to channel barrier, and inducing a source-to-drain current pathway. The location at which holes accumulate depends on the specific device type (in the substrate for GaAs MESFETs [19], [20], in the buffer layer for InAs HEMTs [24], or in the channel for InP HEMTs [25] and InGaAs MOSFETs [21]). For GaAs MOSFETs, the charge enhancement mechanism is similar to that in GaAs MESFETs; holes accumulate in the substrate and cause extra charge to be collected.

II. Device Description

The devices under test are surface channel GaAs nMOSFETs with gate lengths of 2 and 4 μm; the schematic cross-section is shown in Fig. 1(a). The gate dielectric is composed of 4 nm of La_2O_3 grown on top of a 350 μm thick semi-insulating (SI) GaAs substrate by atomic layer epitaxy (ALE), with 4 nm of Al_2O_3 on top of the La_2O_3 for protection. The distance between electrodes varies with the gate length and is given for devices with $L_G = 4$ μm in Fig. 1(a). The detailed process information is found in [2]. The band diagrams along a vertical cutline through the gate oxide at zero bias applied to all terminals are shown in Fig. 1(b). The electron and hole quasi-Fermi levels

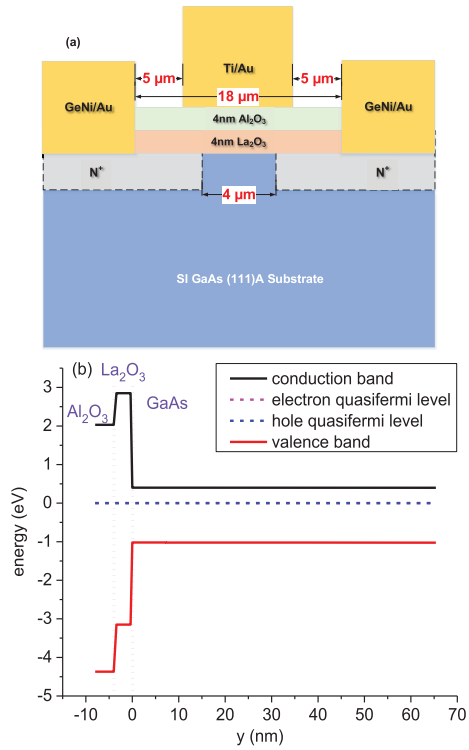

Fig. 1. (a) Schematic cross section of the device with $L_G = 4$ μm; (b) band diagram along a vertical cutline through the gate oxide at $V_G = V_D = V_S = 0$ V. The band diagram is generated from Sentaurus TCAD simulation.

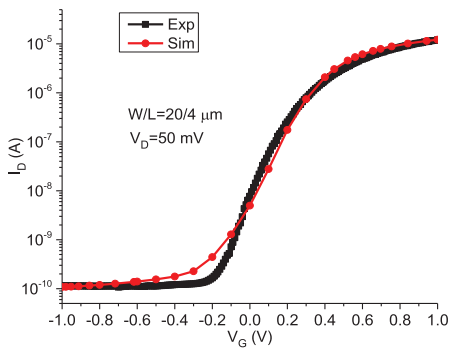

Fig. 2. Measured and simulated $I_D - V_G$ transfer characteristics. $V_D = 50$ mV during measurement. Simulation is done with Sentaurus TCAD tools.

are the same in this case because zero bias is applied to all terminals. The conduction band and valence band offsets between La_2O_3 and GaAs are 2.4 eV and 2.1 eV, respectively [26].

The $I_D - V_G$ transfer characteristic is shown in Fig. 2. The experimental data and simulation data agree well. To simulate the semi-insulating GaAs substrate, carbon acceptor doping and deep donor traps are included [27]. Devices with gate lengths of 2 μm and 4 μm and gate widths of 20 μm and 33 μm were tested ($W/L = 20/4$, 20/2, and 33/4). For both heavy ion experiments and laser experiments, at least three devices were tested. For transient capture, all the devices are mounted in custom milled high-speed packages [21]. For the laser experiments, the backsides of the DUTs were polished before mounting in high-speed packages.

TABLE I
DETAILS OF IONS USED IN EXPERIMENT

Ions	Energy (MeV)	LET (GaAs) (MeV•cm^2/mg)	Range (μm)
Oxygen	14.30	4.3	7.5
Neon	89.95	3.9	35.6
Krypton	387.08	26.6	32.8
Xeon	602.90	47.0	33.0

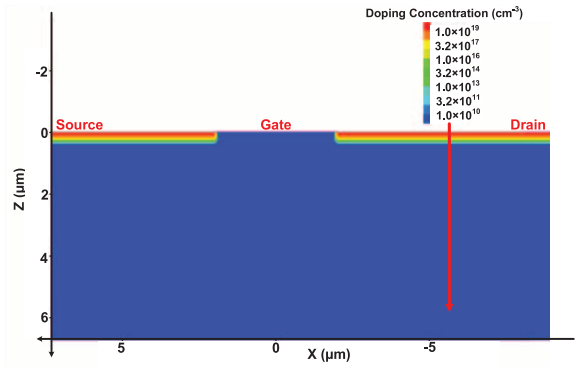

Fig. 3. Device model used in 2D TCAD simulation. Here the drain is in the negative x direction and source is in the positive x direction. The red arrow indicates the strike location, $x = -6$ μm. For the simulation, Sentaurus TCAD tools are used.

III. EXPERIMENTAL AND SIMULATION DETAILS

Broadbeam heavy ion irradiation was performed using oxygen ions in Vanderbilt's Pelletron electrostatic accelerator and different ions at the Lawrence Berkeley National Laboratory. The details of the ions are shown in Table I.

Two-photon absorption (TPA) pulsed laser irradiation is a valuable method to investigate charge collection mechanisms [28]. TPA laser irradiation was performed at Vanderbilt University. All devices were irradiated from the backside by high peak power femtosecond laser pulses. The experimental setup is described in [21]. The laser wavelength is 1.26 μm and the nominal pulse width is approximately 150 fs. The device under test was fixed on an automated precision linear stage with a resolution of 0.1 μm. Optical pulses were focused through the backside of the die onto the front surface of the DUT, using a (100 X) microscope objective with a charge generation spot size of ~ 1.2 μm in GaAs. The laser photon energy is 0.98 eV, which is less than the GaAs band gap of 1.42 eV. As a result, the carriers are generated primarily through two-photon absorption [28].

Quantitative understanding of TPA laser experiments is challenging and remains an active area of research [29]. In this paper, TPA laser experiments are used to map the sensitive areas of the devices by scanning the laser beam across the active areas with varying gate and drain biases. The transients were captured using a Tektronix TDS6124C oscilloscope with 12 GHz front-end bandwidth and 20 GS/s sampling rate. Each oscilloscope channel has 50 Ω input impedance, which is used to convert the transient current to a measurable voltage. During these tests, the source was grounded and the gate bias and the drain bias were varied. A semiconductor parameter analyzer, HP 4156B, supplied the dc biases through Picosecond Model 5542 bias tees with 50 GHz bandwidth.

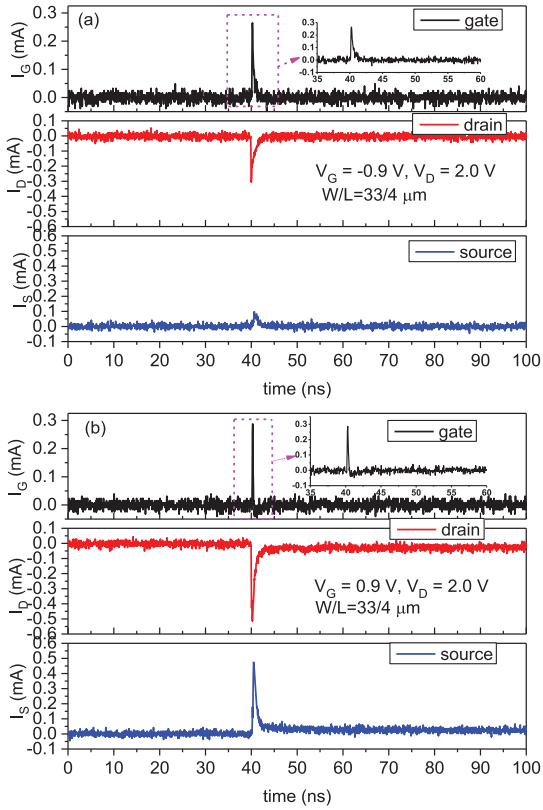

Fig. 4. Representative transients under oxygen ion irradiation at (a) OFF, $V_G = -0.9$ V; (b) ON bias conditions; $V_G = 0.9$ V for a device with $L_G = 4$ μm. For this device, $V_{TH} = 0.4$ V. The inset of the figure shows the zoom into the magenta box region.

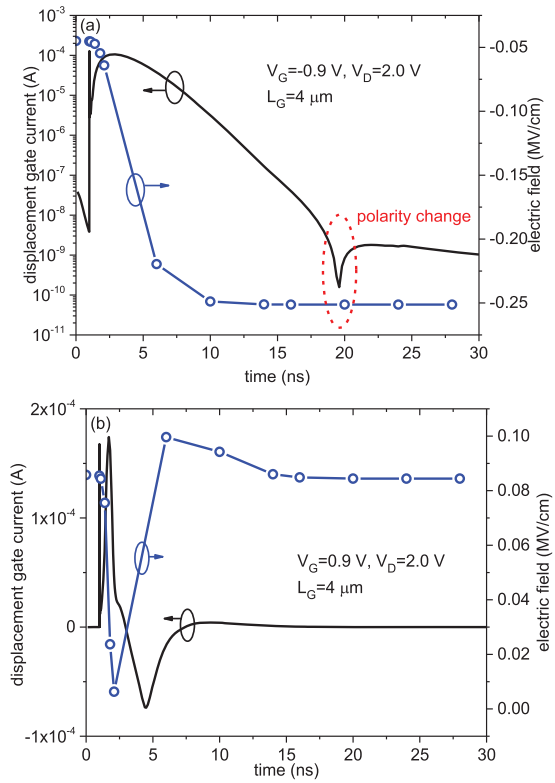

Fig. 5. Displacement gate current and electric field in La_2O_3 as a function of time at (a) $V_G = -0.9$ V; (b) $V_G = 0.9$ V.

2D TCAD simulations, performed with Sentaurus TCAD tools, were used to understand the charge collection process during heavy ion strikes. The models used include drift and diffusion transport, inversion and accumulation layer mobility models, and electron velocity saturation models [30]. In addition, the SRH, radiative and Auger recombination models are used. Events produced by oxygen ions are simulated. The center of the strike is at 1.0 ns, and the strike center is at $x = -6$ μm, as shown in Fig. 3. The radius of the strike is 50 nm. During the simulation, $V_D = 2.0$ V and V_G was varied to study the gate bias dependence.

IV. Experimental Results and Discussion

A. Broadbeam Heavy Ion Tests

Fig. 4(a) and (b) show the transients for a device with $L_G = 4$ μm for OFF and ON gate biases under oxygen ion irradiation. For all transients, the DC current is filtered out and only AC current transients are shown. Under both bias conditions, there are strong gate transients. Positive and negative gate transients correspond to charging and discharging of the gate capacitance, respectively. After an initial positive transient, the gate current polarity changes for devices biased in the ON state (see inset in the top panel of Fig. 4(b)), which is a strong indication of displacement current through the gate dielectric [31], [32]. This polarity change is not observed for devices in the OFF state (see inset of Fig. 4(a)). If there is any negative gate current in the OFF state, it is obscured by the oscilloscope noise.

Fig. 5(a) and (b) show the simulated gate displacement current and electric field in the La_2O_3 as functions of time at $V_G = -0.9$ V and $V_G = 0.9$ V, respectively. The gate transient at $V_G = -0.9$ V is displayed on a log scale to show the polarity change more clearly. When the device is biased in the OFF state, there is a large initial positive gate transient, followed by a polarity change. The electric field in the gate dielectric increases up to 20 ns, and after that it slowly decreases. The moment the electric field reaches a peak is when the gate transient changes polarity. The negative gate current is orders of magnitude smaller than the positive peak gate current, which explains why only positive gate transients are observed in Fig. 4(a). The negative portion of the gate transient is small and likely obscured by the instrument noise.

Also, as shown in Fig. 5(b), when the device is ON, there is a clear polarity change in the gate transient, consistent with the heavy ion data in Fig. 4. The polarity change happens quickly, at approximately 3 ns. The electric field in the gate dielectric decreases up to 3 ns, and then increases to the steady state value.

The source transients differ significantly between the ON and OFF states. During the OFF state, source transients are small, with peak current less than 0.1 mA, which is smaller than the gate transients. When the devices are irradiated in the ON state, the drain and the source transients are approximately equal. This is because the channel resistance is much higher in the OFF state and the source and drain are electrically isolated, which suppresses the source to drain current [33]. However, when the device is biased in the ON state, the source and drain are electrically connected, resulting in large source to drain current.

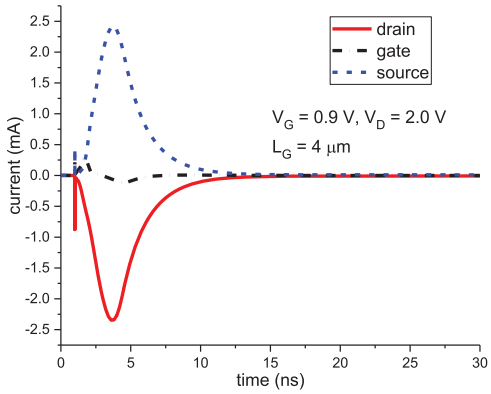

Fig. 6. Simulated current transients at $V_G = 0.9$ V, $V_D = 2.0$ V when striking at $x = -6$ μm. The current is scaled by the width of 33 μm.

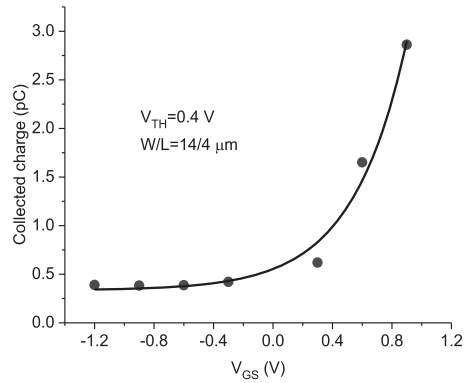

Fig. 7. Drain collected charge as a function of gate bias under oxygen ion irradiation. $V_D = 2$ V during irradiation.

The simulated transients are shown in Fig. 6 biased at $V_G = 0.9$ V. The gate transient, showing the polarity change, is displacement current as discussed in Fig. 5(b). The source and drain transients are approximately equal and opposite, meaning the current comes from the electrons traveling from source to drain. The simulated transients also illustrate charge enhancement, since the charge deposition is 0.58 pC while the drain collected charge is about 8.5 pC. These simulations are not quantitative, however, primarily because they are conducted with 2D rectangular coordinates. In addition, the parasitic capacitance and inductance of the device and the experimental setup are not included. While the simulation results are qualitative, they do illustrate the key characteristics.

The OFF state bias allows radiation-generated holes to stay under the gate dielectric because the electric field attracts the holes. In the ON state, however, holes are repelled from the gate. Consequently the ON state has a stronger restoring force, restoring the pre-strike steady state quickly, and leading to larger displacement current. For the OFF state, in contrast, it takes a longer time to remove radiation-generated holes to recover the pre-strike steady state, so the displacement current lasts for a longer time. The high resistivity and deep traps in the semi-insulating GaAs inhibit hole transport to the substrate contact. Such long-lasting displacement current is typically not observed in Si nMOSFETs because the substrate is quite conductive.

For irradiation in the ON state, source and drain transients have long tails that may last microseconds. This behavior is repeatable both in heavy ion and laser irradiation. The collected charge is obtained by integrating the recorded transient. For transients without long tails, the integration time window used is the region where the transient is larger than 1% of the peak current value, which reduces the noise contribution. For transients with long tails, the end of the integration time is selected to be 200 ns, which is the sampling window during the experiment. The collected charge is shown as a function of gate bias in Fig. 7. Again when the device is ON, there is a long tail in the transient, which contributes a large amount of collected charge. As a result, the collected charge increases with the gate bias. As the oxygen ion generates about 0.58 pC of charge, approximately 3 pC of collected charge corresponds to a charge enhancement factor of 5. This is consistent with the results reported in other types of GaAs FETs [3], [6].

Both positive and negative long-tail transients (compared with the DC terminal current) have been observed in irradiated GaAs FETs [8]–[16]. Deep traps in the substrate close to the channel are responsible for long transients. Negatively-charged traps deplete the channel and decrease the channel current, while positively-charged traps increase the channel current. This process lasts until the trapped electrons/holes are emitted from the deep traps, which may require microseconds or even seconds. For the GaAs MOSFETs examined here, the effects appear to be due to holes trapped in deep traps in the substrate, which backgate the channel and induce long term transients, similar to the results described in [8]–[10].

The properties of the traps depend on the device structure, material, and process. Electron traps with activation energy in the range of 0.7 to 0.9 eV have been reported in previous work, which are related to Cr impurities or EL2 traps in the GaAs substrate [12]–[16]. Similar energy levels are reported for hole traps. Shallower traps with activation energies of 0.57 eV, 0.37 eV and 0.14 eV also have been reported in GaAs MESFETs/MODFETs [10], [14]–[16]. The specific type of trap responsible for the long tail in the GaAs MOSFETs evaluated here remains to be determined, but likely are also deep levels in the substrate. Hardening techniques to reduce the long-term transients, such as including a buried p-layer under the active region and AlGaAs buffer [15], [16], may therefore also be applicable to these GaAs MOSFETs.

To understand the charge enhancement process, Fig. 8(a) shows the simulated electrostatic potential (colors) and hole density difference between post-strike (4.0 ns) and pre-strike conditions (contour lines). Holes accumulate in the substrate and the channel, due to their long lifetime in the substrate [17], [18], which leads to an increase in the local electrostatic potential. This potential increase backgates the channel and also produces bipolar amplification, which leads to source to drain current [4], [19], [20]. Fig. 8(b) shows the conduction band along a horizontal cutline in the channel located 50 nm below the gate dielectric. The conduction band energy drops about 0.37 eV at 4.0 ns, which is the peak of the transient, due to an increase in the electrostatic potential. Although the source to channel barrier remains high, about 0.7 eV, the source to drain current flows outside the depletion region, where the gate has little control, as shown later.

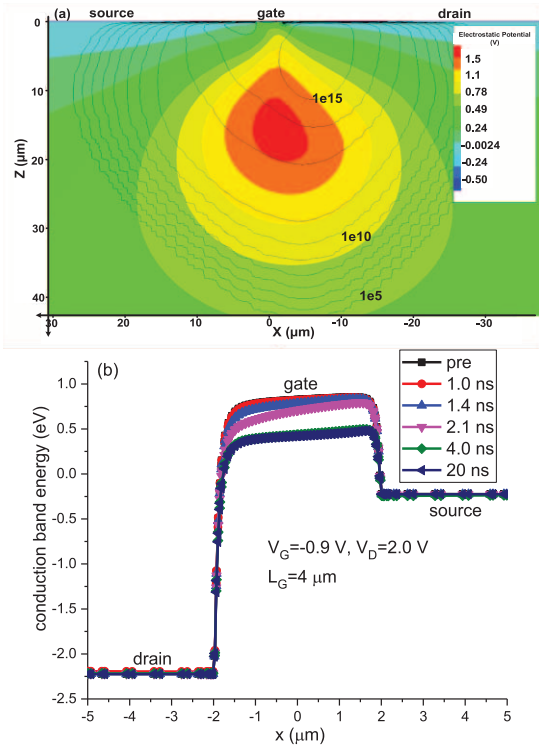

Fig. 8. (a) The color map shows the electrostatic potential difference and the contour plot shows the hole density difference between post-strike (4.0 ns) and pre-strike at $V_G = -0.9$ V. (b) The conduction band energy is plotted along a horizontal cutline at z = 50 nm at different times.

The cross section as a function of LET is shown in Fig. 9. Here two different kinds of cross sections are shown. The first is the event cross section, which is the total number of recorded events divided by total fluence. An event is triggered and recorded in the oscilloscope when the current is higher than 0.12 mA. However not all the recorded events would cause an upset in real applications. To illustrate the effects that may occur in a particular application, a cross section based on the number of recorded events with a peak drain current over 2 mA is also plotted (called the over-threshold cross section). The over-threshold cross section is plotted for two different gate biases. The event cross section is the largest, as it considers every event that is recorded. All cross sections increase with LET. Moreover, the over-threshold cross section at $V_G = 0$ V is slightly larger than the cross section at $V_G = -0.9$ V. This is because the peak drain current increases slightly with the gate bias, as discussed below.

B. Pulsed Laser Results

In order to understand the charge collection mechanisms more completely, pulsed laser irradiations were performed. A line scan from drain to source, parallel to the channel, was performed at different bias conditions, shown as the white and red dots in the inset of Fig. 10. Fig. 10(a) and (b) show the transients at $x = -22$ μm (red dot located in the drain and referenced to x-axis scale in Fig. 8(a)) of a line scan for devices in the OFF and ON bias conditions, respectively. In the OFF state, there is no source transient, and only the gate and the drain transients are present. However, when the device is ON,

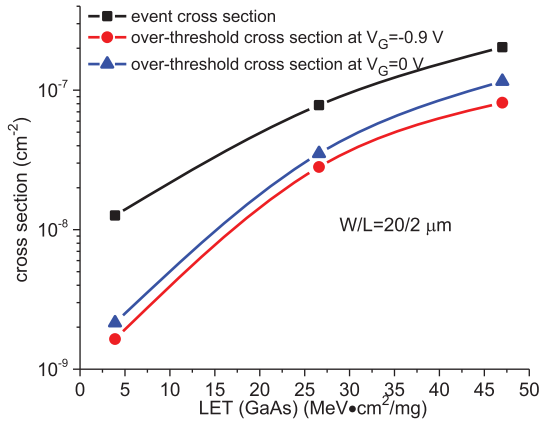

Fig. 9. The event cross section and the over threshold cross section at $V_G = -0.9$ V and $V_G = 0$ V as a function of LET. $V_D = 2$ V during irradiation.

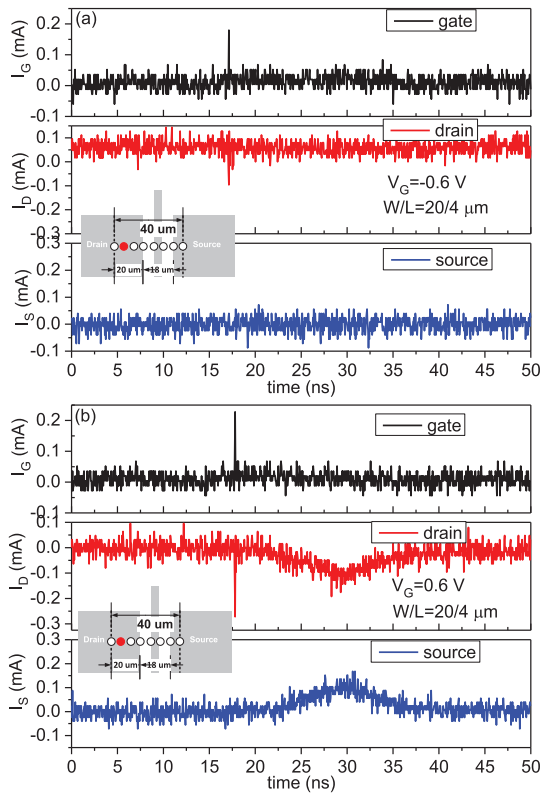

Fig. 10. Transients during pulsed laser irradiation for biases (a) $V_G = -0.6$ V; (b) $V_G = 0.6$ V. $V_{TH} = 0.3$ V, $V_D = 2.0$ V. The inset shows the line scan across the device during the laser irradiation. The white circles represent the possible scan points. The red circle represents the current strike point. For this transient, the current strike location is $x = -22$ μm. The center of the gate is taken as the origin, and the drain is in the negative x direction. The laser pulse energy is 0.51 nJ.

at the same strike location, there are source transients that are approximately equal to the drain transients. This behavior is consistent with the heavy ion results in which it was seen that in the OFF state, the source transients are quite small.

Two peaks are observed for drain transients in the ON state, similar to those shown in [3], [4], [6]. Following the strike, there is charge collection at very short times that relaxes so fast that it is limited by the instrument resolution. This is due to collection of the generated electrons close to the drain. The peak in the gate transients corresponds to the change of electric field in the

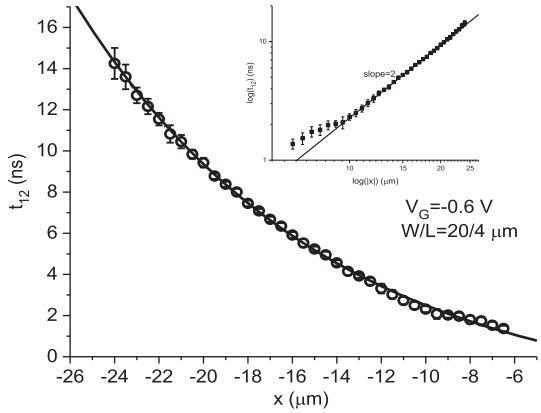

Fig. 11. The time difference between the first peak and second peak of the drain transients versus the strike location. Here the center of the gate is taken as the origin and the drain is in the negative x direction. The error bar represents one standard deviation of the transients taken at a single location. The inset plots the same data on a log-log scale.

gate dielectric during carrier generation, as shown in the simulated results in Fig. 5. This peak is due to displacement current, consistent with the heavy ion data and accompanying simulations. The second peak is due to the generated holes moving toward the source, which backgate the channel and/or induce the bipolar amplification. The time difference between the two peaks is related to the time required for holes to move toward the gate. Fig. 11 shows the time difference between the two peaks as a function of strike location. The farther the strike location is from the gate, the longer it takes for the second peak to show up. The inset shows the data in a log-log plot, in which the slope is very close to 2, which suggests that the time it takes for holes to move toward the gate is the diffusion time.

The source and drain collected charge and peak drain current along a line scan at different gate biases are shown in Fig. 12(a) and (b), respectively. On the drain side, the peak drain current increases with gate bias, indicating the sensitive area moves deeper into the drain with higher gate bias. This is consistent with the results shown in Fig. 10. The source and drain collected charge are approximately equal and increase with the gate bias. The region between the gate and the drain has the largest collected charge.

The increase of the collected charge with gate bias is partially due to the increase of the peak current with the gate bias. The greater contribution to the collected charge comes from the long tails in the ON state, as shown in Fig. 13. The peak drain current has little gate bias dependence; however, the tail current increases with the gate bias, also observed in GaAs MESFETs [8]. From $V_G = -0.6$ V to $V_G = 0.9$ V, the tail current increases by almost 0.05 mA, which can contribute as much as 3 pC to the total collected charge in a time window of 60 ns.

The peak drain current in these GaAs MOSFETs does not vary significantly with gate bias, which contrasts with results reported for several other types of devices. The peak drain current in InGaAs MOSFETs [21] and AlSb/InAs HEMTs [24]reached a maximum around the threshold or pinch-off voltage. For GaAs HFETs [6] and InP HEMTs [25], due to the limited bias range reported, such roll-off behavior at higher gate biases was not observed. In both devices, however, the peak

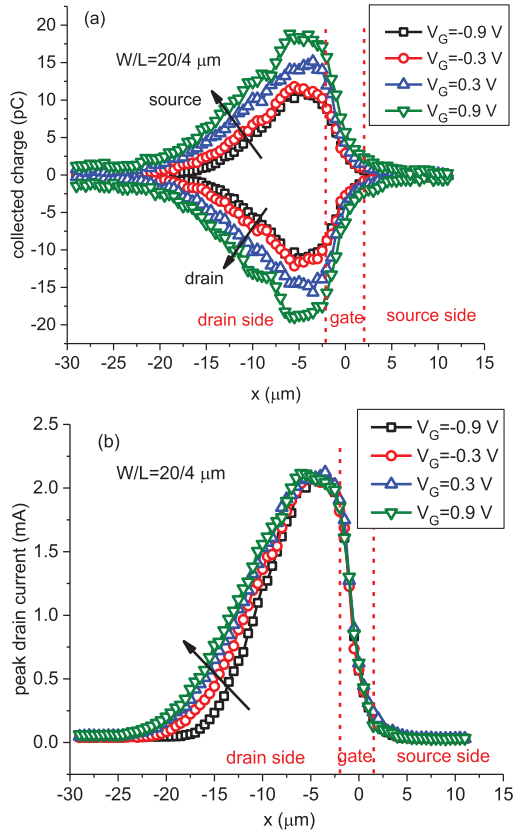

Fig. 12. (a) Collected charge, and (b) peak drain current along a line scan at different gate biases. $V_{TH} = 0.3$ V, $V_D = 2.0$ V. In (a), the positive collected charge corresponds to the source, and the negative collected charge corresponds to the drain. The arrows show the trends vs. gate bias.

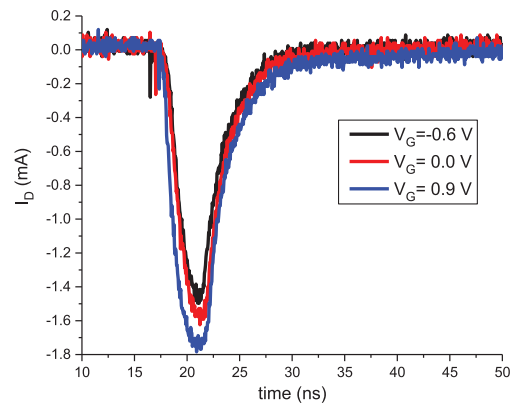

Fig. 13. Drain transients at different gate biases at a location of x $= -9$ μm. $V_{TH} = 0.3$ V, $V_D = 2.0$ V. The inset shows the tail portion of the transient.

drain current varied strongly with the gate bias. The peak drain current in these surface channel GaAs MOSFETs is relatively insensitive to gate bias because of the vertical band-structure of the device. Devices that are sensitive to gate bias usually have quantum-well channels, which confine the radiation-generated carriers. The gate has control over the quantum-well, which in turn controls the charge collection. However, for surface channel GaAs MOSFETs, significant current flows outside the gate control region, as shown below.

To study the gate bias dependence of the charge collection, simulated electron current density differences between post-ion-strike (4.0 ns) and pre-ion-strike at $V_G = -0.9$ V and $V_G = 0.9$ V are shown in Fig. 14(a) and (b), respectively, like that

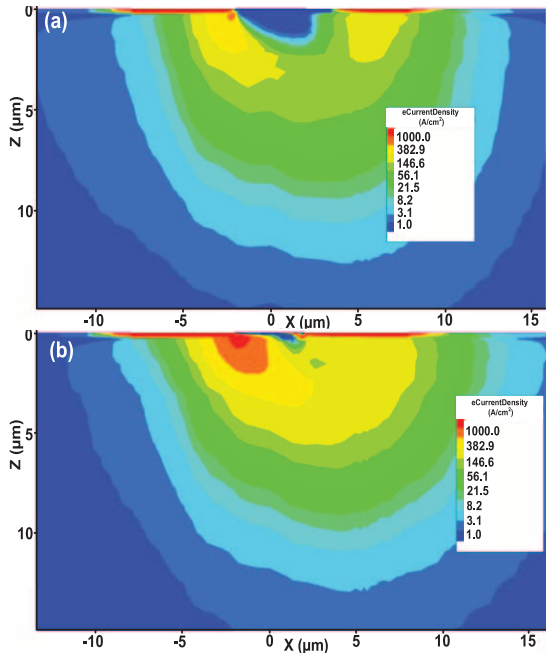

Fig. 14. Electron current density difference between post-strike (4.0 ns) and pre-strike at (a) $V_G = -0.9$ V; (b) $V_G = 0.9$ V.

is shown in [19]. In the OFF state, the current flows outside the depletion region, where the gate has little influence. The current is due to the source to substrate barrier lowering, as shown in Fig. 8 [19], [20]. In the ON state, the current density is higher compared with the OFF state, which explains the increase of the peak drain current with gate bias at the same strike location, as shown in Fig. 12(b). The current flows closer to the channel because there is no depletion region in the ON state. The current density is higher in the ON state because the depletion region in the OFF state pushes the current flow farther away from the channel. In the ON state, the current flows in the channel in addition to those regions away from the channel.

To understand the spatial dependence of the charge collection, a horizontal line scan similar to the TPA laser experiment is simulated in TCAD. Fig. 15 shows the simulated peak drain current along a horizontal cutline at $V_G = -0.9$ V and $V_G = 0.9$ V. The peak drain current increases with gate bias. The simulation results are qualitatively consistent with the TPA laser results of Fig. 12. These results show that the area between the gate and drain has the highest sensitivity, due to the higher electric field in those regions. The simulated current and the TPA laser results of Fig. 12 cannot be compared quantitatively because the simulations are conducted using 2D rectangular coordinates, but the trends in the peak current are replicated well via simulation.

Fig. 16 shows the peak drain current along a line scan at three different drain biases. The collected charge follows the same behavior as the peak drain current. The drain side is the most sensitive to the drain bias, while the areas below the gate and the source do not show drain bias dependence. The peak drain current increases with drain bias, similar to results in [6], [7], due to the higher electric field on the drain side when the drain bias is higher. The higher electric field leads to higher electron velocity, which means higher drain current for the same amount of charge generation. These results suggest that the sensitive volume increases with both drain and gate bias.

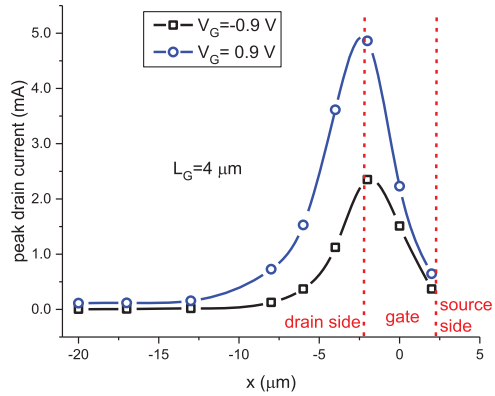

Fig. 15. Simulated peak drain current along a horizontal cut line at two different gate biases.

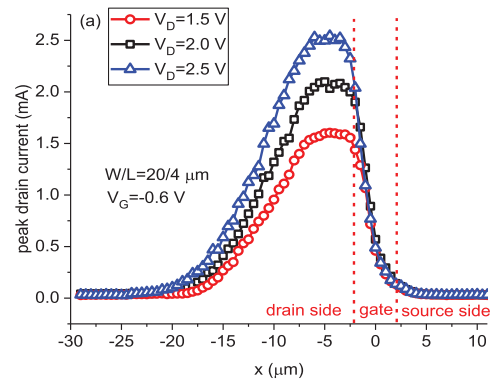

Fig. 16. Peak drain current along a line scan vs. drain biases. $V_{TH} = 0.3$ V.

V. Conclusions

The single event transient response of surface channel GaAs MOSFETs is investigated through broadbeam heavy ion irradiation and TPA laser irradiation. 2D TCAD simulations are used to understand the charge collection mechanisms. There are significant gate transients, even though the barriers between the gate dielectric and GaAs are large enough and the gate dielectric is thick enough to remove the possible conduction current through tunneling. Experimental results and TCAD simulations confirm that the transients come from displacement current. The presence of deep traps in the semi-insulating substrate lead to long-lasting tails in the displacement current.

The source transients are very small in the OFF state and slowly increase with the gate bias. The source transients are associated with the charge enhancement processes, such as backgating and bipolar amplification. These processes occur because the radiation-generated holes accumulate in the substrate and increase the local electrostatic potential, which backgates the channel and causes bipolar amplification. The long tails in the source/drain transients in the ON state are likely due to holes trapped in deep levels in the semi-insulating GaAs substrate, which can modulate the channel. In addition, experimental results suggest that the sensitive volume increases with the drain bias.

Because of charge enhancement effects, the soft error rate of GaAs MOSFET circuits may be higher than that of their silicon counterparts. For example, critical LET values lower than 1 MeV/mg/cm^2 [3] have been reported for GaAs MESFET logic. However, for GaAs MOSFET circuits, the error rate may

not be as sensitive to supply-voltage scaling as silicon because of its higher drive current. After an ion strike, GaAs circuits will have stronger restoring forces compared with silicon circuits, as shown in [22]. Hardening techniques could be used to reduce the charge enhancement effect by reducing the hole lifetime in the substrate. Techniques such as incorporation of low temperature grown GaAs buffer layers have been shown to be effective in reducing the enhancement effect [17], [18] in earlier studies of different device types; similar methods are also likely to be successful for these devices.

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