Properties of InAs metal-oxide-semiconductor structures with atomic-layer-deposited Al_2O_3 Dielectric

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(Received 25 July 2007; accepted 16 March 2008; published online 11 April 2008)

InAs is very attractive as a channel material for high-speed metal-oxide-semiconductor (MOS) field-effect transistors due to its very high electron mobility and saturation velocity. We investigated the processing conditions and the interface properties of an InAs metal-oxide-semiconductor structure with Al_2O_3 dielectric deposited by atomic-layer deposition. The MOS capacitor *I-V* and *C-V* characteristics were studied and discussed. Simple field-effect transistors fabricated on an InAs bulk material without source/drain implantation were measured and analyzed. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2908926]

The rapid growth of the integrated circuit industry has been based on the continuous scaling down of silicon metal-oxide-semiconductor field-effect-transistor (MOSFET) size. However, as channel lengths reach 22 nm, further scaling becomes problematic. High mobility III-V channel materials have emerged as a promising solution and are under intensive investigation to further improve the transistor performance.[1] Among the choices of alternative channel materials, InAs extraordinarily exhibits high electron mobilities ($\sim 33\,000\ cm^2\ V^{-1}\ s^{-1}$) and saturation drift velocities ($\sim 8 \times 10^7$ cm/s).[2] However, as is the case with most III-V semiconductors, the primary obstacle for the development of InAs MOSFET is the lack of a high-quality insulator-semiconductor interface. Previous efforts to develop InAs metal-oxide-semiconductor (MOS) structures with anodic oxide[3,4] and deposited SiO_2 (Ref. 5) resulted in big negative shifts of flatband voltage and large hysteresis, indicating high interface-state and bulk oxide charge densities.

Recent development in the deposition method of high-κ dielectrics has opened more possibilities in this area. Improvement of semiconductor-dielectric interface properties has been reported for GaAs and InGaAs with low indium concentration.[6,7] Compared to the aforementioned channel materials, InAs has a much higher bulk electron mobility and saturation velocity. Recently, InAs MOS structures with Al_2O_3 deposited with the molecular-atomic deposition (MAD) were fabricated and some properties reported.[8] In this work, we report InAs MOS structures with Al_2O_3 deposited by using atomic-layer deposition (ALD). Field-effect transistors (FETs) without source and drain implants were also fabricated and characterized on an InAs substrate.

The MOS capacitors and FETs were fabricated by using single crystal InAs wafers with a *p*-type doping concentration of 2×10^{17} cm^{-3}. The Al_2O_3 dielectric was deposited at 300 °C to a thickness of ~30 nm by using ALD. The MOS capacitor was made by depositing Al electrodes on top of the dielectric and a large-area Ti/Au backside contact. The sample was then annealed at various temperatures, followed by multifrequency *C-V* measurements. The best annealing temperature was found to be ~360 °C. Higher temperature annealing was found to damage the interface quality, which is observed as a degradation in the *C-V* and *I-V* characteristics, and through a change in the interface morphology observed under microscope. Figure 1(a) shows the measured current-voltage characteristics of an InAs/Al_2O_3 MOS diode. The leakage current is below 10^{-8} A/cm^2 at the biases lower than 10 V. Figure 1(b) is a Fowler–Nordheim tunneling fitting of the *I-V* curve. The tunneling current at biases above 10 V has a good fit with the Fowler–Nordheim tunneling mechanism, indicating a low trap density inside the dielectric. By using $m^*=0.23$ for Al_2O_3, the InAs/Al_2O_3 effective barrier height Φ_B was extracted to be ~2.3 eV from the slope of Fig. 1(b).

Figure 2(a) shows the multifrequency *C-V* curves measured on the MOS capacitors annealed at 360 °C for 30 s. The minimum capacitance was observed at ~−1 V. This is a smaller flatband voltage shift than previous reported values,[3–5] suggesting a much less bulk and interface trap densities. The MOS capacitor shows evidence of hole accumulation for negative biases and inversion for positive biases. We also observed frequency dispersion in the *C-V* characteristics, which may be explained by the lossy capacitance model,[9] which suggests that there is a thin layer with a finite resistance between the dielectric and the semiconductor. Figure 2(b) shows the simulated ideal *C-V* curves of *p*-InAs/ALD-Al_2O_3 MOS capacitors by using the Silvaco simulator. In the simulation, $N_c=8.7\times10^{16}$ cm^{-3}, $N_v=6.6$

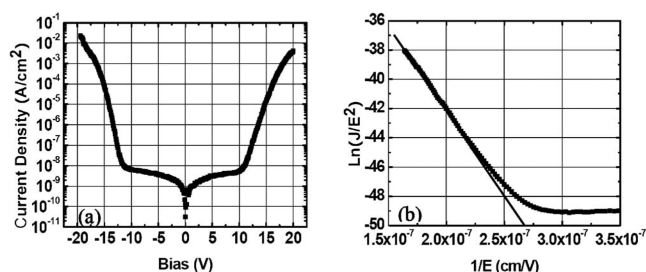

FIG. 1. Measured current density vs bias voltage of an InAs/ALD-Al_2O_3 MOS diode (a) and Fowler–Nordheim tunneling fitting of the MOS diode (b), where *E* is the electric field inside the oxide and *J* is the current density.

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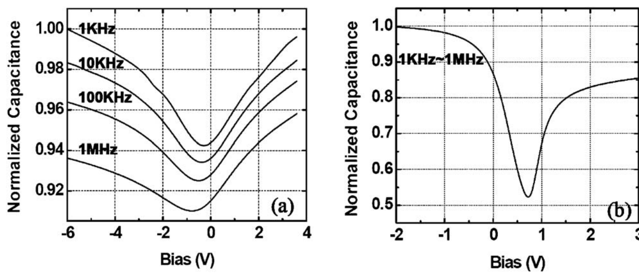

FIG. 2. Measured multifrequency *C-V* curve of an InAs/ALD-Al_2O_3 MOS capacitor (a) and simulated ideal *C-V* curve of InAs without interface states and charges (b).

$\times 10^{18}$ cm^{-3}, and $n_i = 1\times10^{15}$ cm^{-3} (Ref. 10) were used for InAs. The data were normalized to the accumulation capacitance. In Fig. 2(b), the accumulation capacitance is larger than the inversion capacitance because of the small InAs conduction band density of states, which results in a relatively thick electron inversion layer. The *C-V* curve simulated at 1 MHz frequency still exhibits low frequency *C-V* characteristics due to the high thermal generation rate in narrow band gap InAs. Comparing to the simulated the *C-V* curve, the measured device has a negative shift of the flat-band voltage and a much less steeper slope, which is mainly due to the interface states near the conduction band edge. It is known that these interface states invert the *p*-InAs surface to *n* type.[11] Very few reports of *C-V* characteristics on *p*-type InAs can be found in the literature.[8]

In order to make a MOSFET, source/drain dopant implantation and activation annealing are usually required. However, given the low thermal budget that is allowed for the current Al_2O_3–InAs interface, implantation activation annealing is precluded. Excess thermal treatment will cause interface and material damage, as described above. Therefore, an implantation-free MOSFET structure was used to study the transistor operation. The surface Fermi level of air exposed or metal-contacted InAs is pinned ~0.15 eV above its conduction band minimum.[11] As a result, there is always a strong inversion layer at the surface of *p*-type InAs. Utilizing this property of InAs, a simple MOSFET structure can be made on *p*-InAs without involving the source/drain doping process. The structure is shown in Fig. 3. After opening the dielectric window for source/drain contact, Ti–Au contact was directly deposited. As a result, the strong *n*-type inversion layer underneath the Ti–Au contact will form a quasi-Ohmic contact for electrons and a Schottky contact for holes. Furthermore, it is not necessary for the source/drain contacts to be self-aligned to the gate because any air exposed InAs surface will exhibit a strong inversion and hence form a low resistance path between the contact and the channel. A similar inversion channel may exist at the oxide-semiconductor

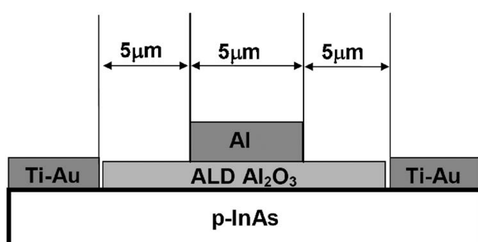

FIG. 3. Schematic layer structure of the large-feature size InAs/Al_2O_3 MOSFET.

interface [i.e., any region between the source (drain) contact and the gate metal, which is passivated by the Al_2O_3], depending on the interface charge density, charge in the oxide, and any fringing fields. At appropriate gate biases, an inversion electron channel can be formed beneath the gate dielectric, enabling current to flow from the source to the drain with little resistance. If the interface between InAs and Al_2O_3 is not pinned, a negative gate bias can be used to switch off the surface electron conduction channel and eventually achieve hole accumulation, as observed in the measured *C-V* results. Ideally, only electron current can be formed between the source and drain. The hole current flow from the source to the drain is blocked because the source and drain contacts (and the air exposed InAs) exhibit a barrier of about 0.5 V (0.35 eV InAs band gap +0.15 eV due to Fermi level pinning *inside* the conduction band) to hole transport.

I_d-V_d characteristics were measured for the fabricated MOSFETs, as shown in Fig. 4(a). It was found that the drain current I_d cannot be fully shut off. For gate biases (V_g) less than −5 V, I_d is independent of gate bias, indicating that I_d has two components: one is the channel current (I_{dc}) component that can be modulated by the gate bias and the other one is a leakage current (I_{dl}) component that is independent of gate bias. The value of the leakage current I_{dl} is equal to the I_d value at $V_g = -5$ V. In order to clearly look at the modulated channel current behavior, we subtracted the leakage current I_{dl} component from all measured I_d values. Figure 4(b) shows the modulated channel current $I_{dc} = (I_d - I_{dl})$ vs V_d characteristics after the subtraction. In this device, the gate electrode width is 5 μm and the distance between the source and drain is 15 μm. The device has a maximum channel current of ~3.5 mA/mm. The further increase of the drain current is limited by the source/drain resistance, whose values were extracted from the measurement of devices with different sizes. The specific contact resistivity between the source/drain metal and the electron inversion layer underneath was measured to be on the order of 10^{-4} Ω cm^2. The sheet resistance of the electron surface inversion layer between the source/drain metal and the gate metal was measured to be ~4 K$\Omega/\square$. Figure 4(c) shows the channel current $I_{dc} = (I_d - I_{dl})$ and transconductance as functions of the gate bias (V_g) for the InAs/Al_2O_3 MOSFET. The subthreshold swing is ~400 mV/decade. The possible reasons for the large subthreshold swing include large C_{it} (large interface-state density), small C_{ox} (thick dielectric layer), and large depletion layer capacitance C_d (small depletion layer thickness in narrow band gap InAs). The maximum transconductance is ~2.3 mS/mm.

Since the band gap of InAs is only 0.35 eV, both thermal generation and band-to-band tunneling can be major sources of leakage current. To experimentally characterize the leakage current, its temperature dependence was measured. Figure 4(d) shows the measured data in the form of log (I_{dl}) vs 1/kT. At small V_d and high temperatures, the leakage current exhibits an activation energy of ~0.1 eV, indicating a thermally activated current component. At high V_d and low temperatures, a temperature independent leakage current is observed, suggesting a tunneling mechanism. The higher the V_d, the more significant the tunneling component is. At room temperature, when $V_d > 0.2$ V, the leakage current is dominated by band-to-band tunneling.

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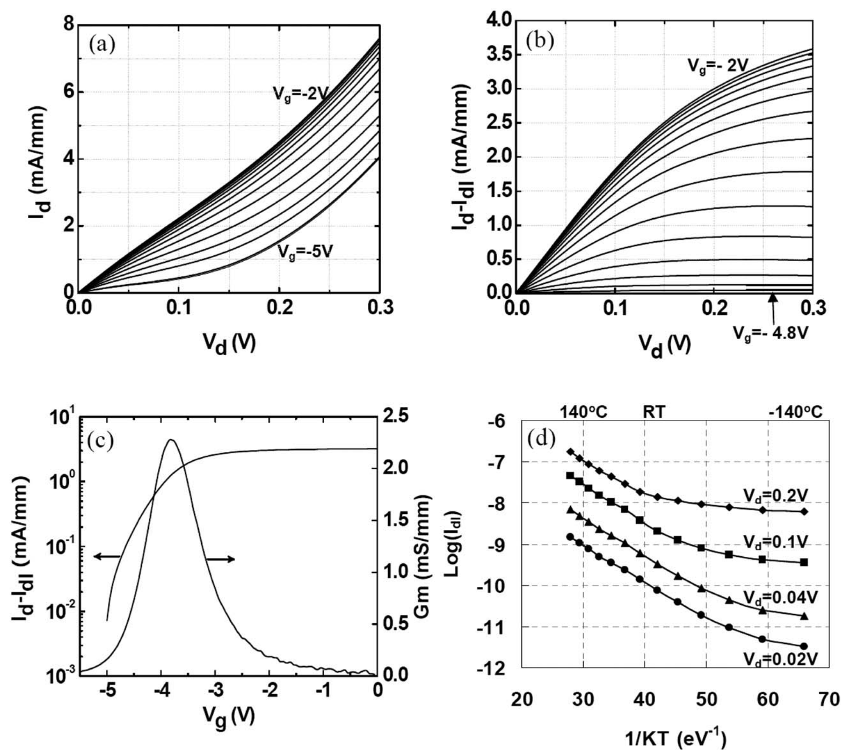

FIG. 4. Measured *I-V* characteristics of the fabricated InAs/Al_2O_3 MOSFET. Measured total drain current (I_d) vs drain bias (V_d) at gate voltage (V_g) steps of 0.2 V (a). Net channel current (I_d-I_{dl}) vs drain bias (V_d) at gate voltage (V_g) steps of 0.2 V (b). Net channel current (I_d-I_{dl}) and transconductance (G_m) vs gate bias (V_g) at V_d =0.2 V (c). Measured temperature dependence of the leakage current (I_{dl}) at different drain biases (V_d) (d).

Significantly higher performance can be expected for a self-aligned structure with aggressive scaling of channel length and dielectric thickness and by reducing the channel leakage. The unique Fermi level pinning properties of InAs are expected to enable implantation-free self-aligned MOSFETs to be achieved with submicron gate dimensions. Leakage can be reduced by using blocking layers (such as AlSb) beneath the channel,[12] heteroepitaxy on lattice mismatched substrates, or other suitable approaches. Although there is a lot that needs to be improved for InAs MOSFETs, InAs has the potential to provide better performance than InSb and InGaAs. While InSb has a higher mobility, InAs has a larger energy separation to satellite conduction band valleys. This is expected to facilitate larger saturated drift velocities and longer velocity overshoot range.[13] While InGaAs has a larger band gap, which may reduce the leakage current and allow higher temperature operation, alloy scattering and a reduced energy separation to satellite conduction band valleys may degrade performance[14] compared to pure InAs.

In summary, we have studied the interface properties and effects of processing conditions of InAs/ALD-Al_2O_3 MOS structures. MOS capacitor *I-V* and *C-V* characteristics were measured and analyzed. A simple large-area FET structure on the InAs bulk material was used to experimentally study the potential of InAs MOSFETs. A gate modulated channel current with a transconductance of ~2 mS/mm was demonstrated. The leakage current is attributed to tunneling at drain biases above a few tenths of a volt. The results and analysis indicate that the InAs–Al_2O_3 MOS system has the potential for high performance MOSFETs, although further optimization has to be demonstrated.

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