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Processing and Characterization of III–V Compound Semiconductor MOSFETs Using Atomic Layer Deposited Gate Dielectrics

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Summary. We demonstrate III–V compound semiconductor (GaAs, InGaAs, and GaN) based metal-oxide-semiconductor field-effect transistors (MOSFETs) with excellent performance using an Al_2O_3 high-permittivity (high-k) gate dielectric, deposited by atomic layer deposition (ALD). These MOSFET devices exhibit extremely low gate-leakage current, high transconductance, high dielectric breakdown strength, a high short-circuit current-gain cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}), as well as high output power and power added efficiency. ALD is a robust process that enables repeatability and manufacturability for compound semiconductor MOSFETs. In order to contribute to the fundamental understanding of ALD-grown high-k/III–V gate stack quality, we discuss stack and interface formation mechanisms in detail for Al_2O_3 and HfO_2 gate dielectrics on GaAs.

16.1 Introduction

GaAs-based metal-oxide semiconductor field-effect transistors (MOSFETs) have been a subject of study for several decades [1–18]. GaAs-based devices potentially have great advantages over Si-based devices for high-speed and high-power applications, in part from an electron mobility in GaAs that is $\sim 5\times$ greater than that in Si, the availability of semi-insulating GaAs substrates, and a higher breakdown field compared to Si. Currently, the GaAs metal-semiconductor field-effect-transistor (MESFET) or high-electron-mobility-transistor (HEMT) is the dominant device for high-speed and microwave-circuits. MESFETs or HEMTs feature gates formed by depositing metal directly on the semiconductor, forming metal-semiconductor (Schottky-barrier) junctions, while MOSFETs have oxide layers (higher barrier) between the metal gate and the semiconductor channel. Compared to GaAs MESFETs or HEMTs, GaAs MOSFETs feature a larger maximum drain current, much lower gate leakage current, a better noise margin, and much greater flexibility in digital IC design due to large gate voltage range.

The main obstacle to GaAs-based MOSFET devices has been the lack of high-quality, thermodynamically stable insulators on GaAs as the gate dielectric that can match device criteria similar to SiO_2 on Si. Both GaAs-based native oxides and deposited insulating layers have been attempted as gate dielectrics. For native oxidation of GaAs, various approaches were applied, i.e., wet oxidation, plasma oxidation, laser-assisted oxidation, vacuum ultraviolet photochemical oxidation, etc. These approaches have had limited success at the device level, however, mainly due to instability of the native oxides of GaAs, and due to the unacceptably high interface trap density D_{it} nearly universally observed with native and deposited oxides. Such interface defects give rise to Fermi level pinning. For example, Fermi level pinning upon GaAs oxidation has been attributed to oxygen-induced displacement of surface As atoms, where doubly O-coordinated second-layer Ga atoms give rise to gap states [19]. Excess interfacial As occupying As_{Ga} antisite defects causes gap states as well [19,20]. Interfacial As may be formed via decomposition of As_2O_3 in the vicinity of GaAs, resulting from the reaction: $As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As$ [21]. After decades of efforts on forming a deposited amorphous oxide on a III–V compound semiconductor using PECVD with decent interface quality [2], much progress has been made recently using in situ deposited $Ga_2O_3(Gd_2O_3)$ or Ga_2O_3 and Gd_2O_3 dielectrics using ultrahigh-vacuum multi-chamber molecular beam epitaxy (MBE) [22–28] and ex situ atomic layer deposition (ALD) grown Al_2O_3 on III–V semiconductors [29–35]. Both methods have been shown to provide a high-quality interface with a low D_{it} on GaAs. Fermi level unpinning in the Ga_2O_3/GaAs system is achieved through a Ga_2O/GaAs-like interface in which the Ga and As surface atoms are restored to near-bulk charge, preventing gap state formation [19]. Promising results have been demonstrated in GaAs MOSFETs using these techniques. Processing and properties of MBE-grown $Ga_2O_3(Gd_2O_3)$ gate dielectrics are addressed in detail in Chap. 3.4 by Kwo. Herein, we focus on ALD Al_2O_3. Another issue for GaAs circuits in competition with silicon is the large defect densities which also preclude large scale integration. The emerging strategy is to use III–V compound semiconductors as NMOS conduction channels and Ge as PMOS conduction channels, to replace part of traditional Si or strained Si, while integrating these high mobility materials with novel dielectrics and heterogeneously integrating them on Si or silicon-on-insulator (SOI).

In order to achieve higher transconductance as well as to downsize the device for higher integrated density, the reduction of the gate oxide thickness is critical, in particular for GaAs digital applications. A gate material with a much wider band-gap providing a higher potential barrier with GaAs is able to significantly reduce the gate leakage current for the same layer thickness of other materials. Al_2O_3 has a high bandgap of $\sim$9 eV, which is much higher than, e.g., for Ga_2O_3($\sim$2.45 eV) or Gd_2O_3($\sim$5.3 eV). As a high-k gate oxide on Si, Al_2O_3 has a dielectric constant of about 9, compared to 3.9 for SiO_2. Al_2O_3 also has a high bulk breakdown field (8–10 MV cm^{-1}), high thermal stability (up to at least 1,000°C), and remains amorphous under typical processing

conditions of interest. It is easily wet-etched yet is robust against interfacial reactions and moisture absorption (i.e., it is non-hygroscopic). ALD is a robust manufacturing process which is already commonly used for high-κ gate dielectrics in Si CMOS technology [36]. It is based on alternating, self-saturating surface reactions, e.g., using $Al(CH_3)_3$ and H_2O for Al_2O_3 growth. In this manner, sub-monolayer thickness control and excellent conformality even on high-aspect-ratio structures may be achieved. The enormous efforts and significant advent of deposited high-quality high-k dielectrics on Si using ALD has also renewed hopes that GaAs CMOS may finally become a reality.

In this chapter, we first focus on materials aspects, characterizing the structure and composition of Al_2O_3/GaAs (and, for comparison, HfO_2/GaAs) stacks fabricated by ALD, to develop an understanding of the impact of material and processing conditions on dielectric film and interface formation. Through electrical characterization of Al_2O_3/GaAs materials systems, e.g., leakage current density and capacitance–voltage (C–V) measurements, we then demonstrate a high bulk and interface quality of Al_2O_3 on GaAs. We further demonstrate GaAs-based MOSFETs with excellent performance using an ALD Al_2O_3 gate dielectric. These MOSFET devices exhibit negligible drain current drift and hysteresis, extremely low gate leakage, high transconductance, and good RF characteristics. Through transistor characteristics and modeling, such as drain current hysteresis and transconductance frequency dependence, we evaluate the interface trap density D_{it} of ALD grown Al_2O_3 on GaAs at the device level. InGaAs MOSFETs are also demonstrated using a similar approach. Finally, we extend our ALD work to wide bandgap semiconductor materials, e.g., GaN. We report on a GaN MOS-HEMT using ALD Al_2O_3 as the gate dielectric. Compared to a conventional GaN HEMT of similar design, the MOS-HEMT exhibits several orders of magnitude lower gate leakage and several times higher breakdown voltage and channel current. This implies that the ALD Al_2O_3/AlGaN interface is of high quality and the ALD Al_2O_3/AlGaN/GaN MOS-HEMT has good potential for high-power RF applications. In addition, the high-quality ALD Al_2O_3 gate dielectric enables an effective two-dimensional (2D) electron mobility at GaAs, InGaAs and GaN to be measured under a high transverse field. The resulting effective 2D electron mobility is much higher than the mobility in Si.

16.2 Materials Structure and Composition

In this section, we discuss structural and chemical aspects of ALD-grown high-k/GaAs gate stacks, as reported in detail in [32]. In particular, the high-k/III–V interface is critical since the presence and nature of a “native oxide” interfacial layer (containing, e.g., Ga_2O_3, As_2O_3, etc.) may impact the electrical quality of the stack and/or pose limits to capacitance scaling. We address two ALD-grown high-k materials frequently studied on Si: Al_2O_3 and HfO_2. Comparison of these materials helps develop an understanding of

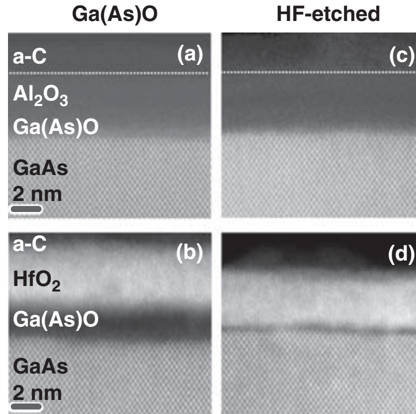

Fig. 16.1. Scanning transmission electron microscopy (STEM) images from 40 Å Al_2O_3 (*top*) and HfO_2 (*bottom*) deposited onto Ga(As)O-covered [(**a**) and (**b**)] and HF-etched [(**c**) and (**d**)] GaAs(100) (reproduced from [37] with permission)

the impact of materials properties on gate stack performance. We address successive stages of gate dielectric formation: starting surface, temperature ramp-up, ALD process, and anneal. Both Al_2O_3 and HfO_2 were grown on oxide-covered ("epi-ready") and HF-etched GaAs(100). For high-k dielectric growth, we followed a procedure that has yielded high-quality Al_2O_3/GaAs gate stacks [24–30]. All ALD work was carried out using commercial ASM Pulsar2000^{TM} or Pulsar3000^{TM} ALD reactors. Depositions were performed using alternating exposures of the common ALD precursors $Al(CH_3)_3 + H_2O$ or $HfCl_4 + H_2O$ in an N_2 carrier gas at 300°C. Carbon or aluminum served as cap layers for microscopy, and films were characterized by ex situ microscopies and spectroscopies [32].

The 20–25 Å thick epi-ready oxide on GaAs is porous and Ga-rich (As : Ga = 0.17) with an increased As concentration near the GaAs substrate [37]. In the following, we will denote this substrate "Ga(As)O/GaAs". During inert anneal to the ALD temperature of 300°C, the epi-ready oxide remains in place [37], consistent with the higher onset temperatures of reactions in various gallium/arsenic oxides on GaAs (300–430°C) [21,38,39]. HF-etched substrates, on the other hand, are mostly oxide-free [40]. Largely independent of surface preparation, as-deposited 40 Å thick ALD-grown Al_2O_3 and HfO_2 films are mostly amorphous as well as continuous (Fig. 16.1), despite a certain degree of high-k agglomeration during initial growth on HF-etched GaAs. This behavior is similar to what has been observed for HF-etched Ge [41].

Interfacial layer thickness after Al_2O_3 and HfO_2 deposition strongly depends on surface preparation. When native oxide removal by an initial HF wet etch is performed, both Al_2O_3 and HfO_2 deposition result in low interfacial layer thickness of only 3–8 Å (Figs. 16.1c,d). On Ga(As)O/GaAs, interfacial layer thickness is ∼10 and 20–25 Å, respectively (Figs. 16.1a,b). Clearly,

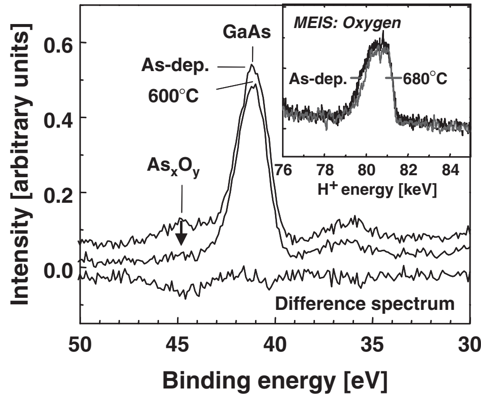

Fig. 16.2. X-ray photoelectron spectroscopy (XPS) data in the As 3d region from 40 Å Al_2O_3 deposited onto Ga(As)O/GaAs(100) before (*top*) and after (*center*) vacuum anneal to 600°C, and difference spectrum (*bottom*). Inset: MEIS spectra in the oxygen region before and after vacuum anneal to 680°C. (reproduced from [37] with permission)

the initial oxide is thinned during the Al_2O_3 ALD growth process, pointing to volatilization of Ga(As)O or its conversion into Al_2O_3. By contrast, the HfO_2 growth process does not cause interface thinning, even though the standard Gibbs energies of formation per O atom are nearly identical (Al_2O_3 : $-527\,\mathrm{kJ\,mol^{-1}}$; HfO_2 : $-544\,\mathrm{kJ\,mol^{-1}}$) and both higher than that for Ga and As oxides [21, 42]. The different degree of interface thinning likely is due to the much higher reactivity of $Al(CH_3)_3$ compared to $HfCl_4$, reflected in standard enthalpies of formation of $-74\,\mathrm{kJ\,mol^{-1}}$ and $-990\,\mathrm{kJ\,mol^{-1}}$, respectively [42, 43]. We note that a large variety of Al precursors is available, all with different enthalpies of formation. By extension, one may expect substantially different gate stack structures to be formed.

Finally, we show that thermal treatments critically impact interfacial layer thickness and composition. The interfacial layer remains Ga-rich during ALD growth, with As oxides still present in the case of Al_2O_3 on Ga(As)O/GaAs (XPS data in Fig. 16.2). During vacuum anneals at 600–680°C, the As oxides decompose (Fig. 16.2), and most oxygen is removed from the interfacial layer, as evidenced by medium energy ion scattering (MEIS, Fig. 16.2, inset). This thermal behavior may be rationalized by recalling results for oxidized GaAs surfaces (without a high-k layer) in inert ambients. At 300–460°C, mixed gallium/arsenic oxides are converted into pure gallium oxide with As precipitates according to the reaction $As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4$ As (with partial As desorption in the form of As_2 and As_4). At ~475°C, any Ga_2O present in the film desorbs; and at 580–630 °C, the remaining Ga_2O_3 is volatilized according to $Ga_2O_3 + 4GaAs \rightarrow 3Ga_2O \uparrow +4As \uparrow$. At similar temperatures, preferential As desorption from the GaAs substrate sets in. Assuming analogous reactions underneath the high-k layers, including facile out-diffusion of volatile species,

a ∼600°C anneal would thus result in (a) a Ga_2O_3-like interfacial layer which, upon continued heating, may be partially or completely removed, and (b) excess interfacial Ga. Our findings of As oxide decomposition and oxygen loss are consistent with this reaction scheme.

The role of the O_2 ambient during the ∼600°C anneal employed in the electrical studies presented in the following sections remains to be explained. TEM and electrical data indicate that no additional interfacial oxide grows. Therefore, the primary difference between oxidizing and reducing anneals may be the oxidation and desorption of excess interfacial Ga. In addition, O_2 may improve high-k quality, volatilizing As or Ga diffused into the layer and filling detrimental oxygen vacancies.

16.3 Electrical Characterization of ALD Al_2O_3 on GaAs

The starting materials were 2 in. Si-doped GaAs(100) wafers with a doping concentration of 6–8 $\times 10^{17}$ cm^{-3}. HF-etched substrates were employed, to ensure minimum Al_2O_3/GaAs interfacial layer thickness, as discussed in the preceding section. The wafers were transferred immediately to the ALD reactor. Again, Al_2O_3 layers were deposited at a substrate temperature of 300°C. An excess of each precursor was supplied alternatively to saturate the surface sites and ensure self-limiting film growth. An inherent characteristic benefit of ALD is the linear relationship between the number of growth cycles and the deposited thickness. In this way, once the growth rate is established for a particular process, the desired thickness can be accurately and reproducibly achieved by simply running a specific number of growth cycles. This feature enables extremely accurate thickness control, even for layers as thin as 10 Å or less. The 600°C O_2 anneals were performed ex situ in a rapid thermal annealing chamber following film deposition. A 1,000 Å thick Au film were deposited on the back side of GaAs wafers to reduce the contact resistance between GaAs wafers and the chuck of the measurement setup. Capacitors were fabricated using 3,000 Å Au top electrodes.

We measured the dependence of the leakage current density (J_L) on the gate voltage (V_g) for a set of ALD Al_2O_3 samples with the oxide thickness systematically reduced from 50 to 12 Å (Fig. 16.3). The plot shows a decrease in current density with increasing film thickness. Direct tunneling current is observed for film thickness ≤30 Å, while film with thickness ≥50 Å shows no significant direct tunneling. The 12 Å Al_2O_3 with the equivalent oxide thickness of only 4.7 Å still shows well-behaved direct tunneling characteristic and does not break down at ±3 V bias. Compared to state-of-the-art SiO_2 on Si, the leakage current density of Al_2O_3 on GaAs is one order of magnitude lower at same electrical thickness (gate stack capacitance). The GaAs/Al_2O_3 barrier height Φ_B is measured as high as ∼3.2 eV, which is higher than the Si/Al_2O_3 barrier height of 2.6–3.1 eV determined by the similar method [44].

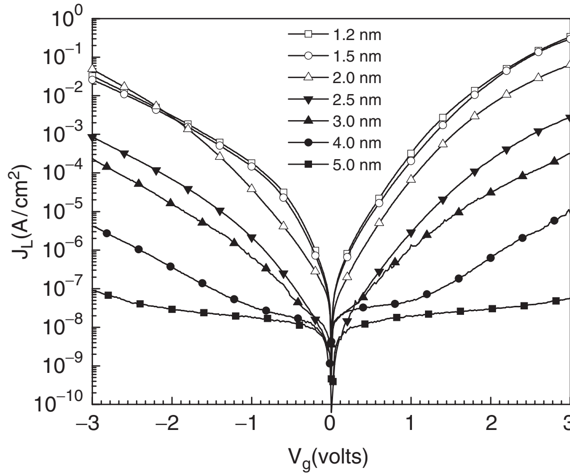

Fig. 16.3. Leakage current density J_L vs. gate bias V_g for ALD Al_2O_3 films on GaAs with different film thickness from 12 to 50 Å

Figure 16.4 shows the summary plot of E_{BR} vs. T_{ox} determined by various methods. The electrical properties of ALD Al_2O_3 films have been investigated by several research groups [44–51]. Most of these studies, however, were performed on $\sim$1,000 Å thick films grown on Si substrates. The E_{BR} of 10 MV cm^{-1} for ALD Al_2O_3 films with a thickness of 50–60 Å is consistent with typical E_{BR} values for high-quality, bulk Al_2O_3 of 8–10 MV cm^{-1}. A substantial E_{BR} enhancement is observed in Fig. 16.4 as the film thickness is reduced to below 40 Å. The E_{BR} for the 12 Å film is more than a factor of 3 larger than the bulk value. This could be explained by a remnant of

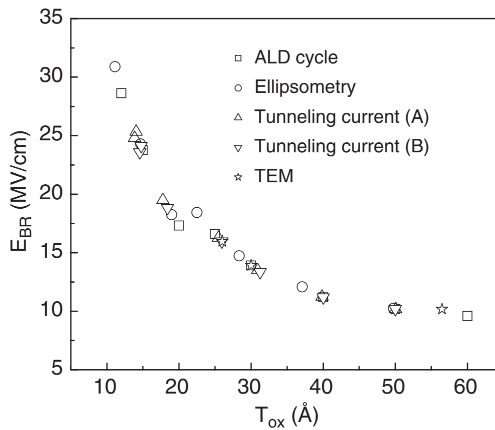

Fig. 16.4. Breakdown electric fields vs. thicknesses for ALD films. The different symbols represent thickness determination by different methods

the E_{BR} enhancement of ultrathin films, or possibly that the relative large leakage current density in an ultrathin oxide prevents the occurrence of hard breakdown of oxide film at a low electric field. The high breakdown field for ultrathin oxide on GaAs provides great opportunity for reducing the gate oxide thickness.

The typical high-frequency and low-frequency C–V curves for a capacitor with a 50 Å-thick ALD Al_2O_3 layer on n-type GaAs are shown in Fig. 16.5. This measurment is taken directly after film growth without any post annealing treatments. The high-frequency trace, e.g., 50 kHz, shows well-behaved depletion at negative bias and accumulation at positive bias. The low-frequency trace, e.g., 500 Hz, shows clear inversion (holes) at negative bias and accumulation at positive bias. There is a few hundred mV hysteresis in the C–V curves in reverse sweeping, depending on the surface preparation of GaAs before ALD growth. Another issue for C–V measurements on GaAs is the frequency dispersion in accumulation. Five to ten percent per decade frequency dispersion at accumulation capacitance is widely observed on unannealed GaAs MOS capacitors. Using a two frequency method of C–V measurement or the four-element equivalent circuit model for ultrathin oxides, [52] we estimate $D_{it} \sim 10^{12}\,cm^{-2}\,eV^{-1}$. This indicates that part of frequency dispersion may originate mostly from the parasitic resistance and capacitance of $10^{17}\,cm^{-3}$ doping levels in the GaAs substrates instead of suspected interface traps. The potential difference of the metal work function and n-GaAs affinity, the Schottky barrier height of the metal backgate on GaAs backside, and the existing hysteresis contribute to the flat-band shift on C–V curves (Fig. 16.5). A postannealing process at 600°C in oxygen ambient for 30–90 s, helps to reduce hysteresis and frequency dispersion and improves the D_{it} to low $\sim 10^{11}\,cm^{-2}\,eV^{-1}$. This is demonstrated in the following section.

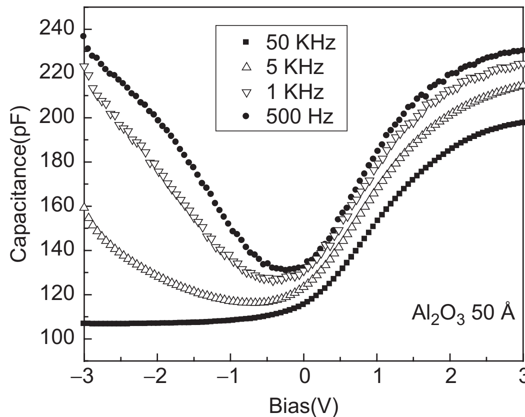

Fig. 16.5. C–V traces for a MOS diode with 50 Å Al_2O_3 on GaAs with an n-type doping of 4–6 × $10^{17}\,cm^{-3}$ at 500 Hz (low frequency), 1, 5 and 50 kHz (*high frequency*). The diameter of the measured diodes is ∼150 µm

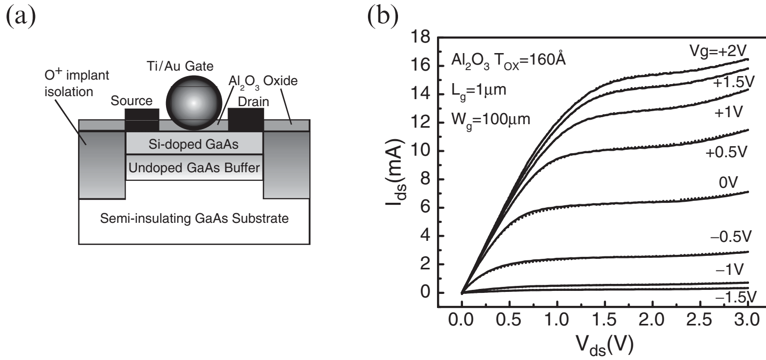

Fig. 16.6. (**a**) Schematic view of a depletion-mode n-channel GaAs MOSFET with ALD-grown Al_2O_3 as gate dielectric. (**b**) Drain current vs. drain bias in both forward (*solid lines*) and reverse (*dotted lines*) sweep directions as a function of gate bias. (reproduced from [30] with permission)

16.4 GaAs MOSFET Fabrication and Characterization

A schematic diagram of the depletion-mode GaAs device is shown in Fig. 16.6 (a). A 1,500 Å undoped GaAs buffer layer and a 700 Å Si-doped GaAs layer ($4 \times 10^{17}\,cm^{-3}$) were grown by MBE on a (100)-oriented semi-insulating 2-in. GaAs substrate. After the semiconductor epi-layer growth, the wafer was immediately transferred ex situ to an ASM Pulsar2000^{TM} ALD module. The GaAs MOSFET devices employed Al_2O_3 gate dielectrics of thickness ranging from 80 to 500 Å.

A postdeposition anneal was done at 600°C for 60 s in an oxygen ambient. Device isolation was achieved by oxygen implantation. Activation annealing was performed at 450°C in a helium gas ambient. Using a wet etch in diluted HF, the oxide on the source and drain regions was removed while the gate area was protected by photoresist. Ohmic contacts were formed by electron-beam deposition of Au/Ge/Au/Ni/Au and a lift-off process, followed by a 425°C anneal in a forming-gas ambient. Finally, conventional Ti/Au metals were e-beam evaporated, followed by lift-off to form the gate electrodes. The process requires four levels of lithography (alignment, isolation, ohmic and gate), all done using a contact printer. The source-to-gate and the drain-to-gate spacings are ~0.75 μm. The sheet resistance of the source/drain region outside the gate and its contact resistance are measured to be $1.3\,k\Omega\,sq^{-1}$. and $1.5\,\Omega\,mm$. The gate lengths of the measured devices are 0.65, 0.85, 1, 2, 4, 8, 20 and 40 μm.

Figure 16.6b shows the DC I–V curve of a MOSFET with a gate length L_g of 1 μm and a gate width W_g of 100 μm. The gate voltage is varied from −1.5 to + 2.0 V with 0.5 V step. The fabricated device has a pinch-off voltage of −1.5 V. The maximum drain current density I_{dss}, measured at positive bias

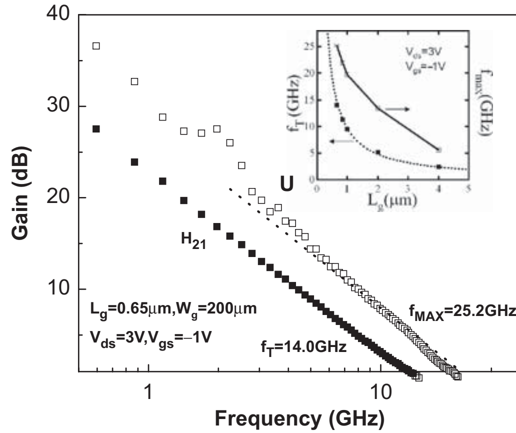

Fig. 16.7. RF characteristics of Al_2O_3/GaAs MOSFETs with gate length and width of 0.65 and 100 μm, respectively. Inset: f_T and f_{max} for different gate lengths. The *dashed line* illustrates the relation of $f_T = v_{sat}/2\pi L_g$. (reproduced from [29] with permission)

$V_{gs} = +2.0$ V, is ∼160 mA mm^{-1}. The knee voltage is ∼0.75 V at $V_{gs} = 0$ V, due to the relatively high series resistance arising from this non-self-aligned process. Under those conditions, the gate leakage current is less than 100 pA, corresponding to $< 10^{-4}$ A cm^{-2}, which is more than three orders of magnitude lower than for an equivalent MESFET under similar bias. Negligible I–V hysteresis is observed in the drain current in both forward and reverse gate-voltage sweep directions. This indicates that no significant mobile bulk oxide charge is present and that density of slow interface traps is low.

Figure 16.7 shows the short-circuit current-gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) measured by an S-parameter network analyzer. The device is biased at $V_{ds} = 3$ V and $V_{gs} = -1$ V. Under these conditions, the 0.65 μm gate length device shows $f_T = 14$ GHz and $f_{max} = 25$ GHz. These values are obtained by extrapolating the short-circuit current gain (H_{21}) and the unilateral power gain (U) curves, respectively, using −20 dB/decade slopes, as shown in Fig. 16.5. The inset of Fig. 16.2 illustrates the f_T and f_{max} as a function of gate length. As the trend shows, f_T and f_{max} can be significantly improved by reducing the gate length. The observed f_T vs. gate length is quite close to the theoretical relation of $f_T = v_{sat}/2\pi L_g$, where v_{sat} is ∼6×10^6 cm s^{-1}. The power-sweep characteristics is also measured at 900 MHz on a 200-μm-wide device under Class A bias of $V_{gs} = -0.5$ V and $V_{ds} = 5$ V. The linear power gain is close to 20 dB. The saturated output power is 13 dBm or 100 mW mm^{-1}. The maximum power-added efficiency (PAE) is over 45%. The PAE is quite encouraging and it has yet to reach a maximum. This is in contrast to the PAE of GaAs MESFETs that tends to peak shortly after gain compression then rolls off mainly due to gate leakage current.

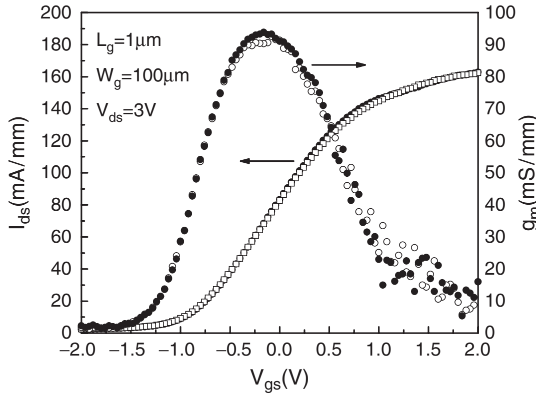

Fig. 16.8. Drain current vs. gate bias in both forward (*empty squares*) and reverse (*filled squares*) sweep directions. Circles are transconductances vs. gate bias at $V_{\mathrm{ds}} = 3\,\mathrm{V}$. (reproduced from [30] with permission)

Figure 16.8 illustrates the drain current as a function of gate bias in the saturation region. The slope of the drain current shows that the peak extrinsic transconductance (g_{m}) of the 1 μm gate length device is typically $\sim$100 mS mm^{-1}. It can be improved to $\sim$130 mS mm^{-1} by reducing the gate length to 0.65 μm. The theoretical intrinsic g_{m} in saturation regime can be estimated to be $\sim$280 mS mm^{-1} by $g_{\mathrm{m}} = v_{\mathrm{sat}} \cdot C_{\mathrm{ox}}$, where v_{sat} is $\sim 6 \times 10^6$ cm s^{-1}. Considering the series resistance of the device $R_{\mathrm{s}} \sim 2.5\Omega$ mm, the theoretical extrinsic g_{m} is $\sim$165 mS mm^{-1} which is $\sim$20% off from the measured peak g_{m} value. We ascribe this reduction of g_{m} to the existing interface traps and the reduction of mobility and saturation velocity at the interface. It is also possible to give a rough estimation of D_{it} using the hysteresis from I_{ds} vs. V_{gs} traces [30]. For ΔV_{gs} of 30 mV shown in Fig. 16.8, the estimated D_{it} is 6×10^{10}/cm^2-eV, which is at the lower side of the D_{it} evaluation. We ascribe the smaller hysteresis observed at the device level here, compared to C–V measurements described above, to the very small gate area and more leakage current in oxide after full device process.

Figure 16.9a shows the peak g_{m} as a function of frequency, measured from DC to several GHz, under typical operating conditions ($V_{\mathrm{ds}} = 3\,\mathrm{V}, V_{\mathrm{gs}} = -1\,\mathrm{V}$). The measurements are performed by three different experimental setups. The DC and RF (MHz–GHz) measurements are performed by a standard parameter analyzer and a microwave network analyzer, respectively. Data in the kHz range is obtained by a signal generator and a lock-in amplifier. It can be seen that the g_{m} remains essentially constant for frequencies above 20 Hz, indicating that efficient charge modulation in the channel can be achieved over the entire useful frequency range of the device. Furthermore, note that there is about a 20% decrease in g_{m} from 20 Hz down to DC. Figure 16.9b shows the model calculation based on all available device parameters. The y-axis is the maximum change of $g_{\mathrm{m}}(g_{\mathrm{m\ min}}/g_{\mathrm{m\ max}})$ between DC and GHz frequencies.

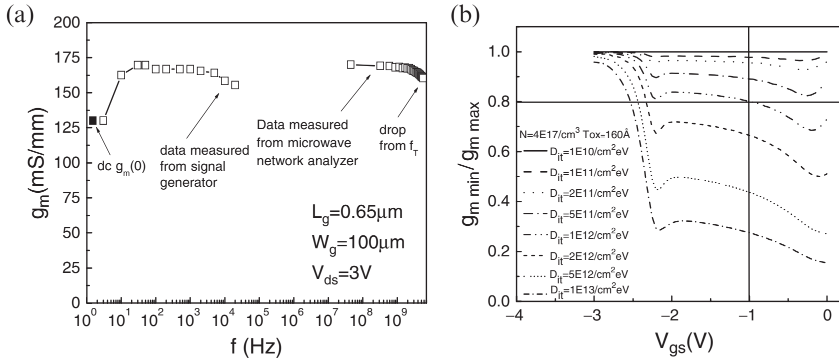

Fig. 16.9. (**a**) Peak transconductance g_m vs. frequency from DC to several GHz. The g_m is essentially constant for frequencies above 20 Hz. V_{gs} is biased at the peak g_m. (**b**) Model calculations of g_m due to the effects of D_{it}. Eighty percent of $g_{m\ min}\,g_{m\ max}^{-1}$ at $-2\,V < V_{gs} < 0\,\mathrm{V}$, as shown in (a), corresponds to D_{it} between 5×10^{11} to $10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$. $g_{m\ min}$ is g_m at DC and $g_{m\ max}$ is the maximum g_m at a few GHz before f_T in real devices. (reproduced from [30] with permission)

If the device has very low D_{it}, e.g., $1 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ as the solid line in Fig. 16.9(b), then g_m is almost constant. The maximum change of g_m is near zero and $g_{m\ min}/g_{m\ max}$ is 1. The model calculation of our devices in g_m gives an upper limit for D_{it} of $5 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$.

16.5 InGaAs MOSFET Fabrication and Characterization

InAs has a room temperature electron mobility as high as 20,000 $\mathrm{cm}^2\,\mathrm{Vs}^{-1}$. Although InAs layers can be formed on GaP or InP substrates, the technology is not mature for commercialization. InGaAs has a mobility between InAs and GaAs. InGaAs is widely used in compound semiconductors to improve the channel mobility, and thereby improve the device performance. $In_{0.53}Ga_{0.47}As$ layers, which are lattice-matched to InP, are used as electron channels for InP HEMTs. The strained thin layer of $In_{0.2}Ga_{0.8}As$ is widely used for pseudomorphic HEMTs (p-HEMTs). A depletion-mode n-channel $Al_2O_3/In_{0.2}Ga_{0.8}As/GaAs$ MOSFET was fabricated using a process similar to that described earlier in this chapter, on GaAs MOSFETs. A 1,500 Å undoped GaAs buffer layer, a 140 Å Si-doped GaAs layer ($2 \times 10^{18}\,\mathrm{cm}^{-3}$), and a 135 Å Si-doped $In_{0.2}Ga_{0.8}As$ layer ($1 \times 10^{18}\,\mathrm{cm}^{-3}$) were subsequently grown by MBE on a (100)-oriented semi-insulating 2-in. GaAs substrate. Figure 16.10 shows the DC I–V curve of an InGaAs MOSFET with a gate length L_g of 1 μm and a gate width W_g of 100 μm. The gate voltage was varied from -4.0 to +3.0 V with 1.0 V steps. Figure 16.10 has 1.0V steps for the gate voltage. The fabricated device has a pinch-off voltage of −4.0 V. The maximum drain current density I_{dss}, measured at positive bias $V_{gs} = +3.0\,\mathrm{V}$, is ∼330 mA mm^{-1}.

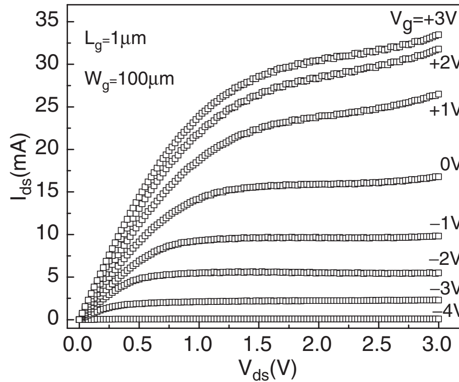

Fig. 16.10. Drain current vs. drain bias as a function of gate bias (reproduced from [33] with permission)

The knee voltage is ∼1.0 V at $V_{gs} = 0$ V, due to the relatively high series resistance arising from this non-self-aligned process. Under those conditions, the gate leakage current is less than 100 pA, corresponding to $<10^{-4}$ A cm^{-2}. Much more accumulation current (∼200 mA mm^{-1}) is observed in InGaAs MOSFET at positive gate bias, compared to GaAs MOSFET. It might indicate a better interface on InGaAs or the D_{it} at conduction band edge of $Al_2O_3/In_{0.2}Ga_{0.8}As$ is better than that at Al_2O_3/GaAs. Since there is no Schottky barrier between metal-InGaAs or metal-InAs, the MOS structure discussed here could be the only way to realize InGaAs or InAs MOSFETs.

16.6 GaN MOS-HEMT Fabrication and Characterization

One of the major factors that limit the performance and reliability of GaN HEMTs for high-power radio-frequency (RF) applications is their relatively high gate leakage. The gate leakage reduces the breakdown voltage and the power-added efficiency while increasing the noise figure. To help solve the problem, significant progress has been made on MIS-HEMTs and MOS-HEMTs using SiO_2 [53–57], Si_3N_4 [58, 59], Al_2O_3 [60, 61] (formed by electron cyclotron resonance plasma oxidation of Al), and other oxides [62]. However these gate dielectrics and their associated processes may not be readily scalable for low-cost and high-yield manufacture. The thickness control of the ALD films, and thus scalability, is much superior than those of the plasma-enhanced-chemical-vapor-deposition (PECVD) grown SiO_2 and Si_3N_4. The quality of the ALD Al_2O_3 is also much higher than those deposited by other methods, i.e., sputtering and electron-beam deposition, in terms of uniformity, defect density and stoichiometric ratio of the films.

ALD Al_2O_3/AlGaN/GaN MOS-HEMT process is similar with the device process we discussed above. A 40 nm undoped AlN buffer layer, a 3 μm

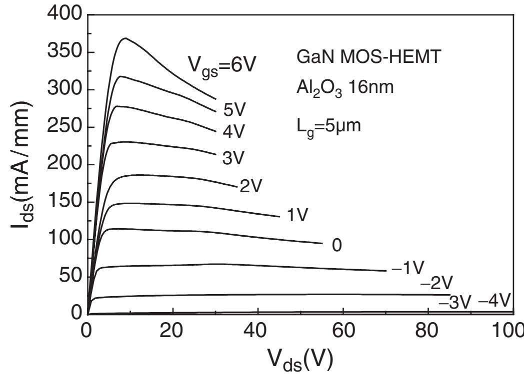

Fig. 16.11. Measured *I–V* characteristics of a GaN MOS-HEMT using ALD Al_2O_3. The negative output conductance under high gate biases ($V_{gs} \geq 0$) is due to self heating. (reproduced from [34] with permission)

undoped GaN layer, and a 30 nm undoped $Al_{0.2}Ga_{0.8}N$ layer were sequentially grown by metal-organic chemical vapor deposition on a 2-in. sapphire substrate. A 16 nm thick Al_2O_3 layer was deposited at 300°C then followed by annealing at 600°C for 60 s in oxygen ambient. Device isolation was achieved by nitrogen implantation. Using a wet etch in diluted HF, the oxide on the source and drain regions was removed while the gate region was protected by photoresist. Ohmic contacts were formed by electron-beam deposition of Ti/Al/Ni/Au and a lift-off process, followed by an 850°C anneal in a nitrogen ambient, which also activated the previously implanted nitrogen. Finally, Ni/Au metals were e-beam evaporated and lifted off to form the gate electrodes.

Figure 16.11 shows that the *I–V* characteristics of the MOS-HEMT are well behaved over a drain bias V_{ds} of 0–100 V and a gate bias V_{gs} of −4 to 6 V. The pinch-off voltage is consistently −4 V. The maximum drain current density I_{ds}/W_g at $V_{gs} = 6$ V is approximately 375 mA mm^{-1}. The off-state three-terminal breakdown voltage is approximately 145 V. The results indicate that ALD Al_2O_3 is an effective gate dielectric for AlGaN/GaN devices. Our devices have no widely observed abnormal *I–V* characteristics at positive gate biases, i.e., PECVD grown SiO_2 GaN MOS-HEMTs [48], which are mostly related with the bulk traps in PECVD grown dielectrics or interface traps at insulating films on GaN.

Figures 16.12a,b illustrate the saturated ($V_{ds} = 10$ V) drain current density and intrinsic transconductance g_m as a function of gate bias for both the MOS-HEMT and the HEMT. The drain current density of the HEMT is limited to 190 mA mm^{-1} at $V_{gs} = 2$ V. By contrast, the drain current density of the MOS-HEMT is 450 mA mm^{-1} at $V_{gs} = 8$ V and can be further increased under higher V_{gs}. The combination of higher breakdown voltage and higher drain current imply that the output power of the MOS-HEMT can be much higher than that of the HEMT. Using $I_{ds}/W_g = e\,n_s\,\upsilon_{sat} = 450$ mA mm^{-1} and a saturated velocity $\upsilon_{sat} = 5 \times 10^6$ cm s^{-1}, the sheet carrier density

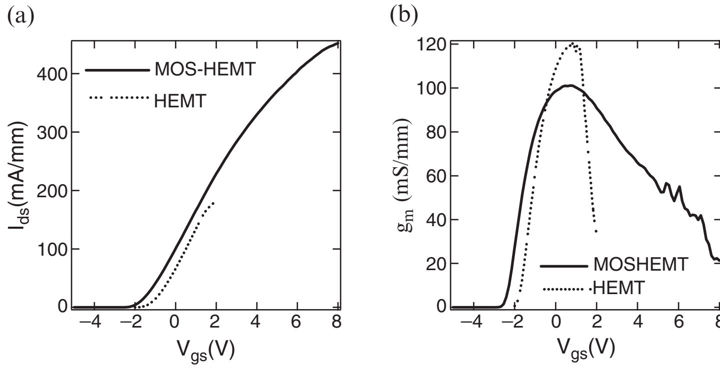

Fig. 16.12. Measured (**a**) transfer and (**b**) transconductance characteristics measured with the MOS-HEMT (*solid line*) and HEMT (*dashed line*) in saturation ($V_{ds} = 10\,V$). (reproduced from [34] with permission)

n_s is estimated to be $6 \times 10^{12}\,cm^{-2}$, which is within the range of values commonly observed for the heterojunction between undoped $Al_{0.2}Ga_{0.8}N$ and GaN. Figure 16.12b shows that the peak g_m is 100 and $120\,mS\,mm^{-1}$ for the MOS-HEMT and the HEMT, respectively. The g_m was calculated from the measured extrinsic transconductance by accounting for the parasitic source resistance R_s of 5.4 and $5.9\,\Omega\,mm$ for the MOS-HEMT and the HEMT, respectively. The R_s values were measured on test structures fabricated alongside the MOS-HEMT and the HEMT according to the transmission line method (TLM). These g_m values are in agreement with theoretical estimates according to $g_m = v_{sat} \cdot C_{MOS-HEMT}$ or $g_m = v_{sat} \cdot C_{HEMT}$. Using $v_{sat} = 5 \times 10^6\,cm\,s^{-1}$, $C_{MOS-HEMT} = 16\,pF$, and $C_{HEMT} = 21\,pF, g_m$ was estimated to be 102 and $133\,mS\,mm^{-1}$ for the MOS-HEMT and the HEMT, respectively. The sheet resistances measured on TLM test structures are 700 and $950\,\Omega\,sq.^{-1}$ for the MOS-HEMT and the HEMT, respectively.

The present Al_2O_3/AlGaN/GaN heterojunction enables us to measure the effective 2D electron mobility μ_{eff} at the AlGaN/GaN heterojunction under high electron density and high transverse field as shown in Fig. 16.13. The 2D electron mobility is governed by Coulomb scattering and phonon scattering under low transverse field. It is dominated by interface roughness scattering and phonon scattering under strong accumulation. The resulting mobility of $1{,}200\,cm^2\,Vs^{-1}$ under low transverse fields is consistent with the value obtained from the Hall measurement. The mobility of $640\,cm^2\,V\,s^{-1}$ under a high transverse field of $0.6\,MV\,cm^{-1}$ is much higher than $400\,cm^2\,V\,s^{-1}$, the universal mobility of Si MOSFETs under the same field. It is also higher than the surface mobility of GaAs or InGaAs MOSFETs we observed earlier. Such an improvement can be attributed to the higher quality of the AlGaN/GaN semiconductor–semiconductor interface than that of the oxide–semiconductor interfaces. The details how to obtain the μ_{eff} vs. E_{eff} are described in [33] and [34].

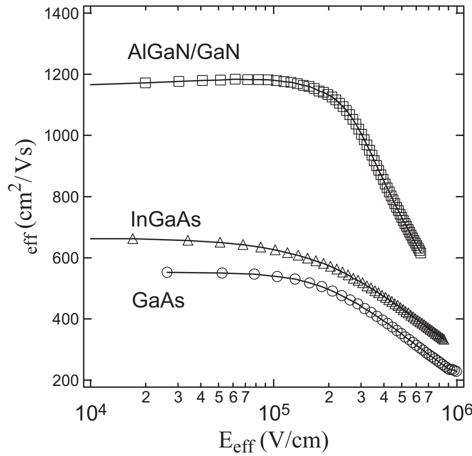

Fig. 16.13. Calculated effective 2D electron mobility vs. effective electric field at the AlGaN/GaN (*squares*), Al_2O_3/InGaAs (*triangles*), and Al_2O_3/GaAs (*circles*) interfaces. (reproduced from [34] with permission)

To study the passivation effect of ALD Al_2O_3 on AlGaN, we measure the sheet resistances of AlGaN/GaN with and without ALD Al_2O_3 on top. The lack of Al_2O_3 passivation at drain-gate and source-gate regions for the baseline HEMT could lead to increased parasitic resistance, thus degrades intrinsic g_m. The parasite resistance is determined from the transmission line model (TLM) method fabricated on the same chip. The sheet resistance measured from TLM for MOS-HEMT with ALD Al_2O_3 passivation is $\sim 700\,\Omega\,\text{sq.}^{-1}$ and for HEMTs without any passivation is $\sim 950\,\Omega\,\text{sq.}^{-1}$, which indicates the effectiveness of the ALD Al_2O_3 passivation on AlGaN. The pulsed drain characteristics also show interesting results. For example, after up to 80 V drain voltage stress, DC drain characteristics (solid lines in Fig. 16.14) show the well-known current collapse effect on drain current at $V_{ds} < 15$ V. It is mainly due to hot carrier injections at the oxide/semiconductor interface or even in the bulk oxide at the drain side under high voltage drain stress. The dashed lines in Fig. 16.14 shows that the short pulse (1μs) drain characteristics are fully recovered from DC characteristics at $V_{gs} = 4$ V quiescent conditions. The short pulse drain measurements at different quiescent points could be an effective method to study Al_2O_3 surface passivation. More device evaluation in terms of CW and pulsed, small- and large-signal characteristics is in progress.

16.7 Conclusions

We have reviewed the properties and performance of ALD-grown Al_2O_3 gate dielectrics for III–V compound semiconductor (GaAs, InGaAs, and GaN) based MOSFETs. Continuous, amorphous Al_2O_3 layers with low leakage

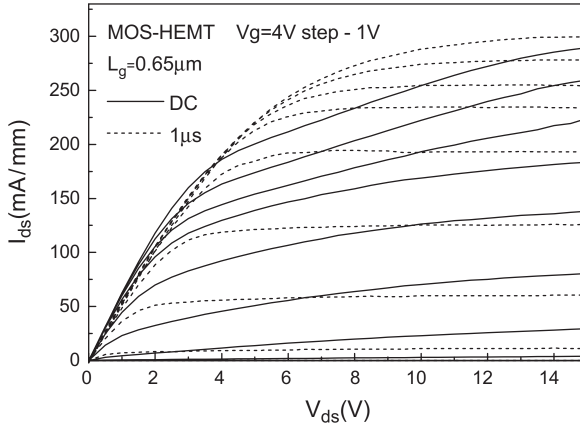

Fig. 16.14. Output *I–V* characteristics of MOS-HEMT under DC (*solid line*) and 1 μs pulsed-gate bias (*dashed line*). The pulse width is 1 μs with 10% duty cycle

current and high breakdown strength may be grown by ALD. Through a combination of surface preparation (e.g., HF etching), choice of a reactive ALD precursor, and thermal processing at ∼600°C, Al_2O_3/GaAs stacks with low interfacial layer thickness can be fabricated. For GaAs MOSFET, submicron gate-length devices exhibit an extrinsic transconductance up to 130 mS mm^{-1}, with negligible *I–V* hysteresis and a gate leakage current density less than 10^{-4} A cm^{-2}. The RF characteristics of an 0.65 μm gate-length device shows an f_T of 14 GHz and an f_{max} of 25 GHz. Through the drain current hysteresis, we obtain 6×10^{10} cm^{-2} eV^{-1} as the lower limit of the interface trap density (D_{it}) of Al_2O_3/GaAs. The upper limit of D_{it} of $5 \times 10^{11}/cm^2$ eV is obtained by transconductance vs. frequency measurements and modeling. InGaAs MOSFET shows a stronger accumulation current, indicating a better interface between Al_2O_3 and InGaAs. ALD Al_2O_3 process also provides high-quality gate dielectric and surface passivation for AlGaN/GaN HEMTs. The resulted MOS-HEMT shows favorable characteristics when compared to MOS-HEMTs with other gate insulators. These results suggest new opportunities for providing processing alternatives, including high-κ gate dielectrics and passivation layers, by ALD for III–V semiconductor devices.

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