Atomic-layer-deposited $LaAlO_3/SrTiO_3$ all oxide field-effect transistors

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Abstract

We have demonstrated well-behaved accumulation-mode all oxide NMOSFETs with amorphous atomic-layer-deposited (ALD) $LaAlO_3$ gate dielectric stacks on crystalline $SrTiO_3$ substrates. A maximum drain current exceeding 10 mA/mm has been obtained on a 3.75μm-gate-length device, proving a very conductive channel can be formed at the oxide-oxide interface. Four different gate dielectric stacks, which are La-first cycle $LaAlO_3$, Al-first cycle $LaAlO_3$, $LaAlO_3$ with 1.5 nm La_2O_3 interfacial layer, and $LaAlO_3$ with 1.8 nm Al_2O_3 interfacial layer, have been deposited on $SrTiO_3$ substrates to systematically study their effects on the conductivity at the different oxide-oxide interfaces. The experimental results show that a La-initiated interfacial layer is preferable to form a more conducting channel at the $LaAlO_3/SrTiO_3$ interface. Low temperature characteristics have also been utilized to provide an in-depth understanding of the channel formation at the oxide-oxide interface. The availability of the MBE technology to epitaxially grow $SrTiO_3$ on Si substrate provides the pathway to integrate ALD $LaAlO_3/SrTiO_3$ devices on Si platform.

Introduction

The class of transition metal oxide compounds exhibit a broad range of functional properties, such as high dielectric permittivity, piezoelectricity and ferroelectricity, superconductivity, spin polarized current, colossal magnetoresistance and ferromagnetism. Almost all these phenomenon result from strongly correlated electronic behavior and turned out to be very sensitive to external parameters such as electromagnetic fields and internal or external pressure. Polarity discontinuities at the hetero-interfaces between two different crystalline materials are believed to play a key role in leading to nontrivial effects. In 2004, Ohtomo and Hwang reported a high-mobility electron gas could be formed at the crystalline $LaAlO_3/SrTiO_3$ hetero-interface with the materials grown at ultra-high vacuum and by pulsed laser deposition technique (PLD) [1,2]. For a very long time, it was widely believed that the oxide-oxide interface needs to be atomically engineered by hetero-epitaxial growth in order to achieve a conducting channel. Later, some research groups reported that the conducting channel can be realized on $SrTiO_3$ with some PLD amorphous dielectrics formed under high temperature and high vacuum conditions [3-6]. In this paper, we demonstrate *for the first time* that the conducting channel can also be formed at an *insulating* amorphous $LaAlO_3$/*insulating* crystalline $SrTiO_3$ (100) interface by a low temperature (300°C) and low vacuum (0.35Torr) atomic-layer-deposition technique. Well-behaved $LaAlO_3/SrTiO_3$ all oxide field-effect transistors (FETs) are realized with gate dielectric stacks of La-first cycle $LaAlO_3$, Al-first cycle $LaAlO_3$, $LaAlO_3$ with a nanometer thin La_2O_3 interfacial layer, and $LaAlO_3$ with a nanometer thin Al_2O_3 interfacial layer. High resolution transmission electron microscopy (HRTEM) and temperature dependent MOSFET characterization are used to systematically study the $LaAlO_3/SrTiO_3$ interface.

Experiments

Fig. 1 and Table 1 show the schematic cross section of an accumulation-mode $LaAlO_3/SrTiO_3$ MOSFET and the device fabrication flow. A simple surface degrease using acetone, methanol and isopropanol was performed on the one-inch $SrTiO_3$ substrate. After a deionized water rinse, wafers were transferred via room ambient into ALD reaction chamber for gate stack deposition. For a systematical interface study, four kinds of high-k gate dielectric stacks were grown on insulating Ti-terminated $SrTiO_3$ substrates. These gate stacks are as follows: La-first cycle 8 nm $LaAlO_3$, Al-first cycle 8 nm $LaAlO_3$, 8 nm $LaAlO_3$ with 1.5 nm La_2O_3 interfacial layer, and 8 nm $LaAlO_3$ with 1.8 nm Al_2O_3 interfacial layer. Reactions of $La[N(SiMe_3)_2]_3$ + H_2O and TMA + H_2O at 300°C were employed for the dielectric deposition. La-first cycle/Al-first cycle refers to using $La[N(SiMe_3)_2]_3$/TMA as the first pulse into the reaction chamber during the ALD process. After the gate dielectric stacks, a layer of Al_2O_3 was immediately deposited as an encapsulation layer on top to prevent water adsorption of $LaAlO_3$ film [7]. After S/D patterning by photolithography, diluted BOE solution (BOE : H_2O ~ 5 : 1) was used to first remove the Al_2O_3 capping layer which was followed by an Argon milling in a Plasma Technology RIE 80 system for 6-10 minutes. During the milling process, over etching was necessary to create shallow trenches on $SrTiO_3$ surface where oxygen vacancies were generated and acted as donors to help to achieve good ohmic contacts on the $SrTiO_3$ surface at the source and drain regions. Ti/Au was deposited as S/D metal by e-beam evaporation and a lift-off process was followed. Finally, the gate electrode was made by e-beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 3.5 μm to 42.75 μm and a gate width of 100 μm. A Keithley 4200 was used to measure the MOSFETs' output characteristics at room temperature, and a Janis 22C/350C Cryodyne Refrigerator system along with a Keithley 2612A SYSTEM source meter were used for low temperature measurement.

Results and discussion

The HRTEM image in Fig.2 shows an amorphous layer of $LaAlO_3$ and a very abrupt $LaAlO_3/SrTiO_3$ interface. A well-behaved I-V characteristic of a 6.75 μm-gate-length accumulation-mode $SrTiO_3$ NMOSFET with ALD high-k dielectric of La-first $LaAlO_3$ is demonstrated in Fig. 3 with a maximum drain current of 8.5 mA/mm and gate leakage less than 10^{-6} A/cm^2. Fig. 4 illustrates the transfer characteristics of this $LaAlO_3/SrTiO_3$ NMOSFET, showing the on-off ratio (I_{on}/I_{off}) of ~ 1000 which is much smaller than that reported in [3]. This low I_{on}/I_{off} ratio is due to the lack of device isolation instead of the intrinsic property of this novel material system. Similar results are also obtained on the devices with a gate dielectric of Al-first $LaAlO_3$. In order to study the importance of atomic structures at the interfaces, the total resistance in mobility region vs. different gate length at different gate biases on La-first and Al-first devices are plotted in Fig. 5 and Fig. 6, respectively. It can be seen that the sheet resistance for the La-first interface at zero bias is 140 kΩ/sq. while it is 280 kΩ/sq. for the Al-first interface. This observation is consistent with the discovery reported in [1,2,8,9], where the 2DEG formation is closely related with the La involved interface structures. The extrinsic peak transconductance G_m at V_{ds}=5V is 2.1 mS/mm and an intrinsic value of 2.8 mS/mm can be obtained after subtracting the contact resistance R_{SD}. The less resistive channel at La-first $LaAlO_3/SrTiO_3$ interface than Al-first $LaAlO_3/SrTiO_3$ interface is also supported by Fig. 7, where the field-effect mobility of La-first interface (with peak mobility of ~3.9 cm^2/Vs) is higher than that of Al-first interface (with peak mobility of ~3.3 cm^2/Vs).

In order to further verify the importance of atomic structures at the interfaces, we deliberately designed two gate stack structures with 1.5 nm La_2O_3 and 1.8 nm Al_2O_3 as the interfacial layer between 8nm $LaAlO_3$ and $SrTiO_3$ substrates. Similarly, well-behaved I-V characteristics are also obtained on these devices. As shown in Fig. 8, a 3.75μm-gate-length device with 1.5 nm La_2O_3 interfacial layer has a drain current of 10 mA/mm. Fig. 9 and Fig. 10 show the similar approach to probe the sheet resistance of different interfacial layers with 320 kΩ/sq. for La_2O_3 and 800 kΩ/sq. for Al_2O_3. The result reconfirms the importance of the atomic structure of La-Ti on $SrTiO_3$ surface to achieve a more conductive channel. Fig. 11 shows the maximum drain current vs. different gate length on the two types of MOSFETs with a reasonable scaling behavior. A more pronounced difference in terms of field-effect mobility can be observed in Fig. 12. As mentioned above, La-Ti atomic structure plays a key role to form a better conducting channel at $LaAlO_3/SrTiO_3$ interface, thus explaining the more obvious difference in terms of mobility than the case between La-first and Al-first as shown in Fig. 7. With different gate lengths, a field effect mobility μ_{FE} ~ 4 cm^2/Vs can be obtained on the devices with 1.5 nm La_2O_3 interfacial layer, while ~ 2.5 cm^2/Vs with 1.8 nm Al_2O_3 interfacial layer. All the data are peak values of field-effect mobility extracted from different gate-length device transfer characteristics in linear region.

Fig. 13 shows the maximum drain current (I_{DSS}) and on-off ratio (I_{on}/I_{off}) vs. measured temperature from 300K down to 25K. The increase of maximum drain current is expected, because electron-phonon scattering should be suppressed with decreasing temperature thus increasing the mobility [10]. The dramatic increase of I_{on}/I_{off} ratio from 10^3 to 10^7 provides an insight into the possible origin of the electron carriers at the $LaAlO_3/SrTiO_3$ interface. I_{off} is dominated by the fringe current between source/drain beyond gate controlled area due to the lack of device isolation. The four orders of magnitude decrease indicates that the intrinsic carriers are "frozen" out at low temperatures. The majority carriers in the channel originated from electrostatic doping or the field-effect. The intrinsic carriers at zero bias could be caused by a combination of the crystal-field effect, pseudo-Jahn-Teller distortion, and interface chemistry. Another possibility is from charge transfer from the wider bandgap oxide into the adjacent narrower gap $SrTiO_3$ layer [11].This charge transfer, similar to modulation-doping in III-V semiconductors, could be significantly suppressed at low temperature. The field-effect mobility vs. temperature for devices with La_2O_3 and Al_2O_3 interface layers are plotted in Fig. 14. High voltage output performance is characterized (seen in Fig. 15) to demonstrate the potential of this novel material system for all-oxide FETs with applications in transparent power amplifier/switch area due to its wide bandgap (3.2eV for $SrTiO_3$). A picture of epitaxial single crystalline $SrTiO_3$ film on 300mm Si wafer is also shown in Fig. 16, which demonstrates great potential to integrate the all-oxide FET technology into Si process platform with the availability of ALD technology on 300mm Si process.

Conclusion

We have found a conducting channel at *insulating* ALD amorphous $LaAlO_3$/*insulating* crystalline $SrTiO_3$ interface and demonstrated well-behaved $LaAlO_3/SrTiO_3$ N-channel MOSFETs. The maximum drain current can exceed 10 mA/mm for a 3.75μm-gate-length device with La_2O_3 interfacial layer at V_{gs} = 5V. Four different gate dielectric stacks are designed to investigate the effect of atomic structures at the interfaces on the channel conductivity, showing that La-Ti interface is preferable for a more conductive channel. With the availability of MBE $SrTiO_3$ and ALD $LaAlO_3$ on 300 mm Si substrates, these all-oxide field-effect transistors have the a path for integration onto the state-of-the-art Si technology platform.

References

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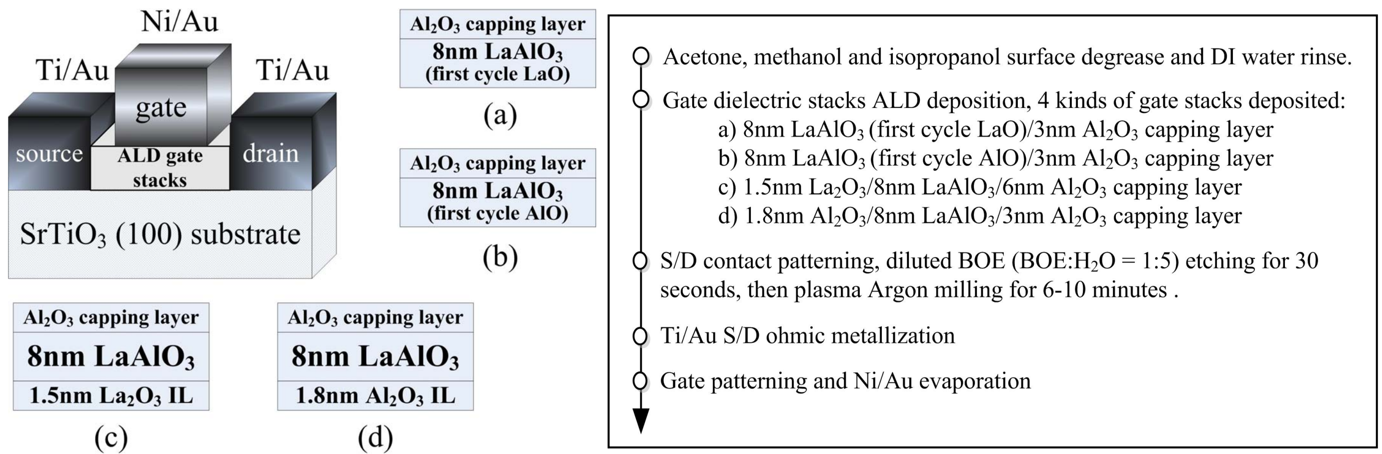

Fig. 1 Schematic view of an accumulation-mode NMOSFET on Ti-terminated $SrTiO_3$ substrate with four types of ALD $LaAlO_3$ gate stacks.

Table 1 Process flow for $SrTiO_3$ NMOSFETs with ALD high-k dielectric. four types of $LaAlO_3$ gate stacks were employed. Plasma argon milling removes $LaAlO_3$ at S/D regions and also generates O vacancies on $SrTiO_3$ surface to ensure Ti/Au Ohmic contacts to the conducting channel.

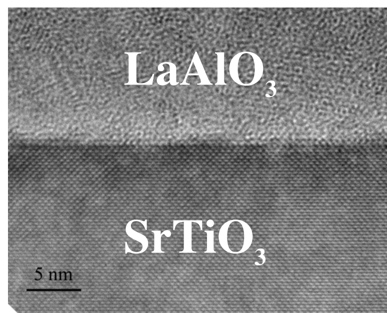

Fig. 2 Cross-section HRTEM image of ALD $LaAlO_3/SrTiO_3$ interface. A sharp and clean interface is obtained.

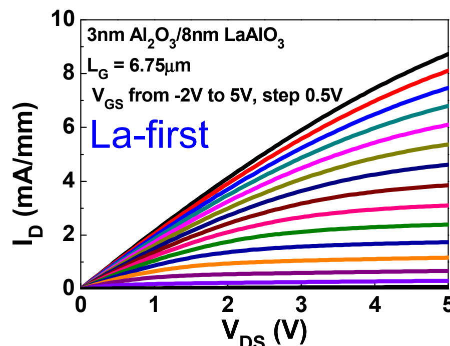

Fig. 3 The output characteristics of a $SrTiO_3$ MOSFET with La-first cycle $LaAlO_3$ as gate dielectric. The gate length of the device is 6.75 μm.

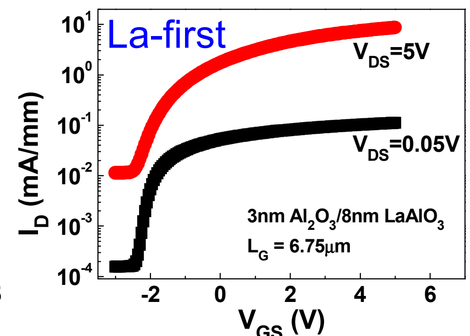

Fig. 4 The transfer characteristics of the same device in Fig.3. The I_{on}/I_{off} ratio is ~ 1000 due to the lack of the device isolation in the current fabrication process.

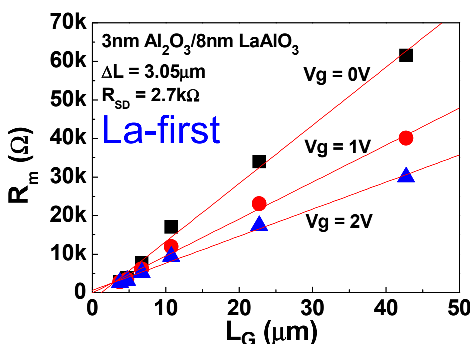

Fig. 5 Channel resistance (R_m) versus designed gate length (L_G) under different gate bias in the linear region on La-first $SrTiO_3$ MOSFETs. The S/D series resistance (R_{SD}) and effective gate length can be obtained at the cross point. La-first interface shows a sheet resistance of ~ 140 kΩ/sq. at zero bias.

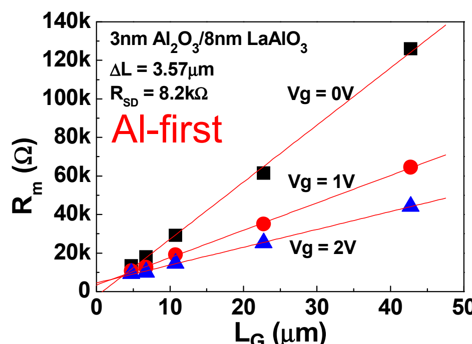

Fig. 6 Channel resistance (R_m) versus designed gate length (L_G) under different gate bias in the linear region on Al-first $SrTiO_3$ MOSFETs. The S/D series resistance (R_{SD}) and effective gate length can be obtained at the cross point. La-first interface shows a sheet resistance of ~ 280 kΩ/sq. at zero bias.

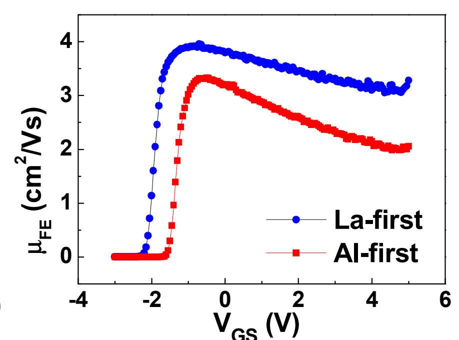

Fig. 7 Comparison of field-effect mobility of La-first and Al-first $LaAlO_3/SrTiO_3$ MOSFETs, showing La-first interface has higher mobility than Al-first interface.

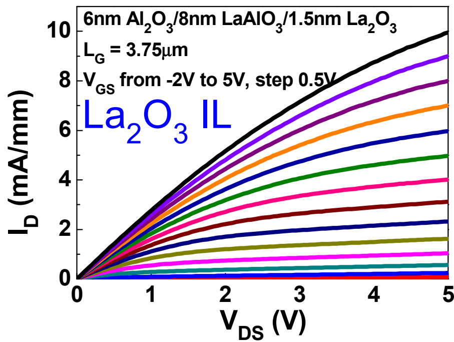

Fig. 8 The output characteristics of a $SrTiO_3$ MOSFET with 1.5 nm La_2O_3 as interfacial layer. The gate length of the device is 3.75 µm.

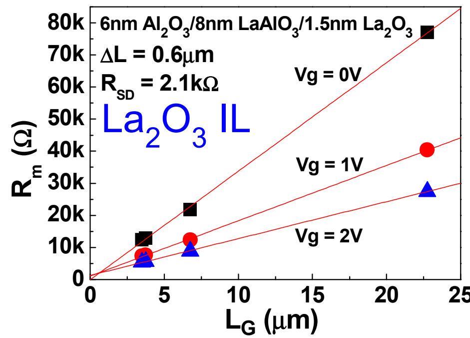

Fig. 9 R_m versus L_G under different gate biases in the linear region on $SrTiO_3$ MOSFETs with La_2O_3 as interfacial layer. La_2O_3 interface shows a sheet resistance of ~ 320 kΩ/sq. at zero bias.

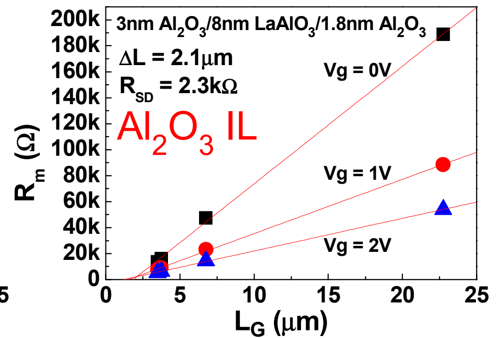

Fig. 10 R_m versus L_G under different gate biases in the linear region on $SrTiO_3$ MOSFETs with Al_2O_3 as interfacial layer. Al_2O_3 interface shows a sheet resistance of ~ 800 kΩ/sq. at zero bias.

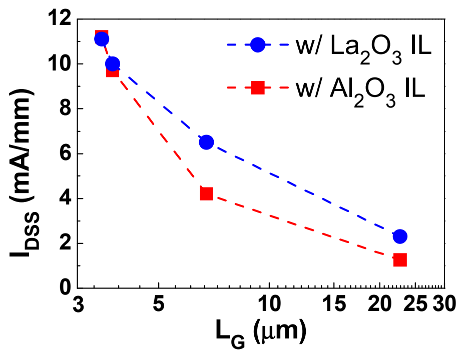

Fig. 11 Summary of the maximum drain current (I_{DSS}) at V_{GS}=5V vs L_G on $SrTiO_3$ MOSFETs with La_2O_3 and Al_2O_3 as interfacial layers. La_2O_3 devices have larger I_{DSS} at the same gate length.

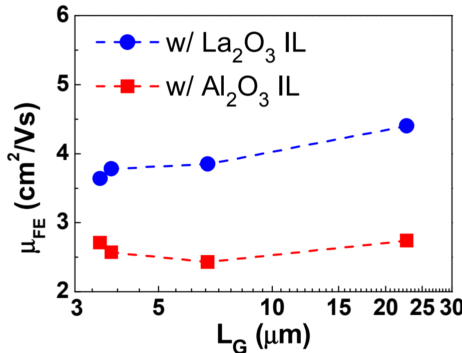

Fig. 12 Summary of field-effect mobility (μ_{FE}) at V_{GS}=5V vs L_G on $SrTiO_3$ MOSFETs with La_2O_3 and Al_2O_3 as interfacial layers. La_2O_3 devices have larger μ_{FE} at the same gate length.

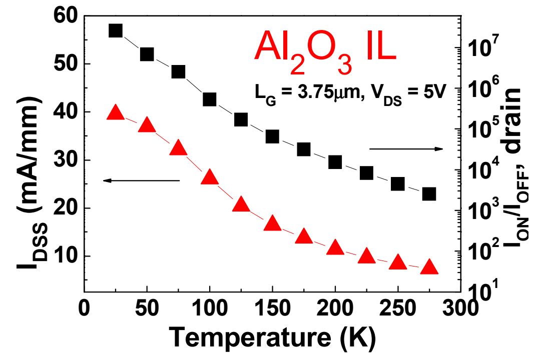

Fig. 13 I_{DSS} and I_{on}/I_{off} (drain current) vs. temperature for a $SrTiO_3$ MOSFET with a gate length of 3.75 µm and Al_2O_3 as an interfacial layer.

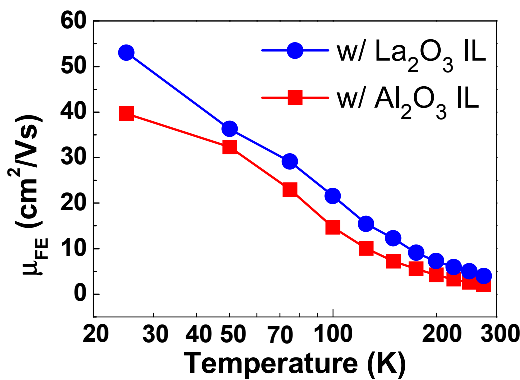

Fig. 14 Temperature dependent μ_{FE} at V_{GS}=5V on $SrTiO_3$ MOSFETs with La_2O_3 and Al_2O_3 as interfacial layers and at L_G =3.75 µm. La_2O_3 devices have larger μ_{FE} at the same gate length.

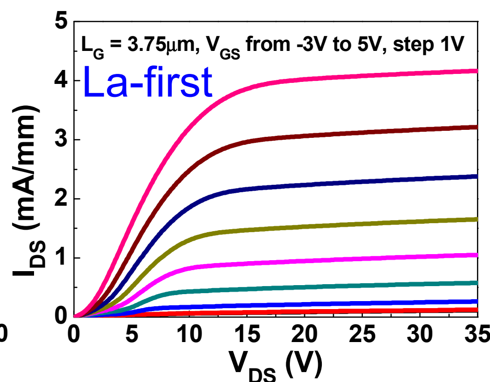

Fig. 15 High-voltage I-V output characteristics of a representative device among these $SrTiO_3$ MOSFETs. The device can be operated in tens of voltages as drain voltage due to the wide bandgap of $SrTiO_3$.

Fig. 16 $SrTiO_3$ single crystalline film was grown on 300 mm Si substrate by MBE as shown in the picture. The length of the ruler in the picture is 12 inch. The shining $SrTiO_3$ surface reflects the part of MBE system in which the film was grown.