High-Frequency Performance Projections for Ballistic Carbon-Nanotube Transistors

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This work was supported by the Network for Computational Nanotechnology (NCN) and the Microelectronics Advanced Research Corporation (MARCO) at Purdue University, and by the Natural Sciences and Engineering Research Council (NSERC) of Canada.

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Abstract

A quasi-static approach is combined with a theory of ballistic nanotransistors to assess the high-frequency performance potential of carbon-nanotube, field-effect transistors. A simple equivalent circuit, which applies in the ballistic limit of operation, is developed for the intrinsic device, and then employed to determine the behavior of the unity-current-gain frequency (f_T) with gate voltage. The circuit is shown to reduce to the expected forms in the so-called "MOS" and "bipolar" limits. The f_T is shown to approach a maximum value of $v_F/2\pi L \approx 130\,\text{GHz}/L\,(\mu\text{m})$ at high gate voltage, where v_F is the nanotube's Fermi velocity and L is the channel length, and to fall at low gate voltage due to the presence of source and drain electrostatic capacitances. The impact of the gate electrostatic capacitance on the f_T is also discussed. Numerical simulations on a "MOSFET-like" or "bulk-switched" carbon-nanotube transistor are shown to support the conclusions.

Keywords

Carbon-nanotube transistor, CNTFET, high-frequency performance, quantum capacitance, small-signal equivalent circuit, unity-current-gain frequency.

I. Introduction

Carbon-nanotube, field-effect transistors (CNTFETs) have now evolved to a state where an assessment of their high-frequency potential is essential to help identify their future role in electronics. Measurements [1]–[3] and initial modeling [4]–[6] are already being undertaken in this regard.

Frank and Appenzeller [1], [2] used a technique that circumvents the low-current-drive problem associated with CNTFETS, which are presently incapable of developing sufficient voltage across the loads presented by conventional high-frequency equipment. They applied a radio-frequency (RF) signal to the source of a diode-connected transistor, and then examined the shifted dc response at the drain, where the shift arises from the transistor's nonlinear current-voltage behavior. For a fixed RF amplitude, they showed that there was no change in the shifted dc response up to 250 MHz [1, Fig. 3], and hence demonstrated that the internal frequency response is at least this high (*i.e.*, that the carriers can respond); their method was later improved to show no change in the response up to 580 MHz [2, Fig. 3(b)].

Li *et al.* [3] measured the microwave reflection coefficient from a load Z_L comprised of a nanotube and a matching circuit. For a semiconducting tube, they found a resonance at 2.6 GHz [3, Fig. 5], which suggested that $Z_L = 50\,\Omega$ at this frequency. Changing the dc gate

bias on the tube changed the resonance amplitude, and the authors claim that this verifies the microwave operation of the transistor.

Burke [4], [5] has suggested an RF circuit model for a metallic nanotube, and emphasized the importance of both quantum capacitance and kinetic inductance. More recently [6], Burke used a standard formula [6, eq. (10)], along with estimated and measured values for the parameters, to predict the unity-current-gain frequency (f_T) of CNTFETs. For a one-micron-long device, he estimates the f_T to be parasitic dominated to a value around 8 GHz; if the parasitics can be reduced to negligible values, he estimates the f_T to be given by 80 GHz divided by the tube length in microns.

Further modeling is needed to definitively characterize the high-frequency potential of CNTFETs. Towards this end, in this work, we use a simple, quasi-static approach, together with a general description of ballistic nanotransistors [7], to develop an equivalent circuit in the ballistic limit of operation. The circuit is then employed to determine the ultimate f_T that can be expected from these devices, and to describe the behavior of f_T with gate voltage.

In Section II of this paper, the model of [7] is combined with the quasi-static assumption to establish the basic equations describing the time-dependent operation of a ballistic transistor. These equations are then employed in Section III to develop a small-signal equivalent circuit. In Section IV, the circuit is used to examine the behavior of the device's f_T with gate voltage, and the results are supported by numerical simulations presented in Section V. Issues related to the validity of the modeling approach, such as the reduction of the small-signal equivalent circuit to the appropriate forms in the so-called "MOS" and "bipolar" limits of operation, are discussed in Section VI. The conclusions are summarized in Section VII.

II. QUASI-STATIC APPROACH AND BASIC EQUATIONS

In the "quasi-static" approach to transistor modeling, dynamic behavior is predicted by employing static equations for charge (or carrier density) and transport current, but with static voltages replaced by their time-dependent counterparts:

$$Q(V_G, V_D, V_S) \rightarrow Q[V_G(t), V_D(t), V_S(t)] \tag{1}$$

$$I(V_G, V_D, V_S) \rightarrow I[V_G(t), V_D(t), V_S(t)] \tag{2}$$

where Q is charge, I is current, t is time, and V_G, V_D, and V_S are the gate, drain, and source voltages, respectively.

Referring to Fig. 1, and employing the model developed in [7] with the quasi-static assumption, one can write the following relations for the electron density at the top of the source-channel energy barrier (located at $z = z_{\text{top}}$):

$$n^+(t) = \frac{1}{2}\int_{E_{\text{C,eq}}}^{\infty} D(E) f[E - qV_{\text{SCF}}(t) - E_F + qV_S(t)]\, dE \tag{3}$$

$$n^-(t) = \frac{1}{2}\int_{E_{\text{C,eq}}}^{\infty} D(E) f[E - qV_{\text{SCF}}(t) - E_F + qV_D(t)]\, dE \tag{4}$$

where n^+ refers to the positive-going (source-injected) density; n^- refers to the negative-going (drain-injected) density; E is energy; $f(E) = 1/[1 + \exp(E/k_BT)]$ refers to the equilibrium Fermi function with k_B being Boltzmann's constant and T being temperature; E_F is the equilibrium Fermi level; $V_{\text{SCF}} = (1/q)(E_{\text{C,eq}} - E_{\text{top}})$ is the "self-consistent potential" at the top of the barrier, which can be visualized as $1/q$ times the distance between the equilibrium conduction-band edge[1] $E_{\text{C,eq}}$ and the band edge under applied voltage E_{top}, with q being the magnitude of the electronic charge; and $D(E)$ is the nanotube's equilibrium density of states [specified by (28) below]. Similarly, the following relations for the transport current can also be written:

$$I_T(t) = I_T^+(t) + I_T^-(t) \tag{5}$$

$$I_T^+(t) = \frac{-4q}{h}\int_{E_{\text{C,eq}}}^{\infty} f[E - qV_{\text{SCF}}(t) - E_F + qV_S(t)]\, dE \tag{6}$$

$$I_T^-(t) = \frac{+4q}{h}\int_{E_{\text{C,eq}}}^{\infty} f[E - qV_{\text{SCF}}(t) - E_F + qV_D(t)]\, dE \tag{7}$$

where h is Planck's constant, I_T is the net transport current (defined as positive when flowing from source to drain), and I_T^+ and I_T^- are the source- and drain-injected components of I_T. Here, we assume only one subband is important for transport, although an extension to multiple subbands can easily be accomplished. On the other hand, the band diagram in Fig. 1 and the model of [7], and hence the analysis to follow, strictly apply only to "MOSFET-like" CNTFETs [7, p. 1859]. Such devices, also known as "bulk-switched" CNTFETs, are now being fabricated

[1] The presence of qV_{SCF} in the argument of the Fermi functions, as opposed to the density of states, in (3) and (4), means that the lower limit of integration must be the position of the conduction-band edge *at equilibrium*. Alternatively, a change of variable allows one to rewrite these relations in terms of a shifted density of states, $D(E + qV_{\text{SCF}})$, and a lower limit of integration that is equal to the band edge under applied voltage, $E_{\text{top}} = E_{\text{C,eq}} - qV_{\text{SCF}}$.

with techniques such as "electrostatic" or chemical doping of the source and drain contact regions [8]–[11]. The idea is to suppress the Schottky barriers at the source and drain contacts, so that the device operates by "bulk switching" in the channel region, just like a conventional MOSFET. Vastly improved dc characteristics have been reported for these new devices, compared to the earlier "Schottky-barrier" CNTFETs, where the device operation was controlled by modulation of the Schottky barriers at the source and drain contacts. In this work, we focus our attention on the improved MOSFET-like (or bulk-switched) structure in order to get a basic idea of ultimate performance limits.

Equations (3) and (4) must be solved *self-consistently* with an electrostatic constraint. As described in [7], this constraint can be written in terms of gate, source, and drain electrostatic capacitances, denoted C_{GE}, C_{SE}, and C_{DE}, respectively, the total carrier density $N(t) = n^{+}(t) + n^{-}(t)$, the total equilibrium carrier density N_0, and the applied voltages, as follows:

$$q[N(t) - N_0] = C_{\text{GE}}[V_G(t) - V_{\text{SCF}}(t)] + C_{\text{SE}}[V_S(t) - V_{\text{SCF}}(t)] + C_{\text{DE}}[V_D(t) - V_{\text{SCF}}(t)]. \tag{8}$$

Use of (3) and (4) on the left-hand side of (8) then yields an equation for the self-consistent potential $V_{\text{SCF}}(t)$. By using the change of variable $E' = E - E_{\text{C,eq}}$ in (3) and (4), with $D(E)$ specified by (28) below, it can easily be shown that the resulting equation will depend only on V_D, V_S, and V_G, and on the internal energy difference $E_{\text{C,eq}} - E_F$. With respect to the external voltages, any one of V_D, V_S, or V_G can be chosen as a reference, as long as the other two are then quoted in terms of this reference; this follows because the device responds only to potential *differences* applied between its external terminals. The internal difference $E_{\text{C,eq}} - E_F$ can be treated as an input parameter.

To determine the ac behavior, the standard procedure is to assume sinusoidal excitation, write each time-dependent quantity in (3)–(8) in terms of static (dc or bias) and dynamic (ac or small-signal) parts, for example, $V(t) = \bar{V} + \tilde{V}\exp(j\omega t)$, where $\bar{V}$ refers to the dc value and $\tilde{V}$ refers to the complex ac amplitude, and then employ Taylor-series expansions to solve the equations for the ac terminal currents in terms of the ac terminal voltages. A simpler, more intuitive approach is to develop a small-signal equivalent circuit whose elements depend on the derivatives of the equations for charge and current with respect to voltage. If the elements are suitably arranged, then this procedure is equivalent to the mathematical procedure of solving the

equations. We will follow the equivalent-circuit approach.

III. Equivalent Circuit for a Ballistic Transistor

For small ac signals, the electrostatic constraint specified by (8) can be represented by the network of Fig. 2(a). From the network, the charge on the *outer* plates of the electrostatic capacitors is

$$q\tilde{N} = C_{\text{GE}}[\tilde{V}_G - \tilde{V}_{\text{SCF}}] + C_{\text{SE}}[\tilde{V}_S - \tilde{V}_{\text{SCF}}] + C_{\text{DE}}[\tilde{V}_D - \tilde{V}_{\text{SCF}}]. \tag{9}$$

Equation (9) can be recognized as the linearized version of (8).

The transport relations (3) and (4) can be differentiated to obtain two transport or "quantum" [12] capacitances:

$$C_{\text{SQ}} = q\frac{\partial n^+}{\partial(V_{\text{SCF}} - V_S)} \tag{10}$$

$$C_{\text{DQ}} = q\frac{\partial n^-}{\partial(V_{\text{SCF}} - V_D)}. \tag{11}$$

It is important to note that the derivatives in (10) and (11) are to be evaluated from (3) and (4) while neglecting the electrostatic constraint of (8). The capacitors C_{SQ} and C_{DQ} hence relate a change in channel charge to a change in channel potential, *based solely on transport considerations*. For small ac signals, the capacitive network in Fig. 2(b) thus represents the transport relations for charge, where

$$q\tilde{N} = C_{\text{SQ}}(\tilde{V}_{\text{SCF}} - \tilde{V}_S) + C_{\text{DQ}}(\tilde{V}_{\text{SCF}} - \tilde{V}_D) \tag{12}$$

is the charge on the *inner* plates of the quantum capacitors. Equation (12) is just the sum of the linearized versions of (3) and (4).

The electrostatic and transport networks of Figs. 2(a) and 2(b) must be connected, and the appropriate connections are shown in Fig. 2(c). These connections demand that the electrostatics and transport agree on both the self-consistent potential $\tilde{V}_{\text{SCF}}$ and the channel charge $q\tilde{N}$; they are equivalent to mathematically demanding that (9) and (12) be solved self-consistently.

In analogy to (10) and (11), it is possible to define two transport or "quantum" transconduc-

tances:

$$g_{\text{SQ}} = q\frac{\partial I_T^+}{\partial(V_S - V_{\text{SCF}})} \tag{13}$$

$$g_{\text{DQ}} = q\frac{\partial I_T^-}{\partial(V_D - V_{\text{SCF}})}. \tag{14}$$

Again, the right-hand sides of (13) and (14) are to be computed by differentiating (6) and (7) while ignoring the constraint imposed by (8). The transconductances g_{SQ} and g_{DQ} hence characterize the modulation of transport current (as opposed to charge) with channel potential, *based solely on transport considerations*. However, since the network of Fig. 2(c) already accounts for self-consistency between the transport and electrostatics, it is sufficient to complete the small-signal equivalent circuit by simply adding two dependent current generators $g_{\text{SQ}}(\tilde{V}_S - \tilde{V}_{\text{SCF}})$ and $g_{\text{DQ}}(\tilde{V}_D - \tilde{V}_{\text{SCF}})$, as shown in Fig. 3(a). Straightforward network transformations yield the alternative form in Fig. 3(b), where

$$g_m = \frac{C_{\text{GE}}}{C_\Sigma}\left(g_{\text{SQ}} + g_{\text{DQ}}\right) \tag{15}$$

and

$$g_0 = \left(\frac{C_{\text{DE}} + C_{\text{DQ}}}{C_\Sigma}\right) g_{\text{SQ}} - \left(\frac{C_{\text{GE}} + C_{\text{SE}} + C_{\text{SQ}}}{C_\Sigma}\right) g_{\text{DQ}} \tag{16}$$

with $C_\Sigma \equiv C_{\text{GE}} + C_{\text{SE}} + C_{\text{DE}} + C_{\text{SQ}} + C_{\text{DQ}}$ being the total device capacitance.

IV. Unity-Current-Gain Frequency

One measure of the high-frequency potential of a transistor is the extrapolated, common-source, unity-current-gain frequency, f_T. We can compute f_T from the circuit of Fig. 3(a) [or 3(b)] to get an idea of transistor speed in the ballistic limit. However, strictly speaking, the capacitance values in the circuit are per-unit-length values, and the circuit accounts for charging effects only at the location of the top of the barrier, *i.e.*, at $z = z_{\text{top}}$. To get an initial estimate of the key factors affecting speed, we will simply multiply the capacitances by the channel length L. If we denote the conduction-band edge under bias at the top of the barrier by E_{top}, as shown in Fig. 1, and assume the device is in saturation (*i.e.*, that the gate and drain voltages are large), then at each point z in the channel, where $z_{\text{top}} \leq z \leq z_{\text{top}} + L$, there should be little charge at energies below E_{top}, and the charge at energies above E_{top} will be less than or equal to the value at $z = z_{\text{top}}$. Therefore, use of the circuit in Fig. 3(a) with capacitance values multiplied by L

should *overestimate* the total channel charge, and hence, if anything, *underestimate* the ballistic f_T. We will later show that the results are in good agreement with those from two-dimensional numerical simulation, at least for high-performance structures.

Analysis of the circuit of Fig. 3(a) yields the following result for f_T:

$$\frac{1}{2\pi f_T} = \tau_Q + \tau_E \tag{17}$$

where τ_Q and τ_E are transport (or "quantum") and electrostatic time constants, respectively, and are given by

$$\tau_Q = L\left[\frac{C_{\mathrm{SQ}} + C_{\mathrm{DQ}}}{g_{\mathrm{SQ}} + g_{\mathrm{DQ}}}\right] \tag{18}$$

and

$$\tau_E = L\left[\frac{C_{\mathrm{SE}} + C_{\mathrm{DE}}}{g_{\mathrm{SQ}} + g_{\mathrm{DQ}}}\right]. \tag{19}$$

Alternatively, if the circuit in Fig. 3(b) is employed, one will find that

$$\frac{1}{2\pi f_T} = \frac{g_m}{LC_{\mathrm{GS}}} \tag{20}$$

where C_{GS} is the effective input capacitance of the CNTFET, specified by the series combination of C_{GE} and $(C_{\mathrm{SE}} + C_{\mathrm{DE}} + C_{\mathrm{SQ}} + C_{\mathrm{DQ}})$:

$$C_{\mathrm{GS}} = \frac{C_{\mathrm{GE}}(C_{\mathrm{SE}} + C_{\mathrm{DE}} + C_{\mathrm{DQ}} + C_{\mathrm{SQ}})}{C_\Sigma} \tag{21}$$

where C_Σ was specified below (16) as the total device capacitance. However, use of (15) shows that (20) and (21) are equivalent to (17)–(19), which are the relations we will use to examine the behavior of f_T. In doing so, it is useful to note that for operation of the device in saturation, there is essentially no transport charge from the drain at energies above E_{top}, so $g_{\mathrm{DQ}} \approx 0$ and $C_{\mathrm{DQ}} \approx 0$ in (18) and (19).

The gate electrostatic capacitance C_{GE} does not explicitly appear in (17)–(19). However, C_{GE} *does* impact the f_T, and, in particular, its *bias dependence*, through the bias dependence of C_{SQ} and g_{SQ}; each of these is found from the derivative of a static charge or current, as specified in Section III, and the static solutions are impacted by C_{GE} through the static part of (8). Further comments regarding the dependence of f_T on C_{GE} will be reserved until the discussion of Fig. 5(b).

To interpret τ_Q, it is necessary to introduce the idea of an "ac distribution function." Under ballistic transport, forward-going carriers are injected from the source and are governed by the source Fermi function,

$$f_S(E,t) = f[E - qV_{\text{SCF}}(t) - E_F + qV_S(t)]. \tag{22}$$

Under small-signal excitation, f_S can be split into static and dynamic parts:

$$f_S(E,t) \approx \bar{f}_S(E) + \tilde{f}_S(E)\exp(j\omega t) \tag{23}$$

where

$$\bar{f}_S(E) = f(E - \bar{\mu}_{\text{eff}}) \tag{24}$$

and

$$\begin{aligned}\tilde{f}_S(E) &= \left.\frac{\partial f}{\partial E}\right|_{E-\bar{\mu}_{\text{eff}}} \times q(\tilde{V}_S - \tilde{V}_{\text{SCF}}) \\ &= \frac{-1}{4k_BT}\text{sech}^2\left[\frac{E-\bar{\mu}_{\text{eff}}}{2k_BT}\right] \times q(\tilde{V}_S - \tilde{V}_{\text{SCF}})\end{aligned} \tag{25}$$

and we have introduced an "effective Fermi level," $\bar{\mu}_{\text{eff}} \equiv E_F + q(\bar{V}_{\text{SCF}} - \bar{V}_S)$, seen at the top of the barrier. Figure 4 shows the shapes of $\bar{f}_S(E)$ and $\tilde{f}_S(E)$ versus energy E, assuming a value of $\bar{\mu}_{\text{eff}}$ that lies above the equilibrium conduction-band edge. The key point to note is that whereas $\bar{f}_S$ is a measure of carrier occupancy for static signals, $\tilde{f}_S$ measures the perturbation in the occupancy under small-signal excitation, and is hence *a measure of those energy channels that most effectively carry the ac current*.

The time τ_Q can now be interpreted as an appropriate average over the ac distribution function $\tilde{f}_S$. Since the carrier velocity is $v(E) = (1/\hbar)[dE/dk]$, and the density of states in the one-dimensional nanotube system is $D(E) = 8/hv(E)$, the time τ_Q can be expressed as follows:

$$\tau_Q \approx \frac{L \times C_{\text{SQ}}}{g_{\text{SQ}}} = \frac{\int_{E_{\text{C,eq}}}^{\infty} \tilde{f}_S(E)[L/v(E)]\,dE}{\int_{E_{\text{C,eq}}}^{\infty} \tilde{f}_S(E)\,dE}. \tag{26}$$

In other words, τ_Q *represents a type of average transit time for carriers injected from the source*. Since this average is computed using information (contained in $\tilde{f}_S$) that strictly applies only at $z = z_{\text{top}}$, where the velocity of the carriers is the slowest, then at any dc bias, the value from (26) can be viewed as an upper bound on τ_Q, and the corresponding value $1/2\pi\tau_Q$ will

tend to underestimate the transport (or "quantum") component of f_T, a point to which we have already alluded.

The time τ_E is just the charging time for the source and drain electrostatic capacitances when $\tilde{V}_{\text{DS}} \equiv 0$ (the condition under which f_T is defined); this becomes clear if one explicitly writes

$$\tau_E \approx \left.\frac{L(C_{\text{SE}} + C_{\text{DE}})}{g_{\text{SQ}}}\right|_{\tilde{V}_{\text{DS}} \equiv 0} = \frac{L(C_{\text{SE}} + C_{\text{DE}}) \times \tilde{V}_{\text{SCF}}}{g_{\text{SQ}} \times \tilde{V}_{\text{SCF}}} \equiv \frac{\tilde{Q}_{\text{SE}} + \tilde{Q}_{\text{DE}}}{\tilde{I}_T}. \tag{27}$$

The overall f_T is limited by the larger of τ_Q and τ_E, as specified by (17).

Figure 5(a) shows a plot of f_T versus gate-bias voltage (taking the source as reference) for a representative device, computed using the above relations and an equilibrium nanotube density of states given by [13, eq. (2)]

$$D(E) = \frac{8}{3\pi a_0 t_E}\left[\frac{E - E_{\text{C,eq}} + \Delta}{\sqrt{(E - E_{\text{C,eq}} + \Delta)^2 - \Delta^2}}\right] \tag{28}$$

where $a_0 \approx 1.42$ Å and $t_E \approx 3.0$ eV are the carbon-carbon bonding distance and energy, respectively, and $\Delta = t_E a_0/d$ is one-half the nanotube's bandgap with d being the tube's diameter. The device is assumed to be a coaxially gated, zigzag nanotube, and to have the following parameter values: equilibrium Fermi level E_F located 0.32 eV below the equilibrium conduction-band edge; a tube diameter $d = 1$ nm; a gate oxide with a thickness $t_{\text{ox}} = 3$ nm and a relative dielectric constant $\kappa = 25$; and a channel length $L = 30$ nm. The gate oxide capacitance was computed from the well-known result for a cylindrical structure,

$$C_{\text{ox}} = \frac{2\pi\kappa\epsilon_0}{\ln[(t_{\text{ox}} + d/2)/(d/2)]} \tag{29}$$

and values $C_{\text{GE}} \equiv C_{\text{ox}}$, $C_{\text{SE}} \approx 0.097 C_{\text{ox}}$, and $C_{\text{DE}} \approx 0.040 C_{\text{ox}}$ were assumed for the purposes of illustration. The drain bias was held fixed at 0.7 V.

As shown in Fig. 5(a), at low gate voltage, f_T is limited by the electrostatic time constant τ_E; here, $C_{\text{SE}}, C_{\text{DE}} \gg C_{\text{SQ}}$ and hence $f_T \approx g_{\text{SQ}}/[2\pi L(C_{\text{SE}} + C_{\text{DE}})]$ follows the exponential dependence of g_{SQ} on V_G. At high gate voltage, when the source quantum capacitance becomes sufficiently large, f_T takes on the value $1/2\pi\tau_Q$, with τ_Q specified by the right side of (26). As the gate voltage is further increased, the self-consistent potential and hence $\bar{\mu}_{\text{eff}}$ both increase, and $\tilde{f}_S(E)$ in (25) becomes nonzero only at energies where $v(E)$ is approximately constant and equal to the Fermi velocity v_F. As a result, τ_Q approaches the value L/v_F, and the f_T

approaches the value $v_F/2\pi L \approx 130$ GHz$/L\,(\mu\text{m})$; since v_F represents the highest attainable carrier velocity in nanotubes, this value of f_T also represents the maximum that is achievable.

It was mentioned earlier that $C_{\text{GE}} \equiv C_{\text{ox}}$ can impact the bias dependence of f_T. In Fig. 5(b), we have replotted the f_T using a C_{ox} value that is five times smaller than that in Fig. 5(a), with all other parameters unchanged. With a smaller C_{ox}, the gate bias is not as effective in controlling the self-consistent potential $\bar{V}_{\text{SCF}}$ at the top of the barrier; it takes more gate bias to create a given $\bar{V}_{\text{SCF}}$. Referring back to Fig. 4, with a smaller oxide capacitance, this means that the effective Fermi level $\bar{\mu}_{\text{eff}} \equiv E_F + q(\bar{V}_{\text{SCF}} - \bar{V}_S)$ seen at the top of the barrier will cross the equilibrium conduction-band edge at higher gate-bias voltages. As a result, τ_Q in (18) approaches its limiting value of L/v_F, and the f_T approaches its limiting value of $v_F/2\pi L$, at higher gate-bias voltages. This can clearly be seen when comparing parts (a) and (b) of Fig. 5. Thus, perhaps counterintuitively, a *smaller* C_{ox} will cause the f_T to approach its peak value at *higher* gate-bias voltages.

V. Numerical Results

Given a numerical simulation program that self-consistently solves the transport and Poisson equations, it is possible to extract the device f_T within the quasi-static approximation. In this case, the result is given by the well-known expression

$$f_T = \left[\frac{1}{2\pi}\right]\left[\frac{dI_D}{dQ_G}\right] \tag{30}$$

where dI_D and dQ_G refer to the changes in static drain-to-source current and gate-electrode charge, respectively, arising from a small change in gate voltage while the drain voltage is held fixed (and the source is taken as reference).

For comparison with the analytical results of Section IV, we numerically simulated a MOSFET-like carbon-nanotube transistor. The simulated device has the same structure and parameter values used in conjunction with Fig. 5, and employs heavily doped source and drain regions surrounding the channel to form an ideal n-i-n “bulk-switched” device. The metal contacts to the source and drain regions were assumed to be ideal (*i.e.*, *without* Schottky barriers), which allowed us to treat the transport semiclassically, and the results were obtained from a self-consistent, Boltzmann-equation solver under ballistic conditions.

Figure 6 shows plots of key quantities versus position z along the channel, under *static* conditions, obtained from the numerical simulation; shown are the band edge under bias $E_C(z)$, the average carrier velocity $v_{\text{avg}}(z)$, and the carrier density $n(z)$. Interestingly, the band edge (and hence potential), carrier velocity, and carrier density are all essentially *constant* along the channel. This important result can be understood by using the "gradual-channel approximation (GCA)" [14, pp. 127–128], [15, pp. 193–194] to obtain an equation for the self-consistent potential $V_{\text{SCF}}(z)$ at each point along the channel. Assuming for simplicity that $C_{\text{GE}} \equiv C_{\text{ox}}$ and $C_{\text{DE}} = C_{\text{SE}} = 0$ in (8), and neglecting the drain-injected charge, one can employ the GCA to equate the electrostatic charge to the transport charge at each point $z \geq z_{\text{top}}$:

$$C_{\text{ox}}[V_G - V_{\text{SCF}}(z)] = q \int_{E_{\text{top}}}^{\infty} D[E + qV_{\text{SCF}}(z)] f[E - E_F + qV_S] \, dE. \tag{31}$$

At high energies, the nanotube density of states becomes approximately constant, corresponding to a linear E-k relationship. As a result, for points $z > z_{\text{top}}$, if we assume $V_{\text{SCF}}(z) \gg V_{\text{SCF}}(z_{\text{top}})$, we can approximate the density of states $D[E + qV_{\text{SCF}}(z)]$ on the right-hand side of (31) by a constant value $8/hv_F$; however, solving (31) for $V_{\text{SCF}}(z)$ on the left-hand side then yields a result that is independent of z. We conclude that the only possible solution of (31) is $V_{\text{SCF}}(z) \approx V_{\text{SCF}}(z_{\text{top}})$, and since the potential is independent of z, so must be the carrier velocity and density. Of course, this result, which has been pointed out and discussed before [16, pp. 4887–4888], hinges on the validity of the GCA, and two-dimensional electrostatics will cause variations, especially near the drain end, as illustrated in Fig. 6. Nevertheless, we expect it to be a good approximation under ballistic transport in high-performance structures, where the gate has good control over the channel potential.

The constancy of the channel potential implies that the circuit developed in Section III by considering only the top of the barrier can continue to be used, provided the capacitances in it are appropriately interpreted. In a MOSFET-like device, the presence of heavily doped source and drain regions leads to the formation of pn junctions at the source- and drain-channel interfaces (where there is heavy band bending in $E_C(z)$ in Fig. 6, around $z = 10$ and 40 nm). Therefore, there are junction space-charge capacitances, C_{JS} and C_{JD}; these then replace LC_{SE} and LC_{DE}. The quantum capacitances remain, but should account for all the channel charge, and are hence redefined to equal the integrals of the right sides of (10) and (11) over the entire channel region; the constancy of the channel potential means that these integrations will approximately equal the

values from (10) and (11) multiplied by the channel length L. Similarly, the gate electrostatic capacitance is just LC_{ox}. The modified circuit is shown in Fig. 7(a).

Since the circuit topology continues to be valid, we should expect the results for f_T from the numerical simulation to be similar to those from the analytical approach in Fig. 5. This is indeed the case, as illustrated in Fig. 8. The falloff in f_T at low gate voltages is due to the presence of C_{JS} and C_{JD} in the MOSFET-like structure, and at high gate voltage, the f_T saturates to a value of approximately $v_F/2\pi L$, as expected. The nonlinear nature of the f_T curve at low gate voltage is due to the nonlinear nature of C_{JS} and C_{JD}, whereas LC_{SE} and LC_{DE} were assumed constant in the calculations for Fig. 5. In general, C_{JS} and C_{JD} will affect both the low-voltage f_T falloff as well as the output conductance g_0, as specified by (16) with $C_{\text{SE}} \rightarrow C_{\text{JS}}/L$ and $C_{\text{DE}} \rightarrow C_{\text{JD}}/L$, and their values must be chosen accordingly if the equivalent circuit is used to mimic numerical results. Alternatively, one could simply employ the *topology* of Fig. 7(a), but use *independently* chosen values for both the output conductance g_0 and transconductance g_m, as found, for example, from the slopes of dc current-voltage characteristics, instead of the values suggested by (15) and (16). In either case, it should be noted that the values of g_m and g_0 will be *effective* values that automatically account for the Landauer contact conductances, which should hence not be included in the circuit separately; in (15) and (16), the conductances are contained within g_{SQ} and g_{DQ} on the right-hand side, and in measurements, information on the conductances will be embedded in the dc characteristics (and hence the extracted values of g_m and g_0) seen at the external terminals.

VI. Discussion

A. *MOS and Bipolar Limits*

The quantum and junction capacitances are not usually considered when characterizing the intrinsic operation of conventional MOSFETs.

Assuming a large drain voltage such that $C_{\text{DQ}} \rightarrow 0$, and then taking the limit where $C_{\text{SQ}} \rightarrow \infty$ and $C_{\text{JS}}, C_{\text{JD}} \rightarrow 0$, the channel charge is determined solely by the gate voltage, and the device is said to operate in the "MOS limit." In this case, the circuit of Fig. 7(a) reduces to that in Fig. 7(b), which can be recognized as having the same topology as the usual small-signal circuit for an intrinsic MOSFET in saturation [14, Figs. 8.17, 8.21]. However, a key difference exists in the value of capacitance seen between the gate and source terminals. In a conventional

MOSFET, this value is $(2/3)LC_{\text{ox}}$, owing to the ohmic drop along the channel, which causes varying levels of inversion from source to drain [15, pp. 240–255]. On the other hand, in a CNTFET, the constancy of the channel potential means that the appropriate value is LC_{ox}.

In the limit that $C_{\text{ox}} \to \infty$ (and again assuming $C_{\text{DQ}} \to 0$), the device is said to operate in the "bipolar limit." In this case, the gate voltage has direct control over the channel potential, and the appropriate equivalent circuit is shown in Fig. 7(c); this resembles the well-known "hybrid-π" model for an intrinsic bipolar transistor working in the forward-active mode [17, Fig. 7.4(b)], but with an infinite value for the incremental base-emitter (gate-source) resistance, since the gate current must be zero at low frequencies.

B. Schottky-Barrier Devices and Scattering

It is worth mentioning here that the circuit in Fig. 7(a) may also have merit for ballistic Schottky-barrier devices. In this case, C_{JS} and C_{JD} could be used to represent the effects of space-charge capacitances arising from the Schottky contacts at the source and drain. The channel region could then be defined as that over which the potential is roughly constant, and the other circuit elements would retain their meaning. However, this requires further study, especially for short devices, where quantum-mechanical effects at the contact barriers are likely to play a role, and where the channel potential is unlikely to be constant. Similarly, the effects of scattering in longer devices also needs study. These are topics of current research, and the results will be reported elsewhere.

VII. CONCLUSIONS

The following conclusions can be drawn from this study of the high-frequency performance potential of carbon-nanotube, field-effect transistors:

1. Starting from a theory of ballistic transistors [7] that focuses on the "top of the (source-drain) barrier," and under the quasi-static assumption, a simple, intuitive equivalent circuit can be developed for a ballistic carbon nanotube transistor. The circuit reduces to the expected forms in the so-called "MOS" and "bipolar" limits.

2. The circuit predicts an intrinsic, ballistic f_T that approaches a limiting value of $v_F/2\pi L$ at high gate bias, *i.e.*, approximately 130 GHz$/L\,(\mu\text{m})$, and that falls at low gate bias

due to the presence of source and drain electrostatic capacitances. The gate electrostatic capacitance $C_{\text{GE}} \equiv C_{\text{ox}}$ also impacts the f_T, with a lower C_{ox} causing the f_T to approach its limiting value of $v_F/2\pi L$ at a higher gate bias.

3. Numerical simulations for a "MOSFET-like" or "bulk-switched" CNTFET show that the circuit holds merit if the capacitances in it are appropriately interpreted; correspondingly, the simulations predict f_T values and behavior similar to those from the top-of-the-barrier approach.

Further work is needed to understand the role of scattering in longer devices; to examine the role of "kinetic inductance" [4], [5], [18] and non-quasi-static effects; to assess the role of parasitics [19]; and to characterize small-signal properties other than the f_T.

ACKNOWLEDGMENTS

The authors are indebted to Mark Lundstrom, Supriyo Datta, and Diego Kienle of Purdue University, and Jing Guo of the University of Florida, for many helpful discussions.

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Figure Captions

Fig. 1. Sketch of the conduction-band edge $E_C(z)$ versus transport direction z in a carbon-nanotube transistor. The E-k relation at $z = z_{\text{top}}$, the location of the top of the source-drain barrier, is also shown. The level $E_{\text{C,eq}}$ denotes the position of the conduction-band edge at equilbrium. The level E_{top} denotes the conduction-band edge at the point $z = z_{\text{top}}$ under applied voltage. The energy difference $qV_{\text{SCF}} = E_{\text{C,eq}} - E_{\text{top}}$ is marked on the diagram. The diagram is *not* to scale.

Fig. 2. (a) Electrostatic network representing the relation (9). (b) Transport network representing the relation (12). (c) Overall capacitive network for ac signals. The "$+$" signs are used to indicate that the sum of the charges on the outer plates of the electrostatic capacitors must equal the sum of the charges on the inner plates of the transport or "quantum" capacitors.

Fig. 3. (a) Small-signal equivalent circuit for a ballistic carbon-nanotube transistor, based on a quasi-static treatment of transport at the top of the source-channel energy barrier. (b) Alternate form of the equivalent circuit, explicitly showing the transconductance g_m and output conductance g_0; equations (15) and (16) specify the values of g_m and g_0 in terms of the elements appearing in part (a).

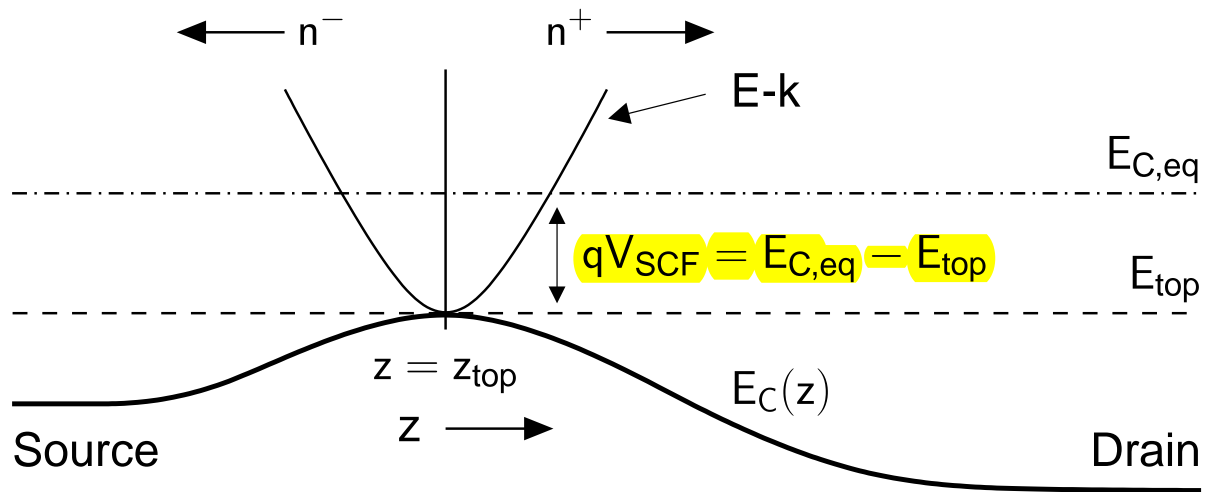
Fig. 4. Sketches of the static and dynamic parts of the source Fermi function $f_S(E)$ versus energy E. The static part $\bar{f}_S(E)$ is specified by (24), and the dynamic part $\tilde{f}_S(E)$ is given by (25). For reference, the positions $E_{\text{C,eq}}$ (the conduction-band edge at equilibrium) and $\bar{\mu}_{\text{eff}} \equiv E_F + q(\bar{V}_{\text{SCF}} - \bar{V}_S)$ (an effective Fermi level seen at the top of the barrier) are also shown.

Fig. 5. (a) Plot of the unity-current-gain frequency f_T versus gate-bias voltage V_G for a zigzag carbon-nanotube transistor, as computed from the analytical relations developed in this work. The drain bias is held fixed at 0.7 V. The device parameters are specified in the text below (28). (b) A replot of f_T for the device in part (a), but with the oxide capacitance reduced by a factor of five while holding all other parameters constant.

Fig. 6. Plots of key quantities versus position z along the channel, as found from numerical simulation under *static* conditions, for various values of gate bias and a drain bias of 0.7 V. Shown are the band edge under bias $E_C(z)$, the average carrier velocity $v_{\text{avg}}(z)$, and the carrier density $n(z)$.

Fig. 7. (a) Small-signal equivalent circuit for a "MOSFET-like" carbon-nanotube transistor operating under ballistic conditions. The circuit has the same topology as that in Fig. 3(b), but the capacitances have been redefined, as described in the text. Parts (b) and (c) show the forms of the equivalent circuit when the device is operating in the "MOS" and "bipolar" limits, respectively.

Fig. 8. Plot of the unity-current-gain frequency f_T versus gate-bias voltage V_G for a "MOSFET-like" carbon-nanotube transistor operating under ballistic conditions, as found from numerical simulation. The drain bias is held fixed at 0.7 V. Other than the doped source and drain regions, the device parameters are the same as those used in conjunction with Fig. 5.



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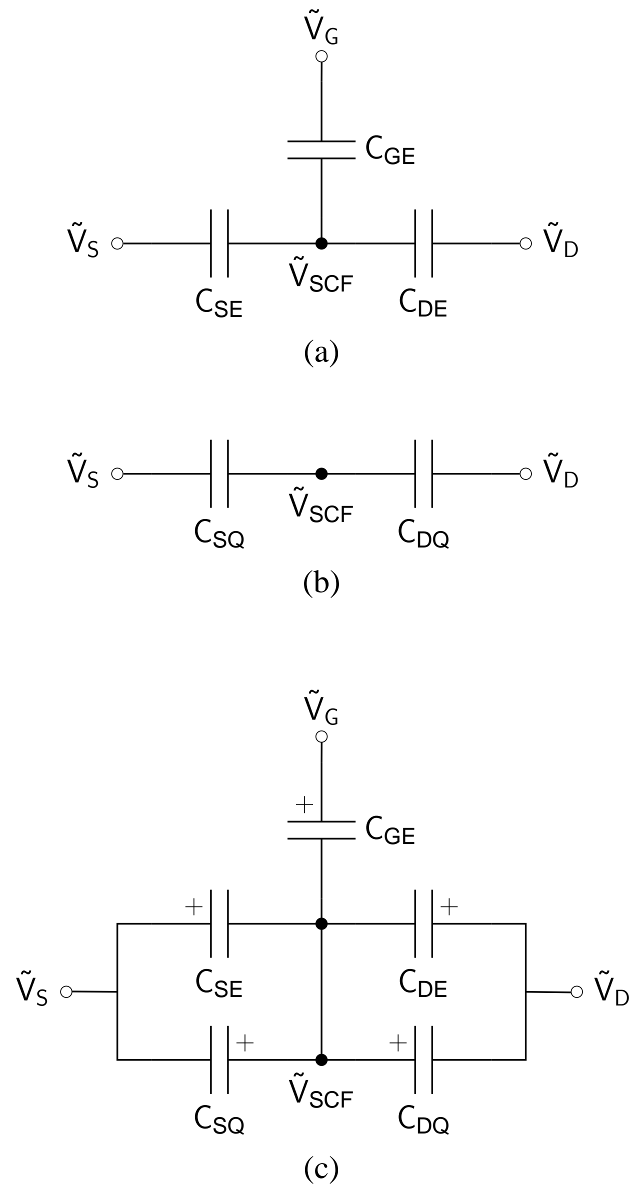
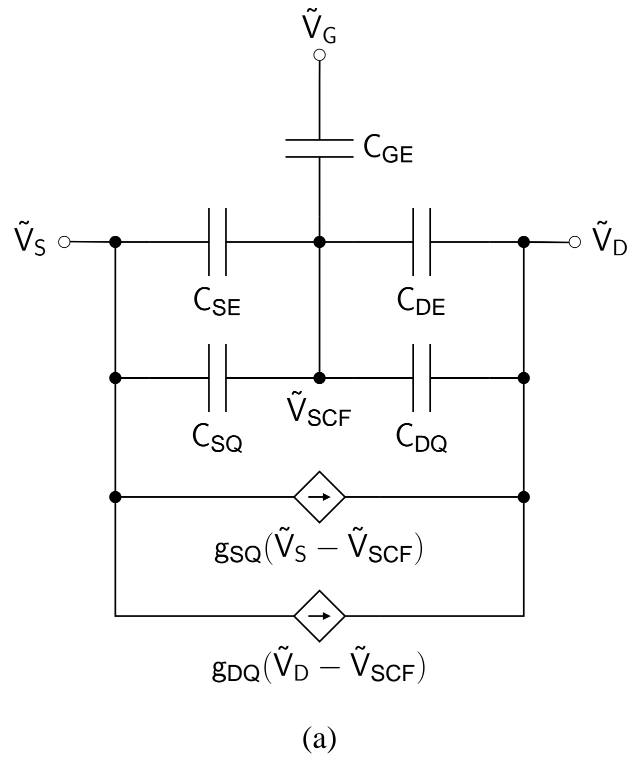
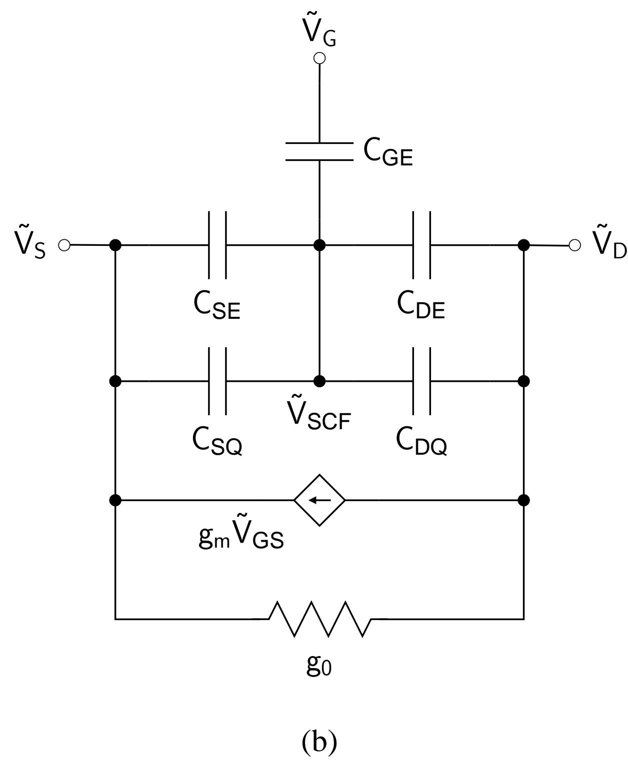


Figure 2

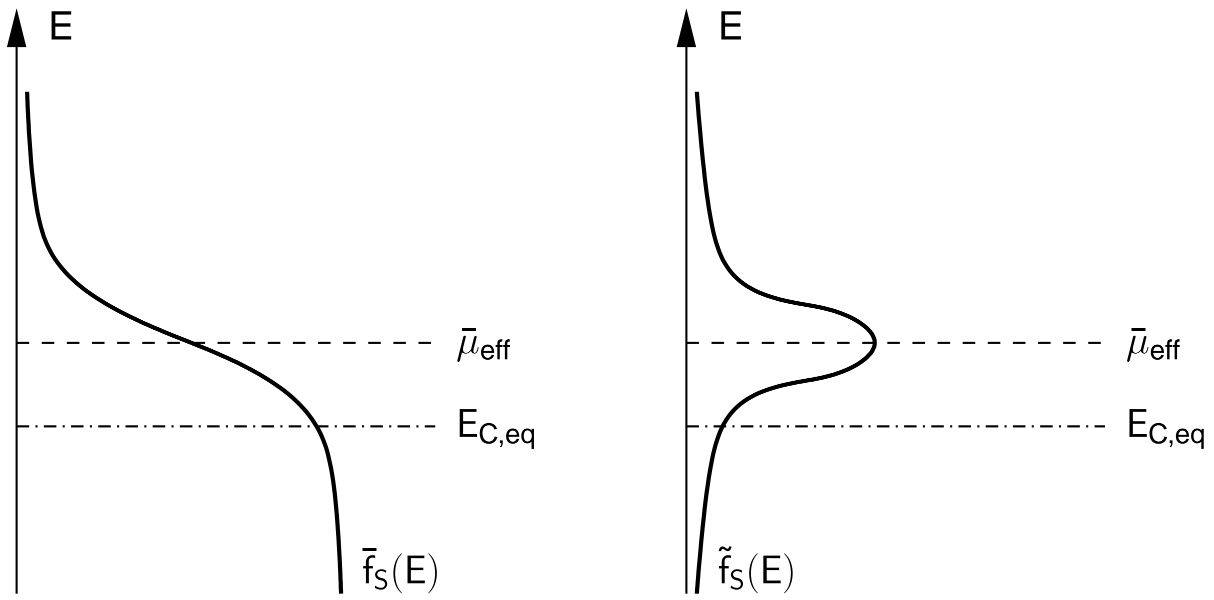


(a)



(b)

Figure 3



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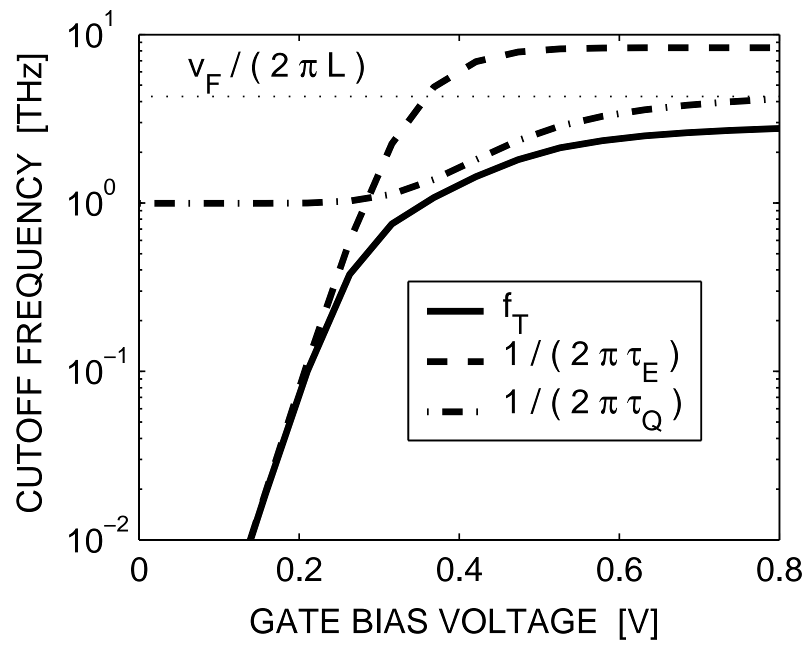
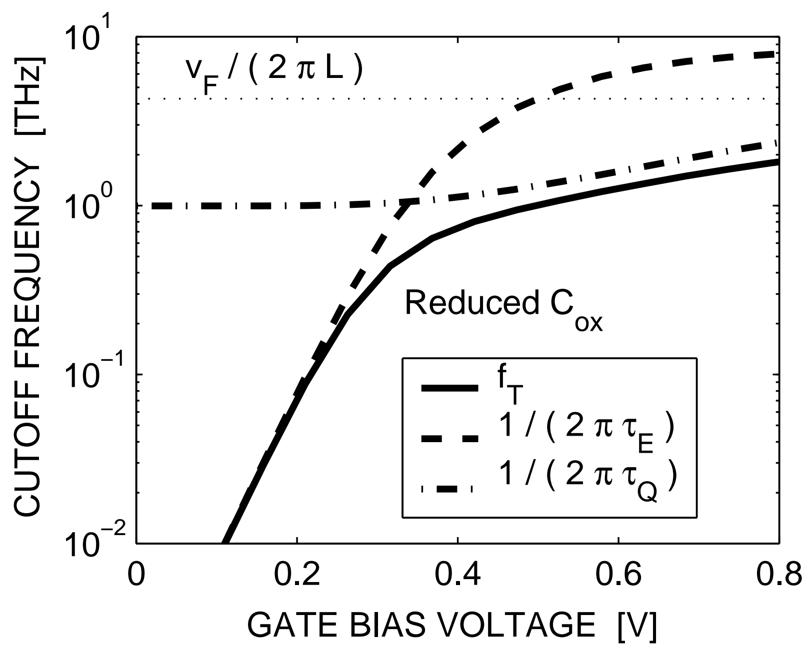


(a)



(b)

Figure 5

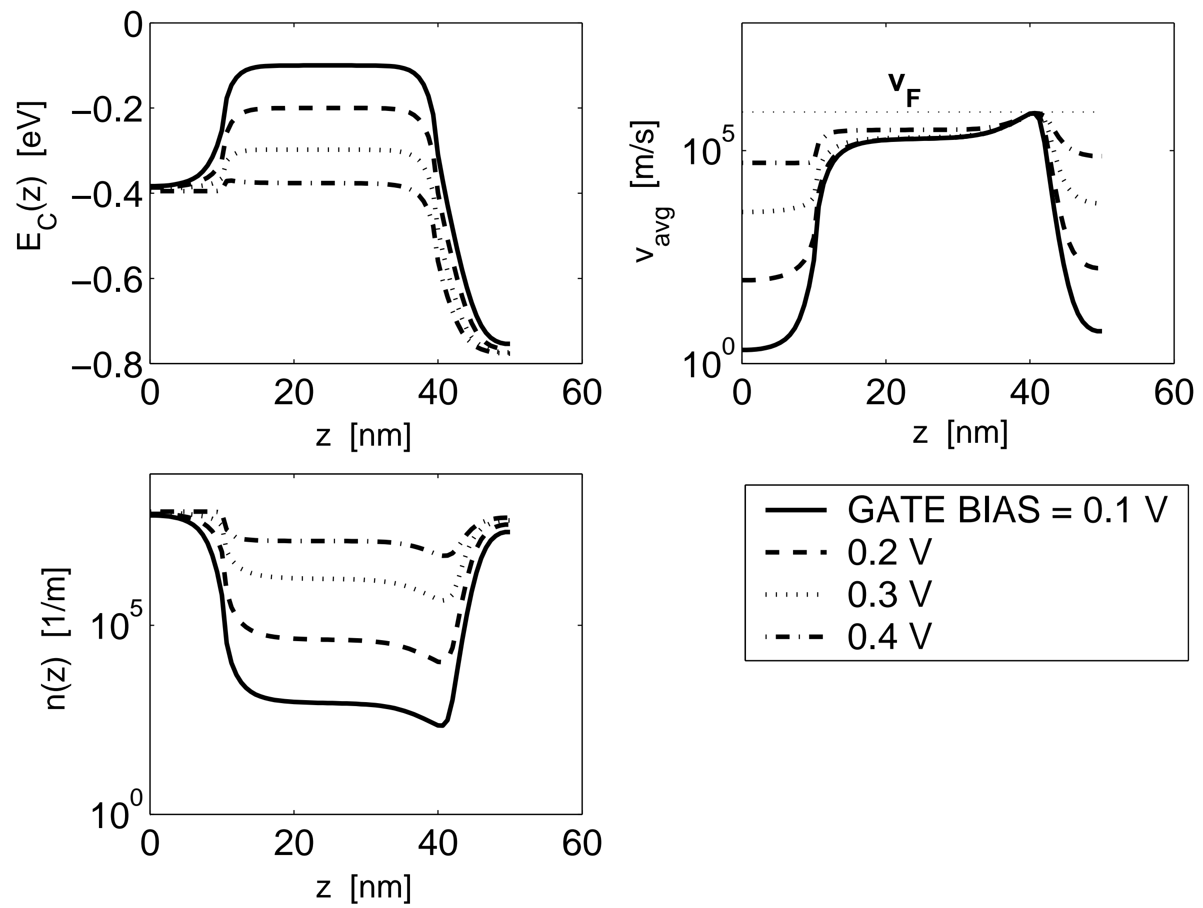


Figure 6

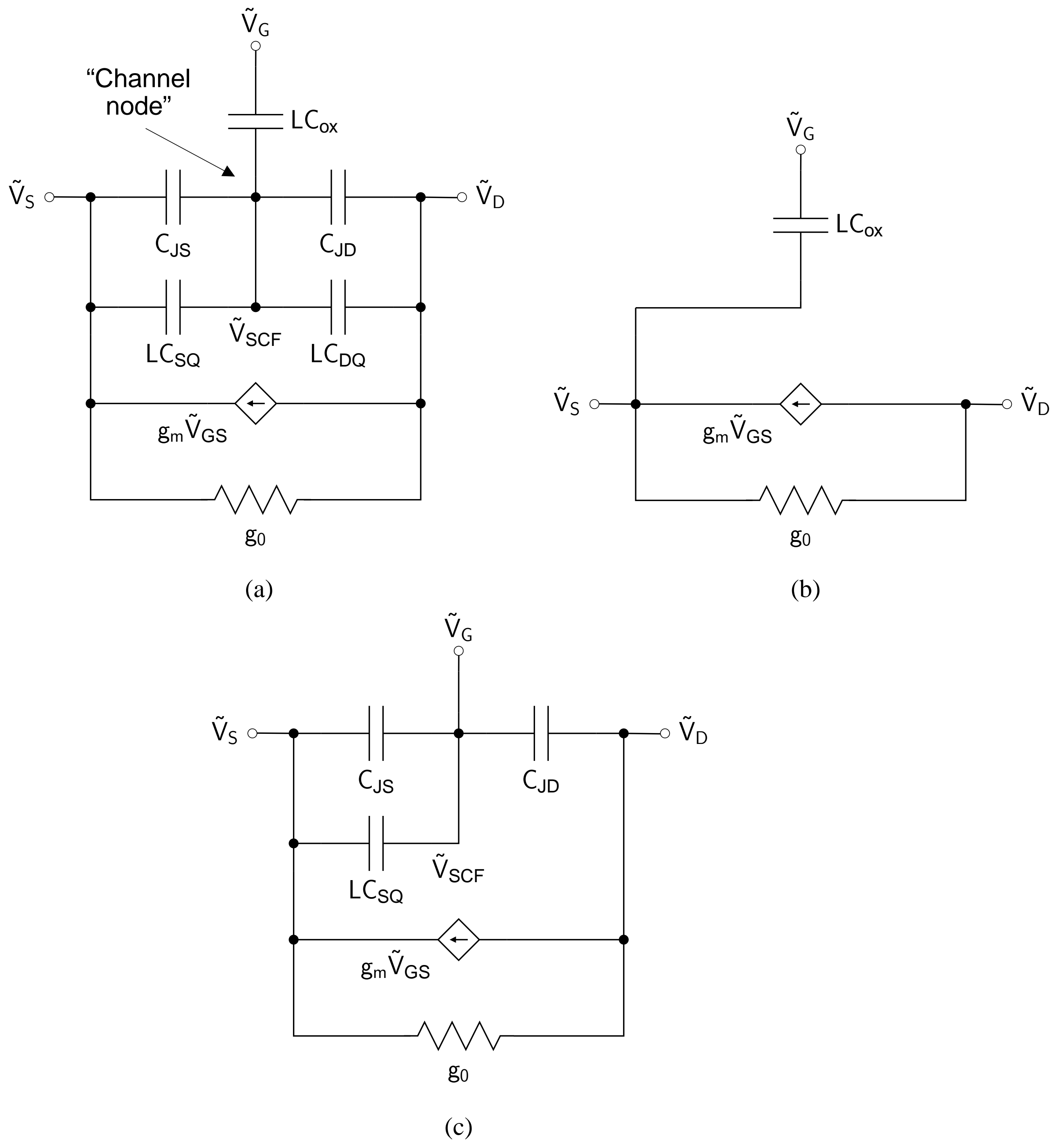


Figure 7

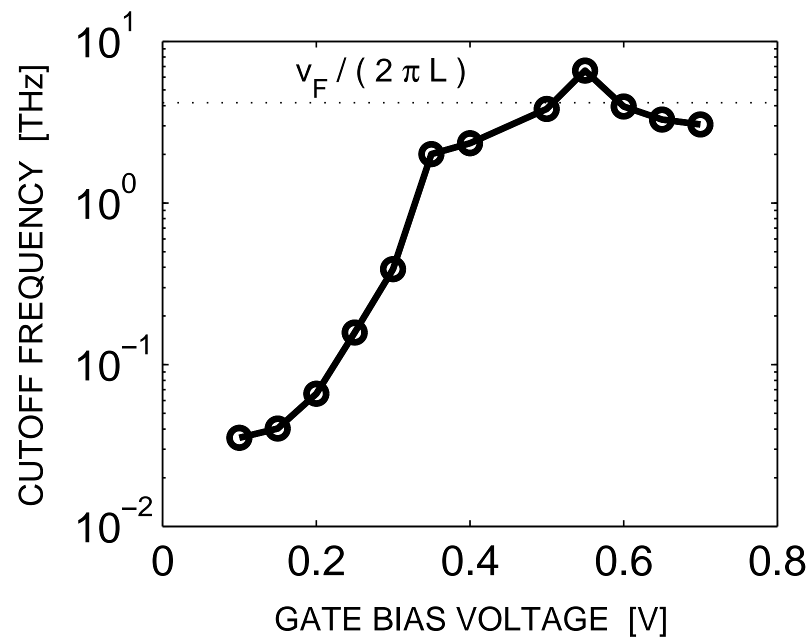


Figure 8