Universality of Off-State Degradation in Drain Extended NMOS Transistors

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Abstract

Off-state degradation in drain extended NMOS transistors is studied. It is shown that the damage is primarily due to Si-O bonds broken by hot carriers. These hot carriers are generated through impact ionization of surface band-to-band tunneling (BTBT) current. The resultant degradation is found to be universal, enabling reliability projections at lower stress voltages and based on shorter duration tests, than previously anticipated.

Introduction

While the scaling of channel length (L_C) and supply voltage (V_D) of logic/memory transistors have followed Moore's law since 1980s, the specification of I/O transistors that interfaces the IC to outside world, have not. And such non-classical transistors (*e.g.*, LDMOS, DeMOS, *etc.* [1-3]) poise unique reliability challenges that can neither be reduced to uncorrelated combination of HCI, NBTI, or TDDB concerns of core transistors, nor can be understood in terms of classical theories [4]. This makes reliability projections of I/O transistors difficult and perhaps unnecessarily conservative.

In this paper, we establish a systematic theory of universality of off-state degradation in Drain extended NMOS transistors (DeNMOS) as an illustrative example of non-classical, but predictable degradation in I/O transistors. Basic device structure of the DeNMOS transistor used in our study is shown in Fig. 1. Although the performance and cost advantage of DeNMOS are obvious (*i.e.,* no additional mask, LDD allowing high-voltage operation, *etc.*), its reliability is not. It has been hypothesized that off-state stress ($V_G = 0V$, high V_D) generates hot carriers by impact ionization (II) of leakage currents (possible candidates: sub-threshold (I_{SD}), substrate ($I_{B,leak}$), edge-tunneling (I_{EDT}), or surface band-to-band tunneling (I_{BTBT}), see Fig. 2). The injection of these hot carriers damages the oxide and leads to gate dielectric breakdown (TDDB) [5,6]. The hypothesis does not specify the *nature, location, and voltage dependence* of the damage. Through series of experiments and well calibrated MEDICI [7] and SMC [8] simulations, we establish for the first time that I_{BTBT} dictates the off-state reliability of DeNMOS by generating the hot holes responsible for breaking the Si-O bonds within the oxide. This degradation is universal, allowing reliability projection at lower V_D and with shorter test time than previously possible.

The origin of hot carrier in off-state DeNMOS

To determine the dominant leakage responsible for generation of hot-carriers at off-state (*i.e.,* $V_G = 0V$; $V_D >$ 5V), we measured the drain current (I_D) under various configurations (Fig. 3). Note that I_D for standard 4T ($I_{D,4T} = I_{SD}+I_{B,leak}+I_{EDT}+I_{BTBT}$) and 3T (source floating, $I_{D,3T} = I_{B,leak}+I_{EDT}+I_{BTBT}$) configurations are identical and is higher than the I_D in 2T (gate & source floating, $I_{D,2T} = I_{B,leak}$) configuration, ruling out I_{SD} and $I_{B,leak}$ as possible sources of hot carrier degradation (HCI). The edge tunneling (I_{EDT}) was found to be much less compared to the net drain current (data not shown) and hence does not contribute significantly to generation of hot carriers. Moreover, since I_D in 3T configuration is insensitive to V_D and V_G so long V_{DG}=const. (Fig. 3, voltage-splitting method [5]; 3T+VS) and since 2T measurements reduces I_D significantly, *we conclude that bulk*

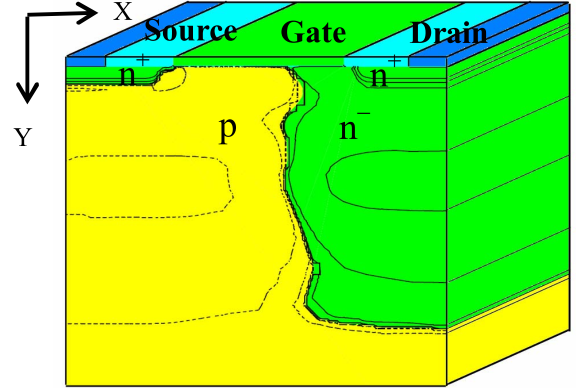


Fig. 1. Device structure of drain extended NMOS transistor.

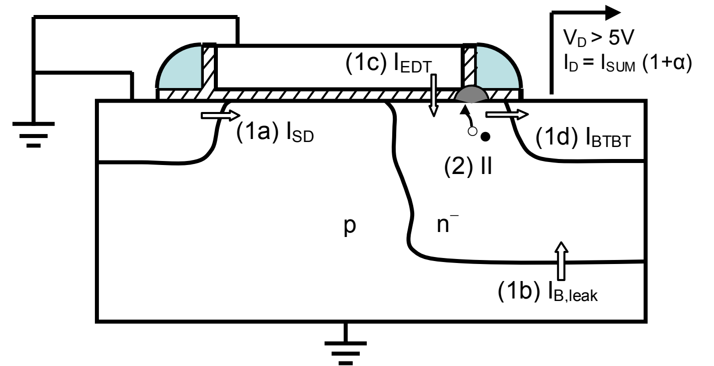
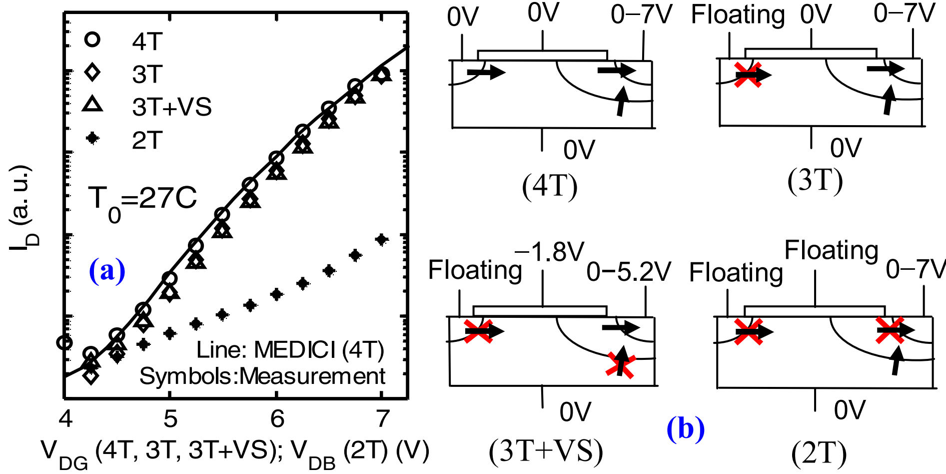


Fig. 2. Current components in DeNMOS device in off-state. (1a) Sub-threshold leakage, I_{SD} (1b) Bulk leakage, $I_{B,leak}$ (1c) Edge tunneling, I_{EDT} (1d) Surface BTBT, I_{BTBT}. Hot carriers generated by impact ionization of BTBT current (rate α; step 2; electrons represented by the filled circle and holes by the empty circle) eventually damage the oxide (shaded region).



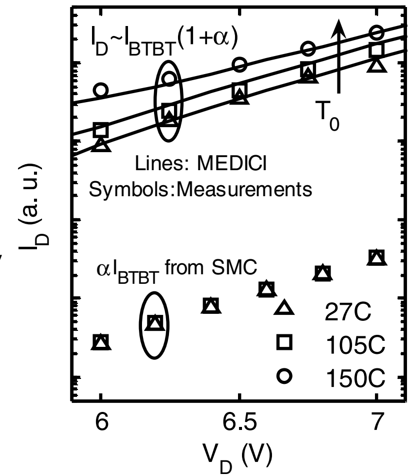


Fig. 3. (a) I_D measurement for various configurations to identify the dominant current component. (b) Current components for individual configuration: Active components are indicated by the arrows and inactive components are crossed out. The same value of off-state I_D (*e.g.*, $V_G = 0V$, $V_D > 5V$) for all configurations except 2T indicate a surface field initiated BTBT as the dominant current component, responsible for HCI damage of DeNMOS transistors.

Fig. 4. I_D measurement at various temperatures identifies relative contributions from BTBT and II. BTBT, being phonon assisted process, has a +ve T_0-dependence while a weak T_0-dependence is expected for II. Net +ve T_0-dependence indicates dominant BTBT contribution. II current from SMC is much less compared to net current.

BTBT plays no role determining hot carriers in DeNMOS. Therefore we attribute the increase in $I_D(V_D)$ to surface field initiated I_{BTBT}, *i.e.*, $I_D \sim (1+\alpha) I_{BTBT}$. The magnitude of α (responsible for the hot carriers, αI_{BTBT}) was estimated by measuring I_D at various temperatures, T_0 (Fig. 4). The positive T_0-coefficient indicates the number of hot carriers generated by II is small ($\alpha \ll 1$), a conclusion supported by extensively calibrated MC-based SMC simulations (Fig. 4). Finally, MEDICI simulation locates the maximum field near the surface and under the gate edge (Fig. 5 shows 2D field; Fig 6 shows 1D field close to the interface), consistent with the surface field initiated BTBT and impact ionization determined by experiments above.

Location/Nature of N_{IT}

With surface I_{BTBT} identified as the dominant source for hot-carriers, lateral charge pumping (CP) measurements [9] were used to find the *location* and *nature* of generated $N_{IT}(x,V_D)$. Our measurements locate the peak of $N_{IT}(x,V_D)$ (co-located with peak of E-field) just outside the gate overlap. This is also consistent with the location of hot hole and electron density computed by SMC simulation (Fig. 7 shows

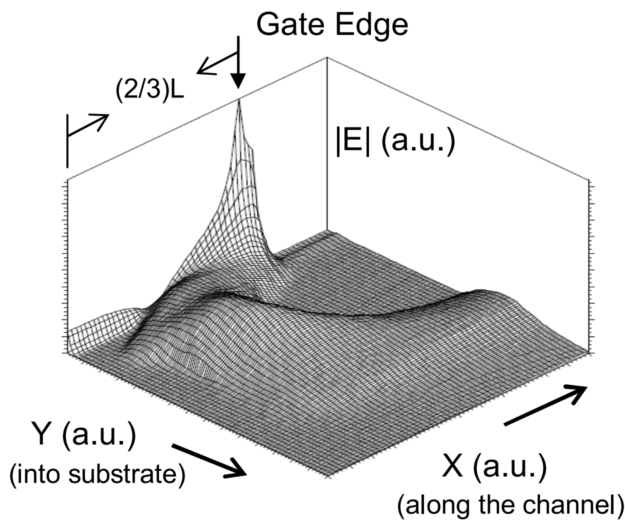


Fig. 5. 2D electric field profile obtained from MEDICI simulation (V_D=8V). The electric field peaks at the gate edge, close to the interface. The BTBT and subsequent II are expected to occur at the peak electric field region. L denotes the channel length.

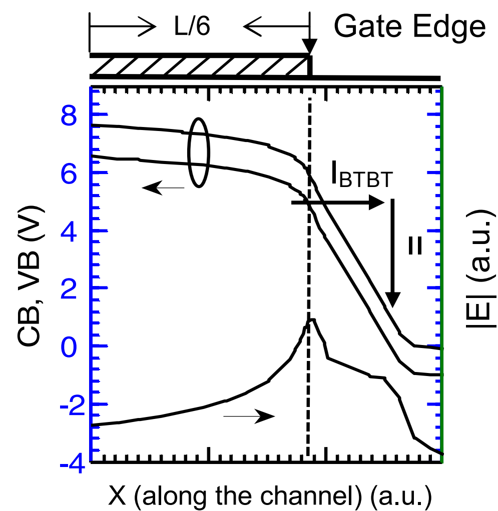


Fig. 6. Conduction and Valence band profiles and electric field along a 1D cut close to the interface (see Fig. 5). The BTBT and II processes are also shown schematically.

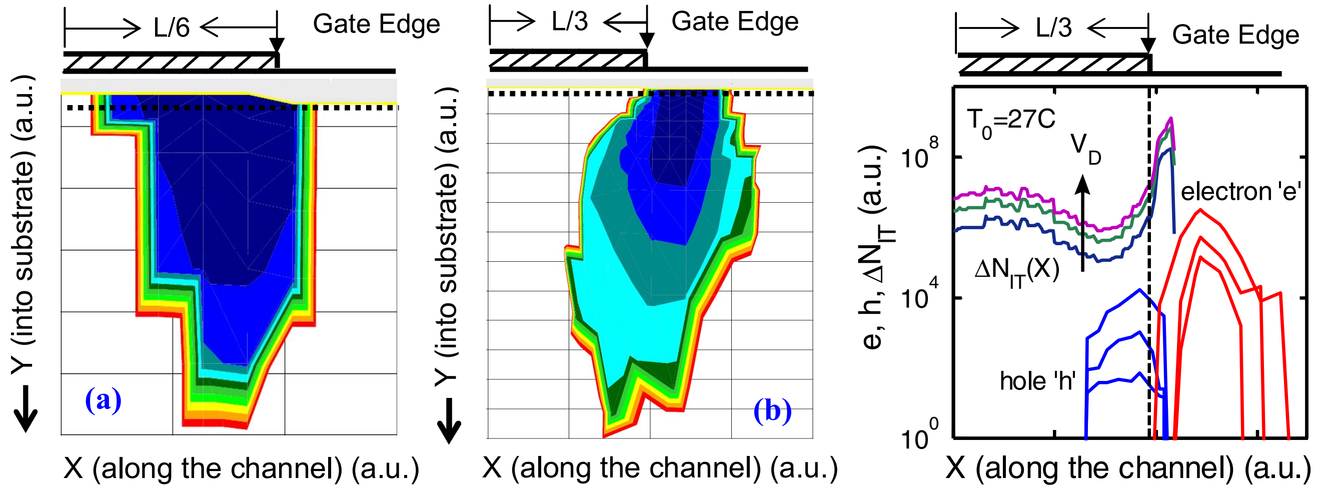


Fig. 7. (a) 2D hot hole (E>4.7eV) and (b) hot electron (E>3.1eV) profiles obtained from SMC (V_D=8V). Peak hot carrier density occurs close to the gate edge. Hot carrier density along the 1D cut (dotted line) close to the interface is shown in Fig. 8.

Fig. 8. Hot electron and hole densities along a 1D cut close to the interface (see Fig 7). $\Delta N_{IT}(X)$ after 1000s stress, obtained from CP measurement, is also plotted. Peak damage occurs near the gate edge and correlates well with the location of spatial overlap of hot carries.

2D hot carrier profile; Fig. 8 shows profile along a 1D cut along with measured $N_{IT}(x,V_D)$). Classical theory correlates HCI damage to broken Si-H bonds [10, 11], yet the following features of the degradation strongly suggest that the origin of N_{IT} in off-state are broken Si-O bonds and not Si-H: (a) high initial time exponent ($\Delta N_{IT} = At^n$; n~0.72-0.88, Fig. 9a) that is inconsistent with dissociation of Si-H bonds and subsequent diffusion of H away from the interface [11], (b) absence of recovery of the CP-current during the relaxation phase [12] following off-state stress (Fig 9b), and (c) correlation of $N_{IT}(V_D)$ from experiments and hot holes $h(V_D$; E>4.7eV) from SMC simulation (implicating the hot holes as the precursor to N_{IT} damage) (Fig 9c) [13, 14]. This distinction of N_{IT} between Si-O and Si-H bonds is important for the lifetime estimation of devices, as it dictates the time exponent of degradation, the recovery behavior on removal of the stress conditions, and voltage and temperature acceleration factors for degradation.

Universal degradation curve/Voltage acceleration

One of the most striking features of the off-state degradation in drain extended devices is the universal nature of the time evolution of interface traps, $\Delta N_{IT}=\xi(t/T(V_D))$ [15]. Individual degradation curves for various stress drain biases can be scaled laterally (in log-log scale, scaling factor $S(V_{D2},V_{D1})\equiv T(V_{D1})/T(V_{D2})$) so that they form a universal degradation curve as shown in Fig. 10. This universality of $N_{IT}(t,V_D)$ appears to be consistent with Bond-Dispersion model [16] and a simulation with a spread in bond energies (σ = 0.1eV) could successfully model the shape of the observed universal curve. The long term degradation curve for individual biases can be constructed by knowing the shape of

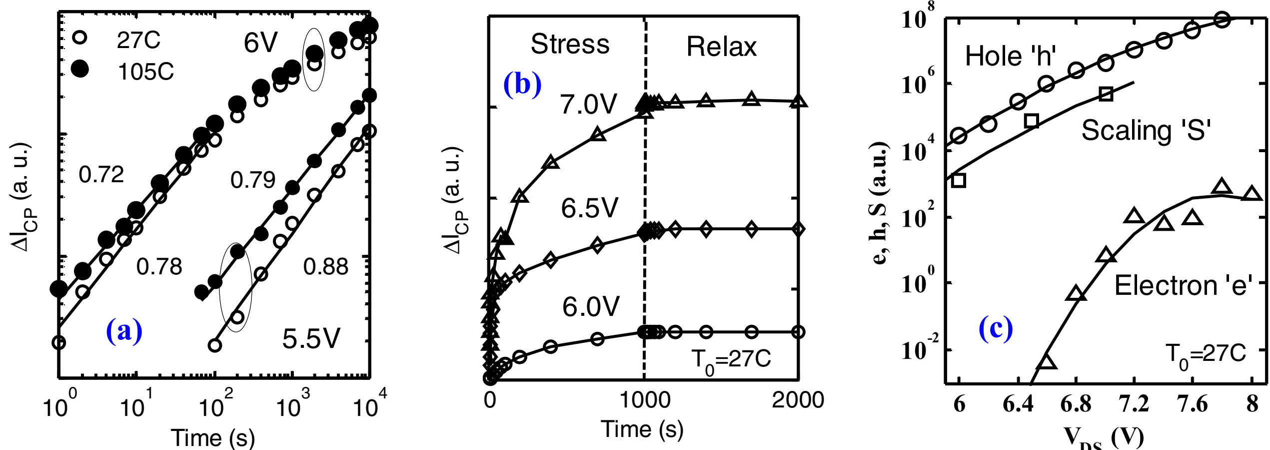
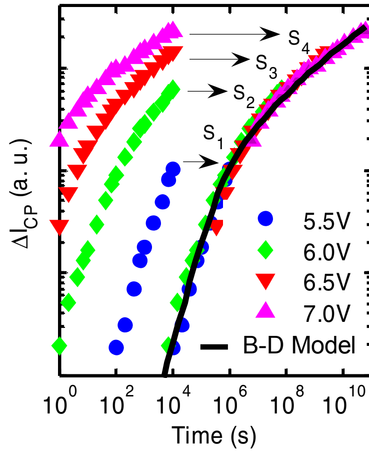


Fig. 9. Time evolution of ΔI_{CP} during (a) stress phase and (b) consecutive stress and relaxation phases. The high initial time exponent in Fig. 9(a) ($\Delta I_{CP}=At^n$; n=0.72-0.88) during stress and lack of recovery during relaxation (Fig. 9(b), t > 1000s) suggest Si-O bond breaking and not Si-H. (c) Integrated hot hole (E>4.7eV; circles) and electron (E>3.1eV; triangles) densities underneath the gate for various stress V_D obtained from SMC (see Fig. 8). The scaling factors (squares) used to compute the universal curve (Fig 10) are also plotted and show good correlation with the computed hot hole density.

the universal curve and the corresponding scaling factors, as shown in Fig. 11. Long time measurement (400ks) at a single V_D is found to follow the degradation curve thus constructed and independently validates the universal nature of the degradation.

Indeed, since $T(V_D) \propto S(V_D)^{-1}$ (Fig. 11), thus $d\ln(T)/dV_D = -d\ln(S)/dV_D$, which implies that universality of degradation allows one to replace the time-consuming measurement of $d\ln(T)/dV_D$ by easy and short measurements of $d\ln(S)/dV_D$. Fig. 12 shows the voltage acceleration of off-state degradation obtained using the scaling factors $S(V_D)$. Thus, the universal nature of degradation provides a powerful algorithm to predict device degradation at lower V_D and shorter stress times than previously possible.

Moreover, the interface trap generation and hot hole density are correlated such that $S(V_D) \propto h(V_D)$ (Fig. 12). Hence, one may simply use the simulation of $h(V_D)$, coupled with a single measurement of $\Delta N_{IT}=\xi(t/T)$ to predict off-state DeNMOS reliability at all operating conditions!



Fig, 10. To prove that shape of degradation is universal, experimental data for various stress V_D (T_0=27C) are shifted laterally by scaling factor 'S'. The resultant curve is universal! Bond dispersive (B-D) model (σ=0.1 eV [16]) interprets the saturation of the universal curve.

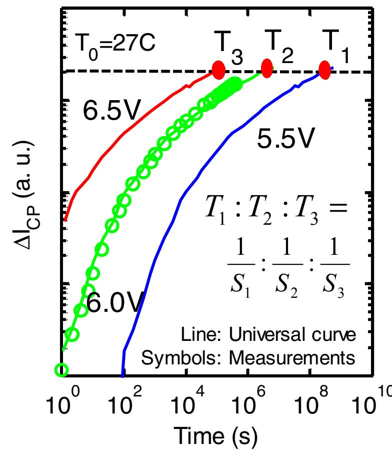


Fig. 11. Degradation curves for individual V_D obtained by shifting back the universal curve (Fig 10). To independently validate the universal curve, long time measurement (400ks) at V_D=6.0V was taken and was found to follow the predicted curve.

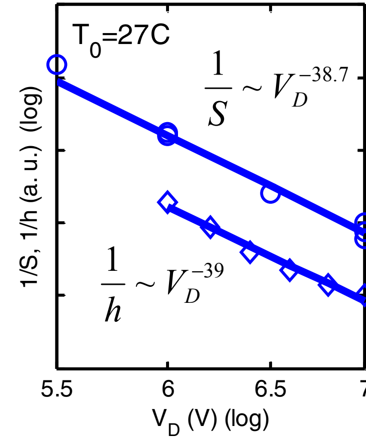


Fig. 12. Voltage acceleration (γ) for scaling factors (S; from measurements, circles) and hole density (h; from SMC simulation, diamonds). Due to similar γ, a single measurement for $\xi(t/T)$ along with simulated $h(V_D)$ is sufficient to predict the degradation for any given bias.

Conclusion

Our study of DeNMOS articulates the first systematic theory of off-state degradation of these non-classical I/O transistors. Specifically, we demonstrate that (1) hot carriers responsible for eventual oxide damage originate exclusively from surface BTBT leakage, (2) contrary to popular belief, N_{IT} consists of mostly broken Si-O bonds, rather than Si-H bonds, and most importantly, (3) the time-evolution of $N_{IT}(t,V_D)$ is universal, enabling reliability extrapolation at lower V_D and based on shorter-duration tests than previously presumed possible.

Acknowledgement: We gratefully acknowledge Texas Instruments for supporting the research, Jeff Bude for providing SMC simulator, and the Network of Computational Nanotechnology for the computational facilities.

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