

Theory of Interface-Trap-Induced NBTI Degradation for Reduced Cross Section MOSFETs

Haldun Küflüoğlu, *Student Member, IEEE*, and Muhammad Ashraful Alam, *Fellow, IEEE*

Abstract—Negative Bias Temperature Instability (NBTI)-induced degradation for ultra-scaled and future-generation MOSFETs is investigated. Numerical simulations based on Reaction–Diffusion framework are implemented. Geometric dependence of degradation arising from the transistor structure and scaling is incorporated into the model. The simulations are applied to narrow-width planar triple-gate and surround-gate MOSFET geometries to estimate the NBTI reliability under several scaling scenarios. Unless the operating voltages are optimized for specific geometry of transistor cross section, the results imply worsened NBTI reliability for the future-generation devices based on the geometric interpretation of the NBTI degradation. A time-efficient and straightforward analysis is developed to predict the degradation. This compact model confirms the numerical simulations.

Index Terms—CMOS reliability, FinFET, modeling, nanowire, narrow width, negative bias temperature instability (NBTI), surround gate, triple-gate, vertical replacement gate (VRG).

I. INTRODUCTION

NEGATIVE BIAS Temperature Instability (NBTI) is one of the degradation mechanisms that generate traps at the Si-channel/gate-oxide interface of MOSFETs during transistor operation. The semiconductor/oxide interface is a rough surface where the highly ordered crystalline channel and the amorphous SiO₂ dielectric meet. At the junction of these dissimilar materials, some of the Si atoms from the channel remain dangling without satisfied chemical bonds, thus, forming the interface traps. The traps lead to poor device performance; therefore, the transistors are annealed in hydrogen ambient during the manufacture. The hydrogen gas diffuses into the gate-oxide and yields passivated Si bonds, as shown in Fig. 1. The hydrogen-annealing technique has provided a viable solution to the interface-trap instabilities for decades; however, recent scaling trends and processing modifications have brought NBTI into attention. Technologically, the trend towards the surface-channel MOSFETs, slow reduction in supply voltages compared to aggressive gate-oxide scaling for higher performance, and the introduction of nitrided oxides to prevent boron penetration from the poly-gate are increasing the NBTI-induced dissociation of the Si–H bonds at the Si/oxide interface [1], [2].

Manuscript received July 5, 2005; revised November 11, 2005. This work was supported in part by the National Science Foundation (NSF) and in part by the Semiconductor Research Corporation (SRC). The review of this paper was arranged by Editor G. Groeseneken.

The authors are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907-1285 USA (e-mail: kufluoglu@purdue.edu).

Digital Object Identifier 10.1109/TED.2006.872098

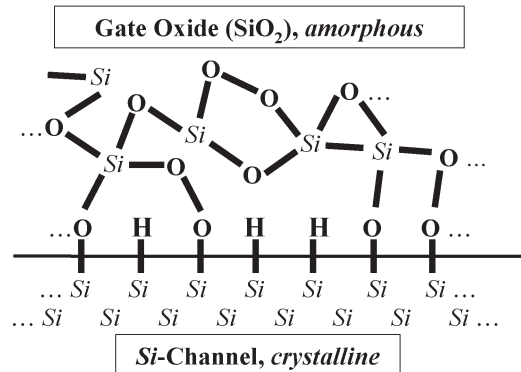


Fig. 1. Schematic of the Si/oxide interface of a MOSFET. The dangling Si bonds are present due to the mismatch between the ordered channel and amorphous oxide. These act as interface traps unless they are passivated by hydrogen annealing. NBTI induces the dissociation of the Si–H bonds causing hydrogen to diffuse away from the interface.

Thus, NBTI poses significant parametric reliability concerns for digital and analog CMOS circuits [3]–[7].

In NBTI, the Si–H bond breaking is triggered in negatively biased ($V_G < 0$ V, $V_S = V_D = 0$ V) PMOSFETs at elevated temperatures present either due to power dissipation from the circuits or due to ambient temperature that the IC operates in. The inversion layer holes tunnel to and are captured by the Si–H bonds at the interface [8], [9]. This weakens the bond and the subsequent thermally assisted dissociation of a Si–H pair yields one donor-like interface trap (i.e., silicon dangling bond) and one H atom that can diffuse in the oxide [10]–[13].

Present-day operation conditions of circuits favor significant NBTI related trap generation in PMOSFETs. The interface traps shift the threshold voltage of MOSFETs, diminish carrier mobility, and add to parasitic capacitances, overall, reduce the drain current of the devices. In NBTI, the interface-trap density increases over time in a characteristic power-law behavior ($\sim t^{0.25}$), and eventually threatens the operational lifetimes of the transistors and the circuits. Therefore, understanding the NBTI degradation is of primary importance for existing and near-future technologies. The experimental characterization period of the device reliability is very short compared to the desired lifetime (e.g., few weeks for the former, about ten years for the latter) of a transistor. For a given technology generation, accelerated characterization tests with higher voltages and temperatures with respect to the operating conditions are performed, and the results are projected to the long device lifetimes. However, the NBTI degradation under the accelerated test conditions and the operating conditions can vary; therefore

such extrapolations are meaningful only with well-calibrated physics-based reliability models.

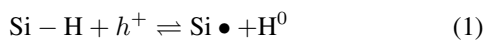
A realistic NBTI model should also explain the degradation for future-generation transistors. Current technology node involves planar MOSFETs with considerably large dimensions along the width direction of the transistors. However, going down the technology roadmap, alternative device geometries, such as narrow-width planar transistors, FinFET/triple-gate MOSFETs, and surround-gate structures, such as vertical replacement gate (VRG) and nanowire transistors, are considered for high-density and high-performance circuits [14]. Extrapolation of the NBTI reliability from the existing MOSFET generations to the ultra-scaled future technologies may lead to erroneous device lifetimes since the scaling of the dimensions and the structural changes can alter the degradation rates of the transistors. In order to fully evaluate the promises of such next-generation transistors, a solid prediction methodology that can extend the current NBTI characterization techniques to future technologies is needed.

The Reaction–Diffusion (R–D) model has provided the theoretical interpretation of the NBTI phenomena. Indeed, this model has successfully interpreted the: 1) robust fractional power exponent [15], 2) activation energies [16], 3) relaxation dynamics [12], 4) frequency dependence, 5) isotope effect [17], and 6) lock-in mechanism [18]. Moreover, recently, a unified model based on the R–D theory that explains the time evolution of NBTI and hot carrier injection (HCI)-induced interface trap generation is suggested [19]. Numerical simulations based on the R–D framework, as well as analytical calculations, show that both the device geometry and the geometry of the degradation can alter the time behavior of the trap-generation rate. In this paper, we extend the geometric interpretation of the R–D model to predict the NBTI reliability for ultra-scaled narrow-width planar, triple-gate, and nanowire MOSFETs and VRG transistors. In Section II, we summarize the geometry-dependent R–D model and introduce a straightforward analysis method to capture the effective trends of scaling such device structures. Finally, in Section III, we compare the numerical R–D simulation results with the analysis developed. These formulas can be used to quickly estimate the reliability performance of a device for specific operating conditions without the need for relatively time-consuming simulations.

II. GEOMETRY DEPENDENT R–D MODEL

A. Analytical Calculations

The R–D framework considers the bond breaking at the interface as a chemical reaction as in (1) [12], [13]



where the interaction of a hole h^+ with the Si–H bond results in a donor-like interface trap and a free H that can diffuse away from the interface or passivate a Si dangling bond. The trap density (N_{IT}) increases with the net reaction given in (2)

$$\frac{dN_{\text{IT}}}{dt} = k_f(N_0 - N_{\text{IT}}) - k_r N_{\text{IT}} N_H^{(0)} \quad (2)$$

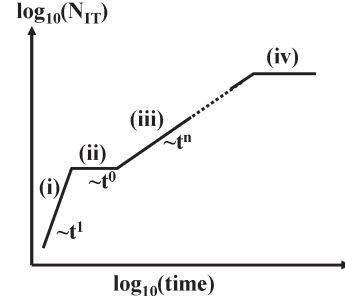


Fig. 2. Schematic of time evolution of the classical R–D model. Regions: (i) generation-limited, (ii) dynamic equilibrium, (iii) diffusion-limited, and (iv) saturation. Region (iii) gives the power-law behavior for NBTI. The degradation in the first two regions is very quick and not observable in experimental measurements.

where k_f and k_r are the bond-breaking and bond-annealing rates in (1), respectively. N_0 is the Si–H bond density available prior to degradation, and $N_H^{(0)}$ is the density of hydrogen at the Si/oxide interface. At the beginning of the stress, both N_{IT} and $N_H^{(0)}$ are negligible ($N_0 \gg N_{\text{IT}}$), and so is the second term in the right side of (2), therefore the increase in N_{IT} is generation-limited, as shown in region (i) ($N_{\text{IT}} \sim t^1$) of Fig. 2. The reaction later reaches a dynamic equilibrium state in region (ii) ($N_{\text{IT}} \sim t^0$) when the annealing term of (2) becomes comparable to the generation term. After sufficient buildup of hydrogen near the semiconductor/oxide interface, the diffusion of H into the oxide begins to dominate, so the net reaction rate becomes limited to the hydrogen diffusion in region (iii) ($N_{\text{IT}} \sim t^n$) of Fig. 2, and gives the characteristic time evolution of the NBTI degradation. Here, the hydrogen diffusion obeys (3)

$$\frac{dN_H}{dt} = D_H \nabla^2 N_H \quad (3)$$

where D_H is the diffusion constant of hydrogen. Eventually, in region (iv), all the Si–H bonds are broken ($N_{\text{IT}} = N_0$), so that the trap density saturates. Based on (2) and (3), which encapsulates the R–D model, it is clear that the temperature and field dependence of the degradation phenomena are not considered explicitly in the R–D model. Rather the oxide-field dependence of the degradation phenomena is incorporated in the factor k_f , and the temperature dependence is included through activation energies of k_f , k_r , and D_H . The rates k_f and k_r that contain the microscopic details of the bond breaking and annealing are effective parameters.

The time exponent n of the interface trap generation can be obtained by solving (2) and (3) simultaneously subject to appropriate boundary conditions of the device geometry. However, before we consider the NBTI degradation for narrow-width or surround-gate devices numerically, it is instructive to consider the problem analytically. For a finite-size device, the hydrogen diffusion will first begin as one-dimensional (1-D) diffusion in bulk of the oxide. Over time, however, the diffusion through the edges will become increasingly important making the diffusion a two-dimensional (2-D) problem and, eventually, when the diffusion radius becomes much larger than the gate area of the device, the diffusion becomes three-dimensional (3-D). Before we discuss this transformation of the diffusion

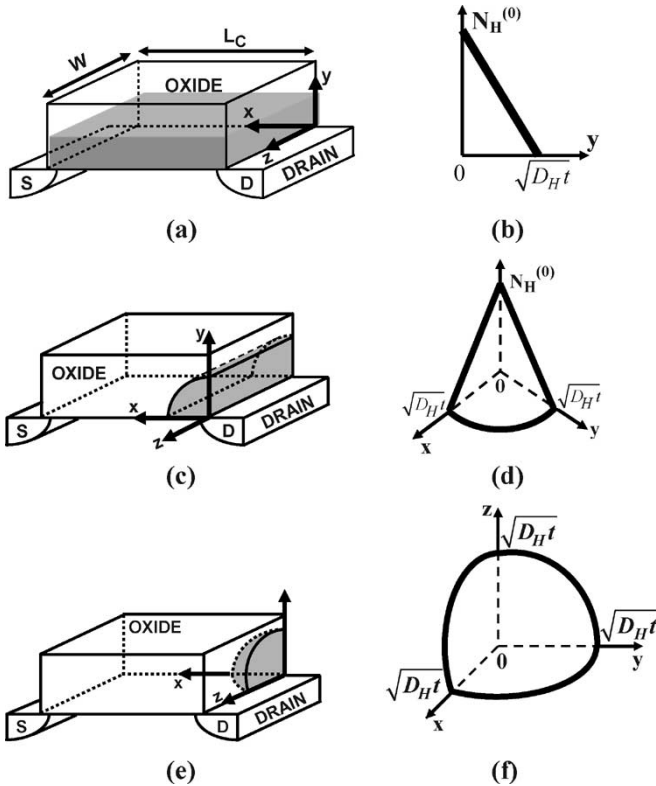


Fig. 3. 1-D, 2-D, and 3-D diffusions of hydrogen are illustrated in the gate oxide of planar MOSFETs. Shaded regions in (a), (c), and (e) represent hydrogen. (a) NBTI trap distribution is uniform over the channel, (b) hydrogen profile for 1-D diffusion, (c) and (d) degradation near the edge and 2-D diffusion profile, (e) degradation localized at a point, and (f) 3-D hydrogen-diffusion profile.

problem from 1-D to 2-D to 3-D as a general problem, we first look at the asymptotic limits of these diffusion cases individually.

B. Asymptotic Diffusion in 1-D, 2-D, and 3-D

One can readily estimate the exponent in diffusion-limited region by using the fact that every free H is associated with one interface trap from (1), i.e., $N_{IT}(t) = \int N_H(r, t) d^3r$. The release rate of hydrogen at the Si/oxide interface is much higher than the diffusion velocity, and the hydrogen profile broadens as $(D_H t)^{0.5}$ into the oxide. In NBTI, assuming the hydrogen profile in Fig. 3(b) due to the 1-D nature of hydrogen diffusion

$$N_{IT}(t) = \int_0^{\sqrt{D_H t}} N_H^{(0)} \cdot \left(1 - \frac{y}{\sqrt{D_H t}}\right) dy \quad (4)$$

$$= \frac{1}{2} N_H^{(0)} \sqrt{D_H t}. \quad (5)$$

The dN_{IT}/dt term is negligible (although it is still time dependent; see Appendix A for discussion) compared to the other two terms in (2), therefore (2) can be simplified as

$$N_{IT} \cdot N_H^0 = \frac{k_f N_0}{k_r}. \quad (6)$$

Substituting $N_H^{(0)}$ from (5) into (6), we obtain

$$N_{IT}^{1-D}(t) = \sqrt{\frac{k_f N_0}{2k_r}} \cdot (D_H t)^{0.25}. \quad (7)$$

Similarly, for 2-D diffusion from a line source, the hydrogen profile can be assumed as in Fig. 3(d), and repeating (4)–(6) in (8) and (9) gives (10)

$$N_{IT}^{2-D}(t) = \frac{1}{4} \cdot \int_0^{\sqrt{D_H t}} N_H^{(0)} \cdot \left(1 - \frac{r}{\sqrt{D_H t}}\right) 2\pi r dr \quad (8)$$

$$= \frac{\pi}{12 \cdot W} N_H^{(0)} (D_H t) \quad (9)$$

$$N_{IT}^{2-D}(t) = \sqrt{\frac{\pi k_f N_0}{12 \cdot W \cdot k_r}} \cdot (D_H t)^{0.5}. \quad (10)$$

Finally, the diffusion from a point source, as illustrated in Fig. 3(c), is of 3-D and, applying the same procedure through (11) and (12), the R–D model predicts (13) assuming the hydrogen profile shown in Fig. 3(f)

$$N_{IT}^{3-D}(t) = \frac{1}{8} \cdot \int_0^{\sqrt{D_H t}} N_H^{(0)} \cdot \left(1 - \frac{r}{\sqrt{D_H t}}\right) 4\pi r^2 dr \quad (11)$$

$$= \frac{\pi}{24} N_H^{(0)} (D_H t)^{\frac{3}{2}}. \quad (12)$$

Using (6) and (12), we find

$$N_{IT}^{3-D}(t) = \sqrt{\frac{\pi k_f N_0}{24 \cdot k_r}} \cdot (D_H t)^{0.75}. \quad (13)$$

The above estimates show that regardless the physics of k_f , k_r , and D_H , the R–D model predicts that the geometry of the problem determines the rate of interface trap generation (n , the time exponent), and this rate increases with the dimension of the hydrogen diffusion. The NBTI time dependence is governed by the slower diffusion process, therefore relatively small distribution (spread of about 0.1 eV and mean energy of 2.8 eV from [20]) in the activation energies of k_f and k_r does not affect the time exponent appreciably [21].

C. Diffusion Length, λ_D , and Finite-Size Effects

The discussion in the previous section is based on the idealized assumption that for 1-D diffusion, the x – z plane [Fig. 3(a)] has an infinite extent, similar for 2-D diffusion; the assumption is that the length of the cylinder is infinite, and that for 3-D diffusion, the source is a geometrical point. In reality, of course, since the channel dimensions of a MOSFET are finite, they can affect the degradation rates of NBTI. In this section, we include these additional geometrical considerations and show that one can derive the corresponding rates. The effect of the geometry of hydrogen diffusion on degradation

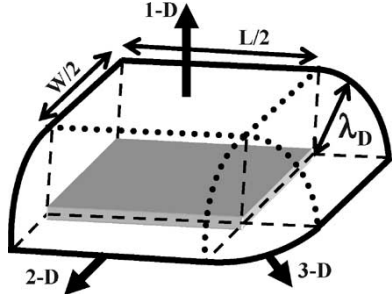


Fig. 4. Diffusion of hydrogen from a planar semiconductor/oxide interface. The rectangular plate (shaded region) shows the degraded interface from which H is released. The wire frame represents the hydrogen profile. At the edges and corners, 2-D and 3-D profiles add to the volume occupied by hydrogen. As the structure is scaled, first the 2-D and then the 3-D components begin to dominate the volume. Due to symmetry, only one quadrant of the gate oxide is drawn.

rate can be analyzed with the concept of the diffusion length $\lambda_D = (D_H t)^{0.5}$. Fig. 4 depicts the diffusion of hydrogen from a planar degraded region. Over the region, the diffusion is of 1-D, however, at the edges, the hydrogen profile extends outward in a cylindrical form. At the corners, similarly, the diffusion becomes 3-D due to the finite dimensions of the degraded area. The exact volume occupied by the hydrogen contains the 1-D rectangular box, the 2-D cylindrical side regions, and the 3-D spherical corners. The volume used in the derivation of (7) assumes $W, L \gg \lambda_D$, but if the contribution of the edges and corners are considered, the trap density can be generalized into (14)

$$N_{IT}^{PL} = \sqrt{\frac{k_f N_0}{W L k_r}} \cdot \left[W \lambda_D \left(L + \frac{\pi \lambda_D}{2} \right) + \frac{2\pi \lambda_D^3}{3} \right]^{\frac{1}{2}} \quad (14)$$

(for detailed derivations of (14)–(16), see Appendix B). From (14), when L and $W \gg \lambda_D$ [Fig. 3(a)], $N_{IT} \sim t^{0.25}$ is obtained as in the case of NBTI time dependence in (7), and if only L is scaled, such that $L \sim \lambda_D$ [Fig. 3(c)], then $N_{IT} \sim t^{0.5}$. Furthermore, if $W, L \sim \lambda_D$, N_{IT} approaches $\sim t^{0.75}$ as in (13), signaling increased the degradation rates for aggressively scaled planar MOSFETs.

During the degradation, the hydrogen can diffuse into the Si channel, surrounding isolation or poly-gate. In this condition, the diffusion constant of hydrogen in other materials should be considered and D_H is replaced with the effective diffusion constant (e.g., $D_{\text{eff}} = D_H$ before the hydrogen reaches the poly-gate, $D_{\text{eff}} = D_{\text{POLY}}$ afterwards). The D_{Si} is about the same as D_H [22]. The technologically important poly-gates are highly doped, therefore the diffusion of hydrogen is not affected significantly by the grain boundaries [23]. The D_{eff} does not change the time exponent of NBTI except for brief transients when the hydrogen meets with the material boundaries. The diffusion length is modified accordingly, i.e., $\lambda_D \sim (D_{\text{eff}} t)^{0.5}$, and the geometry effect will still increase the degradation rate.

The Si/oxide interface roughness has a negligible effect on the geometry analysis in the R–D model. In modern MOSFETs, the roughness is at atomistic dimensions (few Å), which is much smaller compared to λ_D .

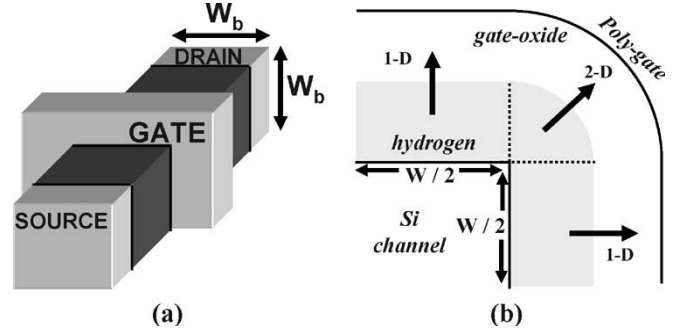


Fig. 5. (a) Schematic view of triple-gate MOSFET, and (b) cross section of the body of the transistor. The planar channels allow 1-D hydrogen diffusion in the dielectric; however, the corners of the triple-gate transistor add 2-D regions and enhance the overall diffusion rate. The effect is pronounced when the transistor is scaled. One quadrant of the cross section is shown due to symmetry.

The diffusion-length analysis can also be extended for nonplanar-MOSFET geometries. Fig. 5(a) shows the cross section of the body of a triple-gate transistor. The schematic in Fig. 5(b) reflects the hydrogen diffusion when NBTI is considered. The profiles over the three-planar channels are 1-D, but the corners contribute 2-D cylindrical volumes. Similar to the planar-MOSFET case, the degradation can be derived as (15) if the gate length is sufficiently long compared to λ_D

$$N_{IT}^{\text{TRI}} = \sqrt{\frac{k_f N_0}{W k_r}} \cdot \left[W \lambda_D + \frac{\pi \lambda_D^2}{4} \right]^{\frac{1}{2}} \quad (15)$$

When $W \gg \lambda_D$, (15) approaches (7) since the diffusion is mainly 1-D. The time exponent n increases as W is scaled and results in a higher degradation rate.

Another nonplanar structure is the surround-gate cylindrical MOSFET with channel radius R depicted in Fig. 6(a). For NBTI degradation, the hydrogen diffusion is confined within the distance $R < r < R + \lambda_D$, and shown as the cylindrical shell in Fig. 6(b). The interface-trap density can be calculated from the geometry-dependent R–D relation as

$$N_{IT}^{\text{CYL}} = \sqrt{\frac{k_f N_0}{R k_r}} \cdot \left\{ \lambda_D \left(1 + \frac{R}{\lambda_D} \right) (2R + \lambda_D) - \frac{1}{3} [R^2 + R(R + \lambda_D) + (R + \lambda_D)^2]^{\frac{1}{2}} \right\} \quad (16)$$

In the limit $R \gg \lambda_D$, the hydrogen diffusion is effectively of 1-D nature and the cylindrical channel resembles that of a planar MOSFET. Therefore, $N_{IT}(t) \sim t^{0.25}$ is obtained under NBTI stress. For $R \ll \lambda_D$, the hydrogen diffusing into the Si channel can be considered with the D_{eff} . Eventually, the density of hydrogen inside the channel will be equal (and still time dependent, inherently in the R–D model) to that of the Si/oxide interface, and the diffusion will only evolve outward in the radial direction. In this case, n approaches 1/2, as expected from (16). Similar to the narrow-width planar MOSFET, the time exponent increases with time for each radius.

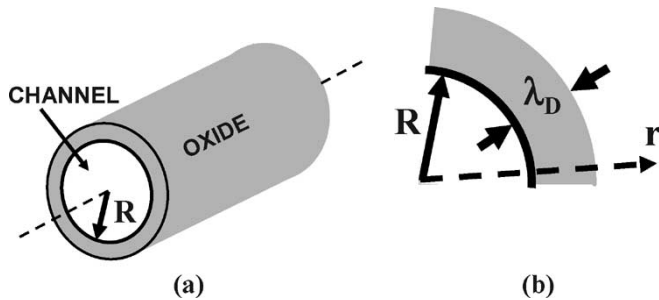


Fig. 6. (a) Cylindrical MOSFET with channel radius R ; the gate oxide surrounds the channel. (b) Hydrogen diffusion occupies a cylindrical shell in the gate oxide. The shaded volume corresponds to hydrogen diffusing away from the semiconductor/oxide interface.

As the devices are scaled to very small dimensions, the area of the Si/SiO₂ interface is reduced. Therefore, individual transistor may contain only a few interface traps and the number of traps can vary significantly from one transistor to the next. In this context, the results in this paper based on R–D model should be interpreted as being the median NBTI degradation averaged over a large number of transistors (e.g., millions of transistors in an IC). The fluctuation of NBTI degradation for individual transistors (around the median degradation predicted by the R–D model) can then be easily calculated by statistical models [24], [25]. This is analogous to gate-oxide degradation models, where average degradation is analyzed by physical models like Anode Hole Injection or Hydrogen Release, while the fluctuation effects are accounted for by statistical models based on percolation theory [26].

Now that we know how the geometry of diffusion is related to trap-generation rate, we will next consider specific technology examples where this could be relevant and explore the validity of the analysis by detailed numerical simulation.

III. SIMULATION RESULTS AND COMPARISONS WITH ANALYSIS

Over the last ten years, the continued miniaturization of MOSFETs has allowed unprecedented scaling of planar devices now reaching down to 65-nm node. According to the International Roadmap for Semiconductors (ITRS), the oxide scaling is about to reach its technological limits due to the exponential increase in the leakage current [14]. This leaves the burden of scaling mainly to the Si body of the transistors. Until the 45-nm node, the employment of silicon-on-insulator (SOI) and ultrathin body (UTB) architecture can maintain the miniaturization trends by reducing short channel effects (SCE) and capacitive losses, and blocking most of the leakage paths [27]. Afterwards, multiple-gate MOSFET structures, such as FinFETs and tri-gate transistors, will be needed to improve the SCE further and control the leakage better. Scaling below channel lengths of 20 nm will require nonclassical architectures and materials. VRG and nanowire devices are considered as promising ultra-scaled options that can offer both high-performance and high-density circuits [28], [29]. Self-heating observed in the UTB and SOI MOSFETs may speed up the temperature-activated NBTI degradation; therefore, NBTI can become

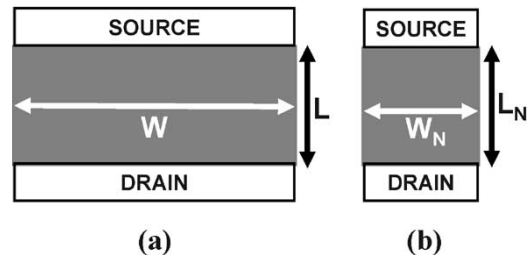


Fig. 7. Top view of planar MOSFETs with shaded area representing the channel. (a) Conventional wide-width MOSFET ($W \gg L$). (b) Narrow-width MOSFET ($W_N \sim L_N$). Narrow-width geometry implies higher NBTI degradation in the R–D model.

a more important concern for the aforementioned devices [30]–[32]. Scaling the dimensions of these future-generation devices can also affect the NBTI reliability due to the geometric dependence, as developed in Section II. In this section, numerical simulation results for several MOSFET geometries that are candidates mentioned in the ITRS are presented. The details of the numerical implementation can be found in Appendix C. The analyses based on the diffusion length are also compared here with simulations for each device structure.

Throughout this paper, only the degradation under DC stress is considered for the simulations to compare the worst case NBTI. AC degradation is proportional to that of DC and asymptotically gives the same time exponent, as obtained from experiments and R–D simulations [12], [13]. Another important feature of NBTI is saturation characteristics. The decrease in the time exponent during saturation can be attributed to the buildup of hydrogen at the material interfaces, consumption of Si–H bonds (see region iv in Fig. 2), or experimental artifacts, such as the delay and subsequent recovery in charge-pumping measurements. The devices studied in the literature, so far, are relatively large-area transistors from the perspective of this paper. At this point, it is not clear whether the saturation or geometry effects will dominate for ultra-scaled devices, therefore, the saturation effects are not included in the numerical solutions. As for the parameters, the D_H (at room temperature) is taken to be 10^{-15} cm²/s and N_0 as 10^{14} cm⁻² for all the simulations [16], [32], [33]. In the experimentally feasible time period (up to 10^5 – 10^6 s), $\lambda_D = (D_H t)^{0.5}$ grows to about 100 nm. The k_f and k_r were assumed to be the same for transistors belonging to a particular geometry. To reduce the simulation time, one-sided diffusion [see Fig. 3(a) and (b)] is implemented in the numerical solutions following (5), (8), and (11), and since $D_{eff} \sim D_H$ as mentioned in Section II-C. The distribution in the activation energies of k_f and k_r is not implemented in the simulations because we anticipate that the effects are negligible. Also, we did not include nitrided spacers or cap layers that can reflect hydrogen and change the dimensionality of diffusion since we want to focus on general principles and because future-generation devices may not contain such structures.

A. Narrow-Width Planar MOSFET

Shrinking the channel lengths of planar MOSFETs for each technology node also scales the channel widths. Additionally,

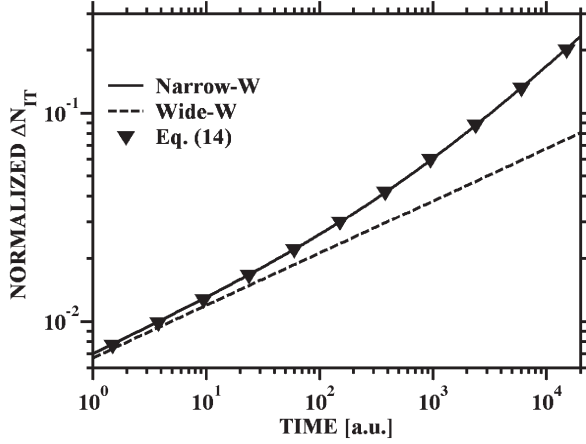


Fig. 8. NBTI-induced interface-trap density for wide ($W \sim 10 \mu\text{m}$, dashed line) and narrow-width ($W \sim 25 \text{ nm}$, solid line) MOSFETs. The time behavior is obtained from the geometry-dependent R-D simulations. The interface-trap density increases when the width is scaled. The symbols from (14) agree remarkably well with NBTI simulations. Since λ_D increases with time, the degradation becomes faster as λ_D/W grows.

the channel widths can be narrowed further for applications that require higher packing densities on chips [34], [35]. A wide-width ($W_w > L$) and a narrow-width ($W_n \sim L$) planar MOSFETs are illustrated in Fig. 7(a) and (b), respectively. Such channel dimensions can have significant impact on the device reliability. The numerical simulation result for NBTI degradation is displayed in Fig. 8 for the narrow-width and wide-width cases. The narrow channel width enhances the diffusion of hydrogen released from the Si-H bonds at the Si/oxide interface; therefore NBTI induced interface-trap densities increase. The diffusion-length analysis obtained from (14) agrees well with the R-D model. Since the analysis involves the geometry of the diffusion, the degradation trends for both wide- and narrow-width transistors can be obtained through (14) quickly without time-demanding NBTI simulations. The time exponent n can range from $1/4$ to $1/2$ for the narrow-width MOSFET unlike the traditional NBTI exponent of $1/4$. As the channel width gets narrower, the exponent increases, as discussed in Section II. Also, the time exponent in the narrow-width case is increasing further with time because the diffusion length λ_D is increasing as $(D_H t)^{0.5}$.

B. Triple-Gate MOSFET

Below the 45-nm node, multiple-gate MOSFET structures offer an alternative to the conventional planar transistors. FinFET and tri-gate MOSFETs allow better SCE control and, since they have multiple channels, lower operating voltages and mobilities are acceptable compared to the single-gate MOSFETs. Decreasing the body thickness W_b allows improved electrostatics, therefore, it is an important parameter from the scaling perspective [36]. The scalability range of the body thickness is currently approaching down to sub-10-nm regime [37]–[44]. The consequence of such dimensions in terms of NBTI reliability is considered in Fig. 9(a) and (b). The numerical NBTI simulation is compared with the experimental NBTI degradation of a triple-gate MOSFET with $W_b = 30 \text{ nm}$ in

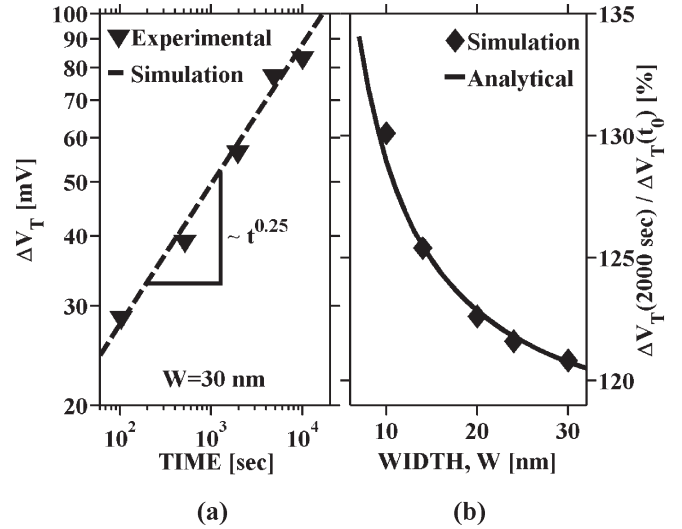


Fig. 9. (a) Experimental data from [45] and numerical simulation results for a triple-gate MOSFET with $W = 30 \text{ nm}$. The two agree. (b) NBTI degradation for scaled triple-gate transistors. The relation deduced from (15) and numerical simulation compares well. Same oxide capacitance is assumed for all widths. The t_0 is the time when the first data point is measured in the experiment.

Fig. 9(a), and it agrees well with the data. In Fig. 9(b), a scaling scenario for the triple-gate transistor is illustrated. As the body thickness is reduced, the 2-D components at the corners of the body facilitate the diffusion of hydrogen, and the degradation predicted by the NBTI simulation increases significantly. The estimation from (15) also confirms the trend of the simulations. Again, the compact relation derived from the concept of diffusion length provides a time-efficient approximation.

Besides the scaling, facet dependence of NBTI can induce a problem for the triple-gate MOSFETs as well. If the channels have different crystal orientations, NBTI can degrade these surfaces in dissimilar amounts, thus, the electrical parameters of the three channels can shift differently over time [45]. Since the gate control will change, the electrostatic advantages of the triple-gate geometry can be lost during device operation.

C. Surround-Gate MOSFET

Further going down the ITRS below the 20-nm node, the multiple-gate geometry is expected to lead into the all-around-gate structures for ultimate gate control. Surround-gate MOSFETs with Si channels were fabricated in [46] and, recently, cylindrical Si-nanowires with diameters down to 5 nm were realized [47]–[48]. Both these experimental work and numerical studies reflect that such devices can potentially continue the scaling of transistors [49]–[51]. However, the geometry dependent R-D model predicts worsened NBTI reliability for the ultra-scaled cylindrical MOSFET. Fig. 10 shows that the lifetime of the devices decreases significantly as the channel radius is shrunken. The lifetimes are obtained through asymptotic extrapolation of the numerical simulation results, namely the N_{IT} versus time behavior, as it would be done in experimental characterization. The lifetime criterion for the MOSFETs is when the trap density increases to a certain amount at the Si/oxide interface, thus a critical V_T shift is reached ($\Delta V_T \sim \alpha \cdot q \Delta N_{IT} / C_{OX}$, q electron charge, C_{OX}

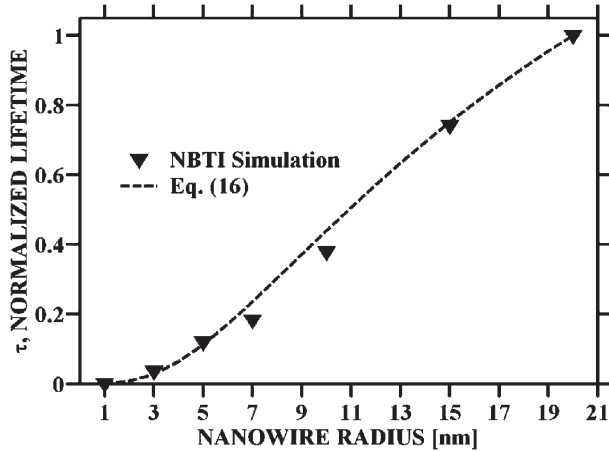


Fig. 10. Lifetime of cylindrical MOSFETs as a function of channel radius R . The lifetimes are normalized to that of $R = 20$ nm. As the device radius is scaled, the hydrogen diffusion is enhanced and the lifetime decreases. The symbols are obtained through the geometry-dependent R–D simulations. The dashed line represents the compact form of (16) and it compares well with the simulation.

oxide capacitance, and α ($\sim 0.1 - 1.0$) is the fraction of N_{IT} that contributes as positive interface charges [1]). For the scaled radii, the curvature of the interface increases the diffusion rate of hydrogen as well as slowing the annealing mechanism [19]. The interface trap generation accelerates and, thus, the lifetime of the surround-gate MOSFETs are reduced. The analysis of (16) compares well with the results of the numerical solution; therefore, an accurate prediction of the device lifetime can be obtained without the involved R–D simulations.

For the narrow-width triple-gate surround-gate MOSFETs discussed, the NBTI degradation rate n increases as the device geometry is scaled. The overall NBTI damage, however, is determined with the additional parameters k_f , k_r , N_0 , and D_H [see (7), (10), (13)], which depend on the operating voltage, oxide thickness, strain, and also the transistor geometry [1]–[4]. Therefore, since reduced cross section devices have better electrostatic control at lower operating voltages, one may be able to reduce k_f of these transistors to compensate the increase in NBTI exponent n discussed above. Establishing the necessity, as well as the possibility of such co-optimization of performance and reliability, is key goal of this paper.

IV. CONCLUSION

The geometric interpretation of the hydrogen diffusion in the gate oxide allows extending the NBTI modeling from current-generation devices to the ultra-scaled and future-generation MOSFETs. The geometry of the MOSFETs shapes that of hydrogen diffusion and, thus, determines the NBTI-induced interface trap generation rate. Assuming that the other parameters remain the same, numerical simulations and a time-efficient straightforward theoretical analysis imply that, for narrow-width planar, triple-gate, and surround-gate MOSFETs, the NBTI degradation rate increases significantly as the devices are scaled down. This signals that the expected performance enhancement of such future-generation devices must be tempered by reliability considerations.

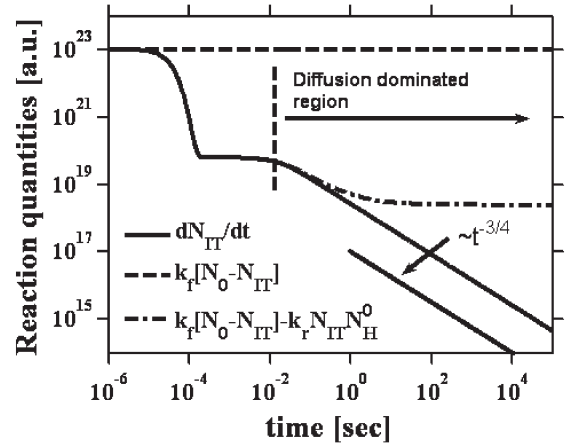


Fig. 11. Components of (2), obtained from the numerical simulation. dN_{IT}/dt term is negligible compared to the bond-breaking and annealing terms in the diffusion-dominated regime.

APPENDIX A

DERIVATION OF TIME EXPONENTS IN R–D MODEL ASSUMING STEADY-STATE CONDITIONS

Without the diffusion of hydrogen, the reaction given in (2) will progress into the equilibrium, i.e., forward and reverse reactions will balance. Diffusion, being a slower process compared to bond breaking and annealing, removes hydrogen from the Si/oxide interface and limits the rate at which the reaction moves in the forward direction. From a qualitative picture, it can be imagined that the diffusion acts on the quasi-steady-state condition of the reaction [$(dN_{IT}/dt) \sim 0$]. Quantitatively, Fig. 11 shows the quantities of (2) extracted from the numerical simulations. In the diffusion-dominated regime, where the NBTI time exponent ($N_{IT} \sim t^{0.25}$) is obtained, the dN_{IT}/dt term is orders of magnitude smaller than the bond breaking ($k_f[N_0 - N_{IT}]$) and annealing ($k_r N_{IT} N_H^0$) components. Analytically, $(dN_{IT}/dt) \sim t^{-3/4}$ and the numerical simulation match this behavior. Therefore, the assumption that dN_{IT}/dt is negligible compared to the reaction terms can be justified and it is employed in deriving (6). The assumption is used for analytical solutions; the numerical simulations solve the system without any approximations.

APPENDIX B

DIFFUSION-LENGTH ANALYSIS

In deriving (14)–(16), the hydrogen concentration at the Si/oxide interface $N_H^{(0)}$ is assumed to be the same everywhere including the edges and corners. In reality, this may not be correct; however, the results will only contain terms with minor scaling constants if the exact relations are to be obtained.

A. Planar MOSFET

Starting from the integral relation for the general case

$$N_{IT}(t) = \frac{1}{W \cdot L} \int N_H^{(0)}(r) d^3r. \quad (A1)$$

The volume occupied by the hydrogen profile contains the rectangular, cylindrical, and spherical sections as in (A2)

$$\begin{aligned}
N_{IT}(t) &= \frac{1}{W \cdot L} \left\{ \int_0^{\lambda_D} N_H^{(0)} \left(1 - \frac{y}{\sqrt{D_H t}} \right) W \cdot L \cdot dy \right. \\
&\quad + \frac{2}{4} \int_0^{\lambda_D} N_H^{(0)} \left(1 - \frac{r}{\sqrt{D_H t}} \right) \cdot 2\pi r L dr \\
&\quad + \frac{2}{4} \int_0^{\lambda_D} N_H^{(0)} \left(1 - \frac{r}{\sqrt{D_H t}} \right) \cdot 2\pi r W dr \\
&\quad \left. + \frac{4}{8} \int_0^{\lambda_D} N_H^{(0)} \left(1 - \frac{r}{\sqrt{D_H t}} \right) \cdot 4\pi r^2 dr \right\} \\
&= N_H^{(0)} \cdot \left\{ \frac{WL\lambda_D}{2} + \frac{\pi\lambda_D^2(L+W) + \pi\lambda_D^3}{6} \right\}. \quad (A2)
\end{aligned}$$

Using

$$N_{IT} \cdot N_H^{(0)} = \frac{k_f N_0}{k_r} \quad (A3)$$

we obtain the following compact form for planar MOSFETs

$$\begin{aligned}
N_{IT}^{PL}(t) &= \sqrt{\frac{k_f N_0}{WLk_r}} \\
&\cdot \left[\frac{WL(D_H t)^{\frac{1}{2}}}{2} + \frac{\pi(L+W)(D_H t) + \pi(D_H t)^{\frac{3}{2}}}{6} \right]^{\frac{1}{2}}. \quad (A4)
\end{aligned}$$

B. Triple-Gate MOSFET

The diffusion contains 1-D portions for the top and side gates and 2-D components at the corners of the Si-body

$$\begin{aligned}
N_{IT}(t) &= \frac{1}{3 \cdot W} \left\{ 2 \cdot \int_0^{\lambda_D} N_H^{(0)} \left(1 - \frac{x}{\sqrt{D_H t}} \right) W \cdot dx \right. \\
&\quad + \int_0^{\lambda_D} N_H^{(0)} \left(1 - \frac{y}{\sqrt{D_H t}} \right) W \cdot dy \\
&\quad \left. \times \frac{2}{4} \int_0^{\lambda_D} N_H^{(0)} \left(1 - \frac{r}{\sqrt{D_H t}} \right) \cdot 2\pi r dr \right\} \\
&= N_H^{(0)} \cdot \left\{ \frac{1}{2} \left(\lambda_D + \frac{\pi\lambda_D}{9 \cdot W} \right) \right\}. \quad (A5)
\end{aligned}$$

From (A3), the substitution gives

$$N_{IT}^{TRI}(t) = \sqrt{\frac{k_f N_0}{2k_r}} \cdot \left[(D_H t)^{\frac{1}{2}} + \frac{\pi \cdot (D_H t)}{9 \cdot W} \right]^{\frac{1}{2}}. \quad (A6)$$

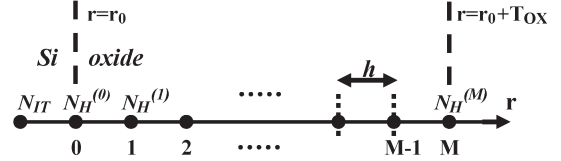


Fig. 12. Simulation domain of the R–D model is discretized uniformly from the Si/oxide interface to the gate. The first node is the interface-trap density term and the other nodes are the hydrogen density in the oxide.

$$J = \begin{bmatrix} a_{N_H^M} & \dots & \cdot \\ \vdots & \ddots & \vdots \\ \cdot & \dots & a_{N_H^0} \end{bmatrix} \begin{matrix} a_{BC} \\ a_R \\ \{a_{N_{IT}}\} \end{matrix}$$

Fig. 13. Form of the Jacobian matrix used in the time-dependent Newton–Raphson iteration. The matrix contains the diffusion block for hydrogen and the interface-trap block. The chemical reaction and the boundary condition terms provide the coupling between the two blocks for simultaneous solution. The hydrogen block is tri-diagonal in 1-D implementation.

C. Cylindrical MOSFET

The hydrogen profile is written in cylindrical coordinates and the integral becomes

$$\begin{aligned}
N_{IT}(t) &= \frac{1}{2\pi R \cdot L} \int_R^{R+\lambda_D} N_H^{(0)} \left(1 - \frac{r-R}{\sqrt{D_H t}} \right) 2\pi r L dr \\
&= N_H^{(0)} \cdot \left\{ \frac{(D_H t)^{\frac{1}{2}}}{2} \cdot \left(1 + \frac{R}{(D_H t)^{\frac{1}{2}}} \right) \cdot \left(2R + (D_H t)^{\frac{1}{2}} \right) \right. \\
&\quad - \frac{1}{3} \left[R^2 + R \cdot \left(R + (D_H t)^{\frac{1}{2}} \right) \right. \\
&\quad \left. \left. + \left(R + (D_H t)^{\frac{1}{2}} \right)^2 \right] \right\}. \quad (A7)
\end{aligned}$$

Similar to the planar case, using (A3)

$$\begin{aligned}
N_{IT}^{CYL}(t) &= \sqrt{\frac{k_f N_0}{Rk_r}} \\
&\times \left\{ \frac{(D_H t)^{\frac{1}{2}}}{2} \cdot \left(1 + \frac{R}{(D_H t)^{\frac{1}{2}}} \right) \cdot \left(2R + (D_H t)^{\frac{1}{2}} \right) \right. \\
&\quad \left. - \left[\frac{R^2 + R \cdot \left(R + (D_H t)^{\frac{1}{2}} \right) + \left(R + (D_H t)^{\frac{1}{2}} \right)^2}{3} \right] \right\}^{\frac{1}{2}}. \quad (A8)
\end{aligned}$$

APPENDIX C NUMERICAL SOLUTION

The numerical implementation of the R–D model is based on the reaction of (2) and the diffusion process of (3). The

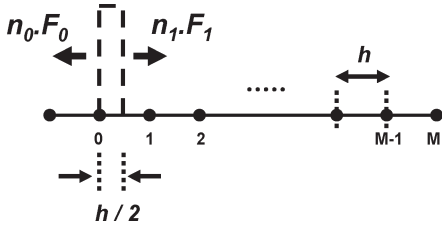


Fig. 14. Box integration is performed at the Si/oxide interface to obtain the boundary equations. The nodes numbered 0–M represent the gate oxide. F_0 and F_1 are the hydrogen fluxes; n_0 and n_1 are the normal vectors at the interface.

interface-trap density and the hydrogen density in the oxide are solved simultaneously through a time-dependent Newton–Raphson iteration scheme [39]. The simulation domain encompasses the Si/oxide interface and the oxide up to the gate, as illustrated in Fig. 12. The first node represents the interface-trap density N_{IT} , and the rest are the hydrogen nodes in the oxide. Fig. 13 shows the general form of the Jacobian matrix for 1-D hydrogen diffusion. The interface-trap density term a_{IT} is coupled to the hydrogen-density term at the interface $a_H^{(0)}$ through the chemical reaction terms a_R and the boundary condition element a_{BC} . Additional off-diagonal pairs are introduced for 2-D and 3-D solutions when implemented in Cartesian coordinates. Cylindrical and spherical coordinates can also be incorporated with the appropriate modification of the matrix elements. At the gate/oxide interface, infinite diffusion velocity ($D_H = \infty$) is assumed. The boundary condition at the Si/oxide interface has to couple the trap density to the hydrogen density correctly and is very crucial for proper convergence [52]. The derivations of the boundary equations for linear, cylindrical, and spherical coordinates are given below.

A. Boundary Conditions for 1-D Diffusion

The hydrogen diffusion satisfies

$$\frac{\partial N_H}{\partial t} = \frac{\partial F}{\partial x} \quad (\text{A9})$$

where the hydrogen flux is given as $F = D_H(\partial N_H / \partial x)$.

Using box integration at the Si/oxide interface as depicted in Fig. 14

$$\begin{aligned} \frac{\partial}{\partial t} \int_0^{\frac{h}{2}} N_H \cdot dx &= \int_0^{\frac{h}{2}} \left(\frac{\partial F}{\partial x} \right) \cdot dx \\ &= F \left(\text{at } \frac{h}{2} \right) - F(\text{at } 0) \\ &= \hat{n}_1 \cdot F_1 + \hat{n}_0 \cdot F_0 \\ &= D_H \frac{\partial N_H}{\partial x} + \frac{dN_{IT}}{dt}. \end{aligned} \quad (\text{A10})$$

Then, the boundary equation for 1-D diffusion is obtained by (A10) and (A11)

$$\frac{h}{2} \frac{\partial N_H}{\partial t} - D_H \frac{\partial N_H}{\partial x} - \frac{dN_{IT}}{dt} = 0. \quad (\text{A12})$$

B. Boundary Conditions for Cylindrical Coordinates

Writing (A9) in cylindrical coordinates $\partial N_H / \partial t = \nabla \cdot F = (1/r)(\partial/\partial r)(rF)$, and when the box integration is applied

$$\int_{r_0}^{r_0 + \frac{h}{2}} \frac{\partial N_H}{\partial t} 2\pi r dr = \int_{r_0}^{r_0 + \frac{h}{2}} 2\pi r \frac{1}{r} \frac{\partial}{\partial r} (rF) dr \quad (\text{A13})$$

$$\int_{r_0}^{r_0 + \frac{h}{2}} \frac{\partial N_H}{\partial t} 2\pi r dr = \pi \left(2r_0 + \frac{h}{2} \right) \frac{h}{2} \frac{\partial N_H}{\partial t} \quad (\text{A14})$$

$$\begin{aligned} \int_{r_0}^{r_0 + \frac{h}{2}} 2\pi r \frac{1}{r} \frac{\partial}{\partial r} (rF) dr &= 2\pi \left[\left(\frac{h}{2} + r_0 \right) \cdot F \left(\text{at } r_0 + \frac{h}{2} \right) \right. \\ &\quad \left. - r_0 \cdot F(\text{at } r_0) \right] \\ &= 2\pi \left[\left(\frac{h}{2} + r_0 \right) \cdot D_H \frac{\partial N_H}{\partial r} \right. \\ &\quad \left. + r_0 \cdot \frac{dN_{IT}}{dt} \right] \end{aligned} \quad (\text{A15})$$

and the boundary equation becomes

$$\frac{h}{2} \frac{\partial N_H}{\partial t} - \frac{2 \left(r_0 + \frac{h}{2} \right)}{\left(2r_0 + \frac{h}{2} \right)} \cdot \left[D_H \frac{\partial N_H}{\partial r} + \frac{r_0}{\left(r_0 + \frac{h}{2} \right)} \cdot \frac{dN_{IT}}{dt} \right] = 0. \quad (\text{A16})$$

C. Boundary Conditions for Spherical Coordinates

The box integration is performed in spherical domain, therefore

$$\frac{\partial N_H}{\partial t} = \nabla \cdot F = \frac{1}{r^2 \sin \theta} \left[\sin \theta \cdot \frac{\partial}{\partial r} (r^2 F) \right] = \frac{1}{r^2} \cdot \frac{\partial}{\partial r} (r^2 F) \quad (\text{A17})$$

$$\int_{r_0}^{r_0 + \frac{h}{2}} \frac{\partial N_H}{\partial t} 4\pi r^2 dr = \int_{r_0}^{r_0 + \frac{h}{2}} 4\pi r^2 \frac{1}{r^2} \frac{\partial}{\partial r} (r^2 F) dr \quad (\text{A18})$$

$$\begin{aligned} \int_{r_0}^{r_0 + \frac{h}{2}} 4\pi r^2 \frac{1}{r^2} \frac{\partial}{\partial r} (r^2 F) dr &= \left[\left(\frac{h}{2} + r_0 \right)^2 \cdot F \left(\text{at } r_0 + \frac{h}{2} \right) \right. \\ &\quad \left. - r_0^2 \cdot F(\text{at } r_0) \right] \\ &= \left[\left(\frac{h}{2} + r_0 \right)^2 \cdot D_H \frac{\partial N_H}{\partial r} \right. \\ &\quad \left. + r_0^2 \cdot \frac{dN_{IT}}{dt} \right] \end{aligned} \quad (\text{A19})$$

$$\int_{r_0}^{r_0 + \frac{h}{2}} \frac{\partial N_H}{\partial t} r^2 dr = \left(3r_0^2 + \frac{3hr_0}{2} + \frac{h^2}{4} \right) \frac{h}{2} \frac{\partial N_H}{\partial t}. \quad (\text{A20})$$

Combining (A19) and (A20) results in

$$\frac{h}{2} \frac{\partial N_H}{\partial t} - \frac{1}{\left(r_0^2 + \frac{hr_0}{2} + \frac{h^2}{12}\right)} \cdot \left[\left(r_0 + \frac{h}{2}\right)^2 \cdot D_H \frac{\partial N_H}{\partial r} + r_0^2 \cdot \frac{dN_{IT}}{dt} \right] = 0. \quad (\text{A21})$$

ACKNOWLEDGMENT

The authors would like to thank S. Mahapatra and T. Nigam, for the helpful comments, and N. V. Pimparkar and P. R. Nair for reviewing the manuscript. The numerical simulations were performed through the facility provided by The Network for Computational Nanotechnology (NCN) at Purdue University.

REFERENCES

- [1] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing," *J. Appl. Phys.*, vol. 94, no. 1, pp. 1–18, Jul. 2003.
- [2] M. A. Alam and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation," *Microelectron. Reliab.*, vol. 45, no. 1, pp. 71–81, Jan. 2005.
- [3] V. Reddy *et al.*, "Impact of negative bias temperature instability on digital circuit reliability," in *Proc. IEEE IRPS*, 2002, pp. 248–254.
- [4] A. T. Krishnan, V. Reddy, S. Chakravarthi, J. Rodriguez, S. John, and S. Krishnan, "NBTI impact on transistor and circuit: Models, mechanisms and scaling effects [MOSFETs]," in *IEDM Tech. Dig.*, 2003, pp. 349–352.
- [5] W. Abadeer and W. Ellis, "Behavior of NBTI under AC dynamic circuit conditions," in *Proc. IEEE IRPS*, 2003, pp. 17–22.
- [6] Y. Chen, J. Zhou, S. Tedja, F. Hui, and A. S. Oates, "Stress-induced MOSFET mismatch for analog circuits," in *Proc. IEEE Integr. Rel. Workshop Final Report*, 2001, pp. 41–43.
- [7] M. Agostinelli, S. Lau, S. Pae, P. Marzolf, H. Muthali, and S. Jacobs, "PMOS NBTI-induced circuit mismatch in advanced technologies," in *Proc. IEEE IRPS*, 2004, pp. 171–175.
- [8] C. J. Nicklaw, Z. Y. Lu, and D. M. Fleetwood, "The structure, properties and dynamics of oxygen vacancies in amorphous SiO₂," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 2667–2673, Dec. 2002.
- [9] L. Tsetseris and S. T. Pantelides, "Migration, incorporation and passivation reactions of molecular hydrogen at the Si-SiO₂ interface," *Phys. Rev. B, Condens. Matter*, vol. 70, no. 24, pp. 245320-1–245320-6, Dec. 2004.
- [10] J. W. McPherson *et al.*, "Complementary model for intrinsic time-dependent dielectric breakdown in SiO₂ dielectrics," *J. Appl. Phys.*, vol. 88, no. 9, pp. 5351–5359, 2000.
- [11] L. Tsetseris *et al.*, "Physical mechanisms of negative-bias temperature instability," *Appl. Phys. Lett.*, vol. 86, no. 14, pp. 142103-1–142103-3, Apr. 2005.
- [12] M. A. Alam, "A critical examination of the mechanics of dynamic NBTI for PMOSFETs," in *IEDM Tech. Dig.*, 2003, p. 345.
- [13] S. Chakravarthi, A. Krishnan, V. Reddy, C. F. Machala, and S. Krishnan, "A comprehensive framework for predictive modeling of negative bias temperature instability," in *Proc. IEEE IRPS*, 2004, pp. 273–282.
- [14] Semiconductor Industry Association (SIA), *The International Technology Roadmap for Semiconductors*. 2004 Update. [Online]. Available: <http://public.itrs.net>
- [15] A. K. O. Jeppson and C. M. Svensson, "Negative bias of MOS devices at high electric fields and degradation of MNOS devices," *J. Appl. Phys.*, vol. 48, no. 5, pp. 2004–2014, May 1977.
- [16] S. Mahapatra, P. B. Kumar, and M. A. Alam, "A new observation of enhanced bias temperature instability in thin gate oxide p-MOSFETs," in *IEDM Tech. Dig.*, 2003, p. 337.
- [17] N. Kimizuka, K. Yamaguchi, K. Imai, T. Iizuka, C. T. Liu, R. C. Keller, and T. Horiuchi, "NBTI enhancement by nitrogen incorporation into ultrathin gate oxide for 0.10 μm gate CMOS generation," in *VLSI Symp. Tech. Dig.*, 2000, pp. 92–93.
- [18] S. Rangan, N. Mielke, and E. C. C. Yeh, "Universal recovery behavior of negative bias temperature instability," in *IEDM Tech. Dig.*, 2003, p. 341.
- [19] H. Kufluoglu and M. A. Alam, "A geometrical unification of the theories of NBTI and HCI time-exponents and its implications for ultra-scaled planar and surround-gate MOSFETs," in *IEDM Tech. Dig.*, 2004, pp. 113–116.
- [20] A. Stesmans, "Dissociation kinetics of hydrogen-passivated P_b defects at the (111) Si/SiO₂ interface," *Phys. Rev. B, Condens. Matter*, vol. 61, no. 12, pp. 8393–8403, Mar. 2000.
- [21] M. A. Alam and H. Kufluoglu, "On quasi-saturation of negative bias temperature degradation," in *Proc. 208th Meeting Electrochem. Soc.*, 2005.
- [22] S. Bedard and L. J. Lewis, "Diffusion of hydrogen in crystalline silicon," *Phys. Rev. B, Condens. Matter*, vol. 61, no. 15, pp. 9895–9898, 2000.
- [23] T. Nigam, "Growth kinetics, electrical characterization and reliability study of sub-5 nm gate dielectrics," Ph.D. dissertation, Departement Elektrotechnik, Katholieke Universiteit Leuven, IMEC, Belgium, 1999, p. 30.
- [24] M. Agostinelli *et al.*, "Random charge effects for PMOS NBTI in ultra-small gate area devices," in *Proc. IEEE IRPS*, 2005, pp. 529–532.
- [25] K. Hess *et al.*, "Simulation of Si-SiO₂ defect generation in CMOS chips: From atomistic structure to chip failure rates," in *IEDM Tech. Dig.*, 2000, pp. 93–96.
- [26] M. A. Alam, B. E. Weir, and P. Silverman, "A future of function or failure?" *IEEE Circuits Devices—Electron. Photon. Mag.*, vol. 18, no. 2, pp. 42–48, Mar. 2002.
- [27] M. Jeong, B. Doris, J. Kedzierski, K. Rim, and M. Yang, "Silicon device scaling to the sub-10 nm regime," *Science*, vol. 306, no. 5704, pp. 2057–2060, Dec. 2004.
- [28] J. M. Hergenrother *et al.*, "The vertical replacement-gate (VRG) MOSFET: A 50 nm vertical MOSFET with lithography-independent gate length," in *IEDM Tech. Dig.*, 1999, pp. 75–78.
- [29] R. Li *et al.*, "50 nm vertical surround-gate MOSFET with S-factor of 75 mV/dec," in *Proc. Device Res. Conf. Dig.*, 2001, pp. 63–64.
- [30] L. T. Su, J. E. Chung, D. A. Antoniadis, K. E. Goodson, and M. I. Flik, "Measurement and modeling of self-heating in SOI nMOSFETs," *IEEE Trans. Electron Devices*, vol. 41, no. 1, pp. 69–75, Jan. 1994.
- [31] R. J. T. Bunyan, M. J. Uren, J. C. Alderman, and W. Eccleston, "Activation of NBTI degradation in SOI PMOS by self-heating," in *Proc. IEEE Int. SOI Conf.*, 1992, pp. 130–131.
- [32] B. Kaczer *et al.*, "Disorder-controlled-kinetics model for negative bias temperature instability and its experimental verification," in *Proc. IEEE IRPS*, 2005, pp. 381–387.
- [33] I. Kizilyalli, J. W. Lyding, and K. Hess, "Deuterium post-metal annealing of MOSFETs for improved hot carrier reliability," *IEEE Electron Device Lett.*, vol. 18, no. 3, pp. 81–83, Mar. 1997.
- [34] M. J. Deen and Z. P. Zuo, "Edge effects in narrow-width MOSFETs," *IEEE Trans. Electron Devices*, vol. 38, no. 8, pp. 1815–1819, Aug. 1991.
- [35] M. Saitoh, E. Nagata, and T. Hiramoto, "Effects of ultra-narrow channel on characteristics of MOSFET memory with silicon nanocrystal floating gates," in *IEDM Tech. Dig.*, 2002, pp. 181–184.
- [36] H. J. Cho *et al.*, "Fin width scaling criteria of body-tied FinFET in sub 50 nm regime," in *Proc. Device Res. Conf. Dig.*, 2004, pp. 209–210.
- [37] Y. Liu *et al.*, "A highly threshold voltage-controllable 4T FinFET with an 8.5 nm thick Si-fin channel," *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 510–512, Jul. 2004.
- [38] F. L. Yang *et al.*, "5 nm gate nanowire FinFET," in *VLSI Symp. Tech. Dig.*, 2004, pp. 196–197.
- [39] E. J. Nowak *et al.*, "Scaling beyond the 65 nm node with FinFET-DGCMOS," in *Proc. Custom Integr. Circuits Conf.*, 2003, pp. 339–342.
- [40] M. Lemme *et al.*, "Subthreshold characteristics of p-type triple-gate MOSFETs," in *Proc. Eur. Solid-State Device Res. Conf.*, 2003, p. 123.
- [41] S. E. Thompson *et al.*, "In search of 'forever,' continued transistor scaling one new material at a time," *IEEE Trans. Semicond. Manuf.*, vol. 18, no. 1, pp. 26–36, Feb. 2005.
- [42] M. Specht *et al.*, "Novel dual bit tri-gate charge trapping memory devices," *IEEE Electron Device Lett.*, vol. 25, no. 12, pp. 810–812, Dec. 2004.
- [43] B. S. Doyle *et al.*, "High performance fully-depleted tri-gate CMOS transistors," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 263–265, Apr. 2003.
- [44] Y. Bin *et al.*, "FinFET scaling to 10 nm gate length," in *IEDM Tech. Dig.*, 2002, pp. 251–254.
- [45] S. Maeda *et al.*, "Negative bias temperature instability in triple-gate transistors," in *Proc. IEEE IRPS*, 2004, pp. 8–12.
- [46] M. Je, S. Han, I. Kim, and H. Shin, "A silicon quantum wire transistor with one-dimensional subband effects," *Solid State Electron.*, vol. 44, no. 12, p. 2207, 2000.
- [47] H. Majima, Y. Saito, and T. Hiramoto, "Impact of quantum mechanical effects on design of nano-scale narrow channel n- and p-type MOSFETs," in *IEDM Tech. Dig.*, 2001, p. 733.

- [48] Y. Cui, Z. Zhong, D. Wang, U. W. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Lett.*, vol. 3, no. 2, p. 149, 2003.
- [49] O. Sang-Hyun, D. Monroe, and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 445–447, Sep. 2000.
- [50] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 18, no. 2, pp. 74–76, Feb. 1997.
- [51] J. Wang, E. Polizzi, and M. Lundstrom, "A computational study of ballistic silicon nanowire transistors," in *IEDM Tech. Dig.*, 2003, p. 695.
- [52] H. Küflüoğlu and M. A. Alam, "A computational model of NBTI and hot carrier injection time-exponents for MOSFET reliability," *J. Comput. Electron.*, vol. 3, no. 3, pp. 165–169, Oct. 2004.



Haldun Küflüoğlu (S'04) was born in Turkey, in 1979. He received the B.S. and M.S. degrees in electrical engineering from Purdue University, West Lafayette, IN, in 2001 and 2003, respectively. Currently, he is working toward the Ph.D. degree, in which his research involves measurements and theoretical modeling of MOSFET degradation mechanisms, such as negative bias temperature instability (NBTI), HCI and time dependent dielectric breakdown (TDDB), and their implications on very large scale integration (VLSI) design, at the same

institution.

His research interests include MOSFET reliability, experimental characterization, and modeling of semiconductor devices. He also participates in OFF-state transistor reliability assessment. Previously, he obtained microfabrication skills in a MEMS-based sensor that was interfaced with live neurons for biological applications.

Mr. Küflüoğlu is a student member of IEEE Electron Device Society (EDS).



Muhammad Ashraf Alam (F'97) received the B.S.E.E. degree from Bangladesh University of Engineering and Technology, Bangladesh, in 1988, the M.S. degree from Clarkson University, Potsdam, NY, in 1991, and the Ph.D. degree from Purdue University, Lafayette, IN, in 1994, all in electrical engineering.

He is a Professor in electrical and computer engineering at Purdue University where his research and teaching focus on physics, simulation, characterization and technology of classical and novel semiconductor devices. From 1995 to 2001, he was with Bell Laboratories, Lucent Technologies, Murray Hill, NJ, as a Member of Technical Staff in the Silicon ULSI Research Department. From 2001 to 2003, he was a Distinguished Member of Technical Staff and the Technical Manager of the IC Reliability Group at Agere Systems, Murray Hill, NJ. He joined Purdue University in 2004 and his current research includes theory of oxide reliability, transport in nanocomposite thin-film transistors, and nano-bio sensors. He has published over 75 papers in international journals and has presented many invited and contributed talks at international conferences.

Dr. Alam received the International Reliability Physics Symposium (IRPS) Best Paper Award in 2003 and the Outstanding Paper Award in 2001, both for his work on gate-oxide reliability. Recently, he was elected an IEEE Fellow for contribution to physics of CMOS reliability and simulation of optoelectronic devices and received the IEEE Kiyo Tomiyasu Award for his contributions to the device technology for communication systems.