

Separation Method of Hole Trapping and Interface Trap Generation and Their Roles in NBTI Reaction-Diffusion Model

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INTRODUCTION

NBTI is one of the most critical reliability problems in advanced CMOS technologies. Its characterization has been corrupted by recovery effect due to the switching and measurement delays [1,2]. In order to eliminate this recovery effect, many different fast I_d - V_g techniques have been developed, including the on-the-fly $I_{d,lin}$ [1-3] and pulse I_d - V_g [4,5]. However, inconsistent NBTI results and hole trapping model were obtained when performing these fast I_d - V_g techniques [3-5]. In this paper, we (1) propose a separation method of hole trapping from the measured V_t shift, (2) study the voltage and temperature dependency of hole trapping and interface trap generation, (3) demonstrate the three significant stages of interface trap generation in analytical H-H₂ NBTI Reaction-Diffusion model, and (4) clarify the influence of hole trapping on device lifetime extrapolation.

EXPERIMENTS

PMOS devices with plasma nitrided oxide SiON (EOT \sim 12Å) were fabricated using advanced CMOS process technology. The delay time of NBTI stress-measure-stress technique was reduced to as short as 1.26 ms by using Keithley 2600 series high speed Source-Measure-Units, thus providing the timing-on-the-fly NBTI characteristics minimizing recovery effect.

RESULTS AND DISCUSSION

Separation Method of ΔV_h and ΔV_{it}

Fig. 1 shows ΔV_t as a function of stress time with various delay times ranging from 1.26 to 420 ms. It seems that ΔV_t magnitude and time exponent vary with the delay time even under the same stress conditions. This controversy can be addressed by proposing the ΔV_t is a combination of hole trapping ΔV_h and interface trap generation ΔV_{it} where the ΔV_h is highly modulated by the delay time. In addition, we found the difference between every two ΔV_t curves in Fig. 1 is a constant during the stress (Fig. 2), presumably due to the difference of two hole trapping levels. Based on the hole trapping/de-trapping model [6-8], ΔV_h should saturate rapidly and keep constant during the stress time. Therefore, the initial ΔV_t measured at very short stress time could be regarded as ΔV_h (Fig. 3), and the contribution of interface traps to overall V_t shift without involving hole trapping could be obtained by subtracting the initial degradation magnitude from whole time evolution curve, as shown in Fig. 3. Since ΔV_h of 1.26 ms delay could be defined as ΔV_t at very short stress time, we could obtain each ΔV_h corresponding to various delays because hole trapping differences between every two delays have been given (Fig. 2). After correcting both hole trapping and recovery effect, the ΔV_{it} curves of various delays overlap together (Fig. 4) and exhibit the ideal time exponent of 1/6 in the classical NBTI reaction-diffusion model. Thus, we may conclude the debate on the various time exponents observed by many research groups results from the interferences from hole trapping and recovery effect in different delay time (Fig. 5).

Voltage Dependence of ΔV_h and ΔV_{it}

Fig. 6 shows time evolution of ΔV_t , having delay \sim 1.26 ms and $n \sim$ 0.12. After subtracting hole trapping, as shown in Fig. 7, the time exponents vary from 1 to 1/6 and ΔV_{it} goes through three different stages as proposed in analytical NBTI Reaction-Diffusion model [7-8]. Within very short stress time, the analytical reaction-limited solution suggests $n \sim$ 1. During intermediate stress time, the atomic hydrogen released from interface is being converted to molecular H₂, and gives a time exponent of 1/3. For long-term, neutral H₂ diffusion becomes the dominant mechanism of interface trap that limits degradation rate ($n \sim$ 1/6). Fig. 8 plots voltage dependent ΔV_h , which is in qualitative agreement with the voltage dependency of trapping model [8]. As ΔV_h increases with increase in stress voltage, it affects the device lifetime significantly at higher stress voltage (Fig. 9) compared to that at lower stress bias. It is noticed that the extrapolation without eliminating contribution of hole trapping significantly overestimates device lifetime at operation voltage.

Temperature Dependence of ΔV_h and ΔV_{it}

Fig. 10 (a) and (b) plot the temperature dependent of ($\Delta V_{it} + \Delta V_h$) measured by timing on-the-fly with delay \sim 1.26 ms and ΔV_{it} only, respectively. Fig. 11 shows the activation energies of ΔV_{it} and ΔV_h . E_a for ΔV_{it} (0.109eV) are in good agreement with activation values of interface trap reported in literatures [2,6]. On the contrary, hole trapping reveals much less temperature sensitivity ($E_a \sim$ 0.04eV) than that of interface trap, also consistent with literature [9]. Fig. 10 (b) also indicates that not only the interface trap at long-term, but also at intermediate stress time are affected by temperature, as expected within R-D framework [7,8]. Thus the temperature dependence of ΔV_{it} suggests temperature activation for H₂ diffusion (governing at long-term) and H-H₂ conversion (dominating at intermediate stress time) are temperature activated.

CONCLUSIONS

In this study, we propose a systematic method to separate the hole trapping from measured V_t shift, thus giving the ideal interface trap generation behavior without measurement disturbance. Three stages of interface trap generation have been illustrated with the analytical H-H₂ NBTI reaction-diffusion model, and the hole trapping has also been verified with its voltage-enhanced and temperature-insensitive properties. Finally, the lifetime extrapolation without considering the hole trapping might lead to significant lifetime overestimation.

REFERENCES

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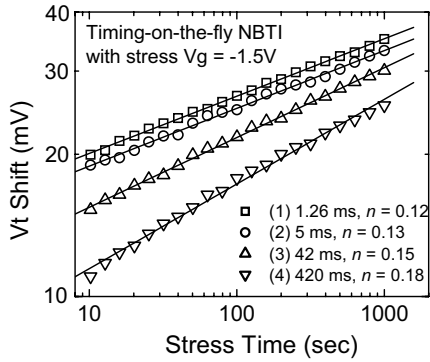


Fig. 1 Time exponent of ΔV_t with various measurement delays.

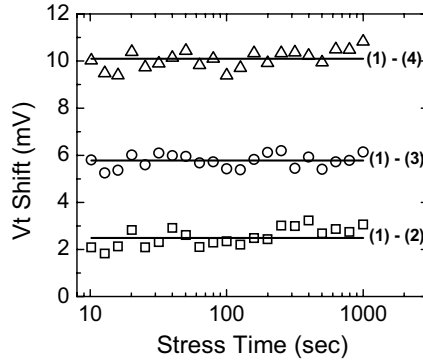


Fig. 2 ΔV_t differences between various measurement delays correspond to Fig. 1.

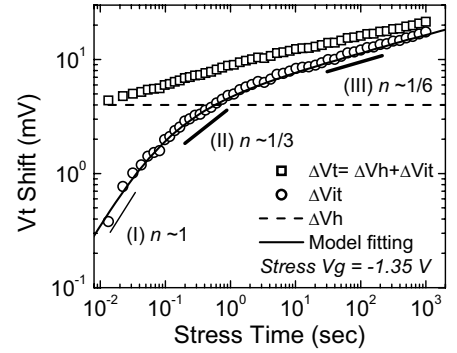


Fig. 3 Stress time dependence of ΔV_t and correction by subtracting hole trapping. The ΔV_{it} trend agrees well with model.

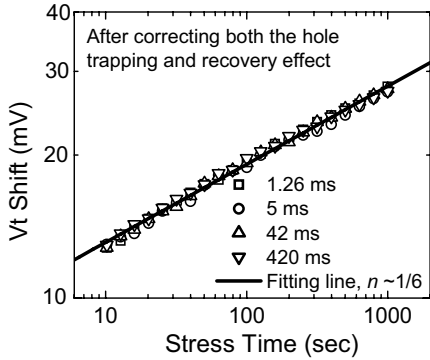


Fig. 4 ΔV_t dependence on stress time after correcting both hole trapping and recovery effects.

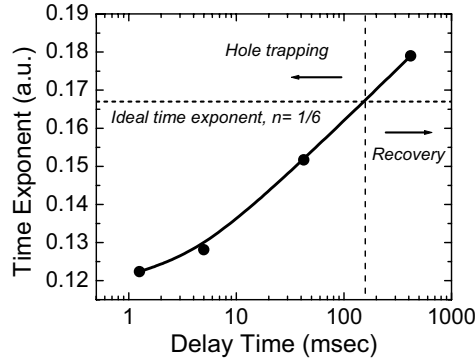


Fig. 5 Measurement delay dependence of time exponent.

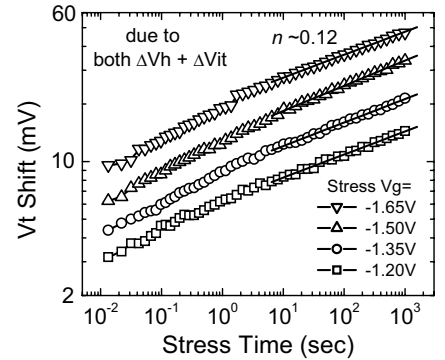


Fig. 6 Time evolution of ΔV_t at various stress bias (delay ~ 1.26 ms). Time exponents for long-term show 0.12 universally.

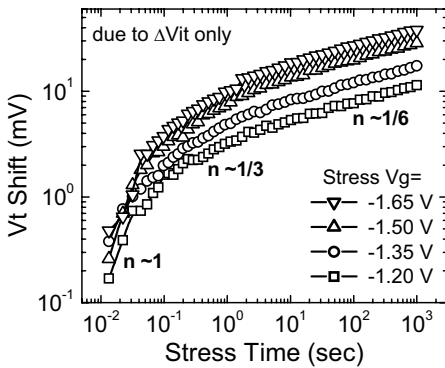


Fig. 7 Time evolution of ΔV_{it} at various stress bias w/o hole trapping. Long-term time exponents show 1/6 universally.

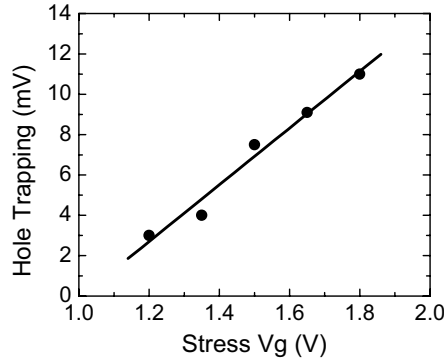


Fig. 8 V_g dependence of hole trapping.

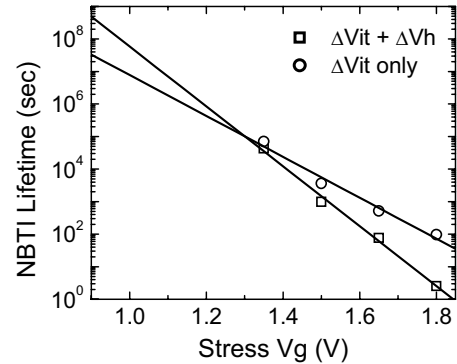


Fig. 9 Device lifetime comparison between fast measurement (delay ~ 1.26 ms) and w/o hole trapping.

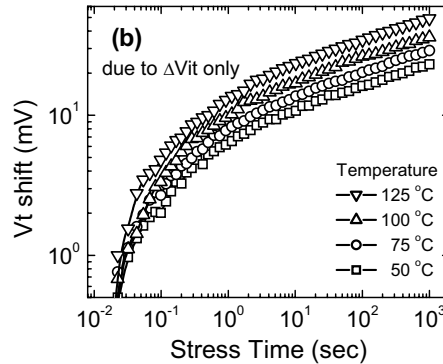
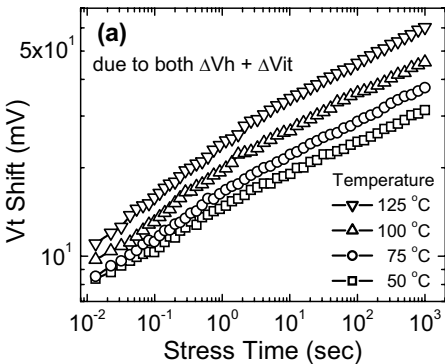


Fig. 10 ΔV_t dependence on stress time evolution of (a) timing on-the-fly (delay ~ 1.26 ms) and (b) ΔV_{it} only with various temperatures.

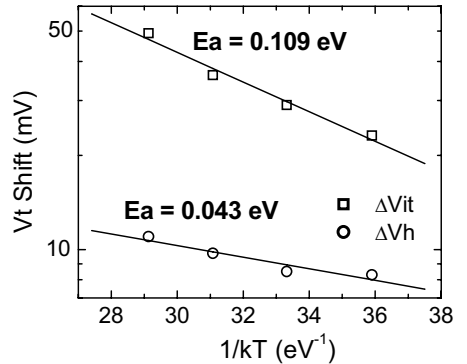


Fig. 11 Temperature activation of ΔV_t for interface traps and hole trapping.