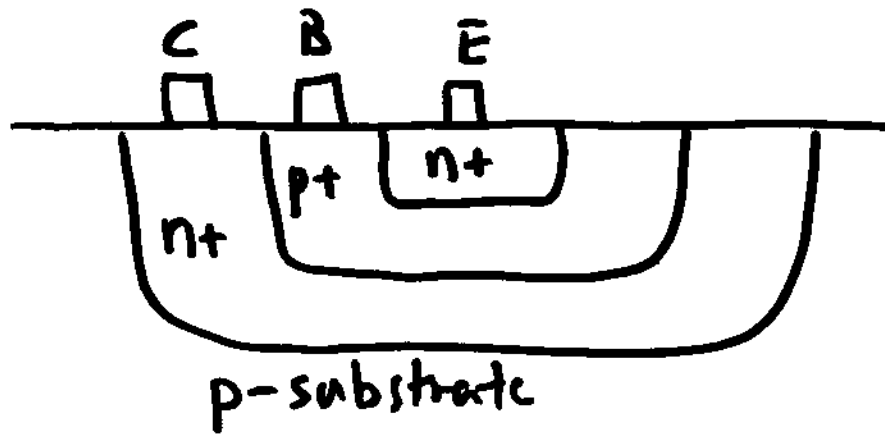


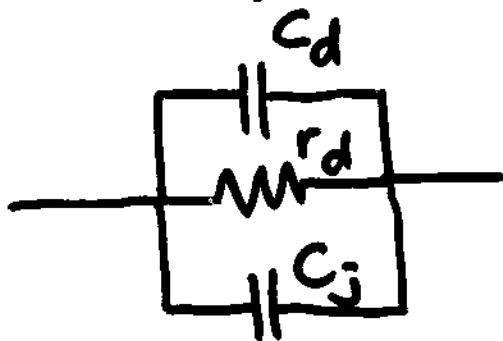
High Frequency BJT Transistor Model



pn-junction



high freq model



C_j : Junction capacitance

$$\frac{C_{j0}}{\left(1 - \frac{V_D}{V_{bi}}\right)^m}$$

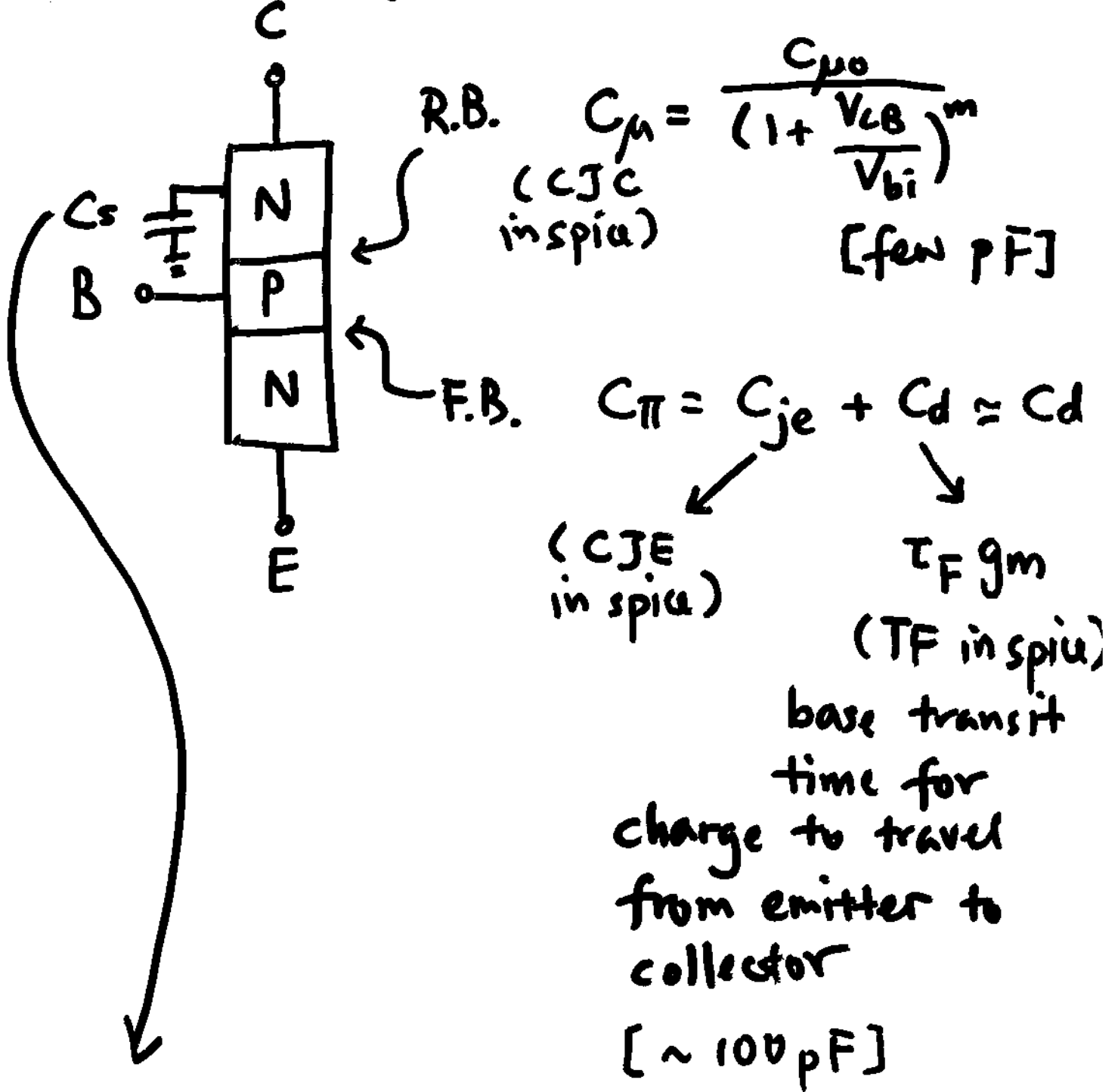
C_d : Diffusion capacitance

$$\beta I_D$$

F.B. : C_d dominates

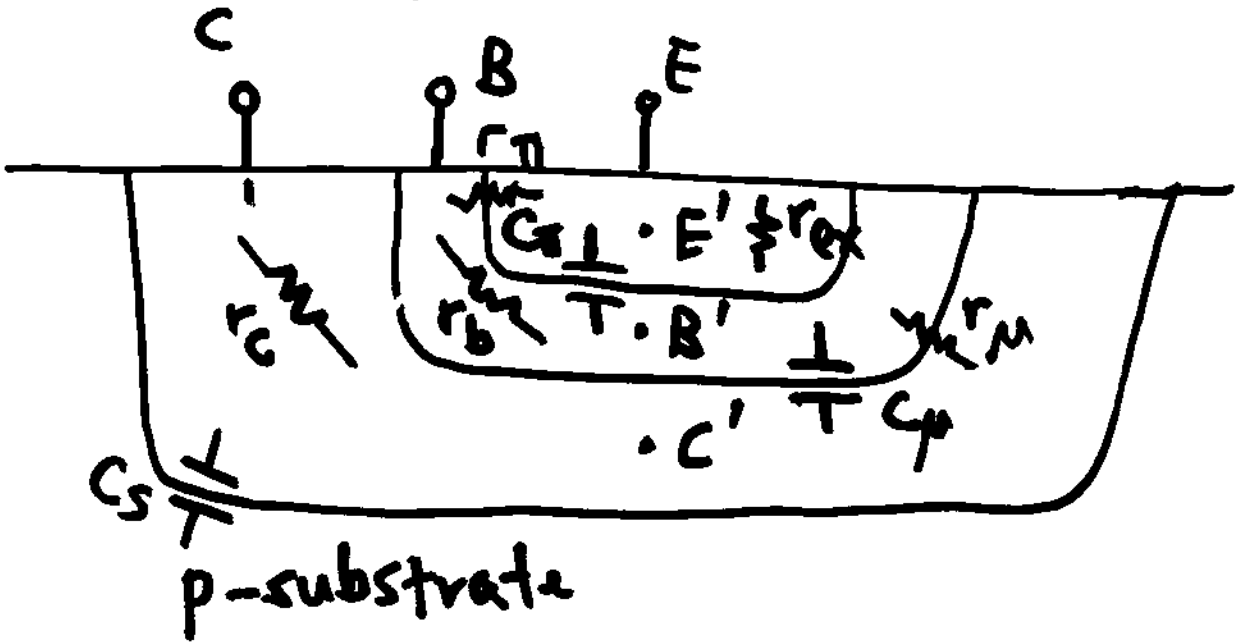
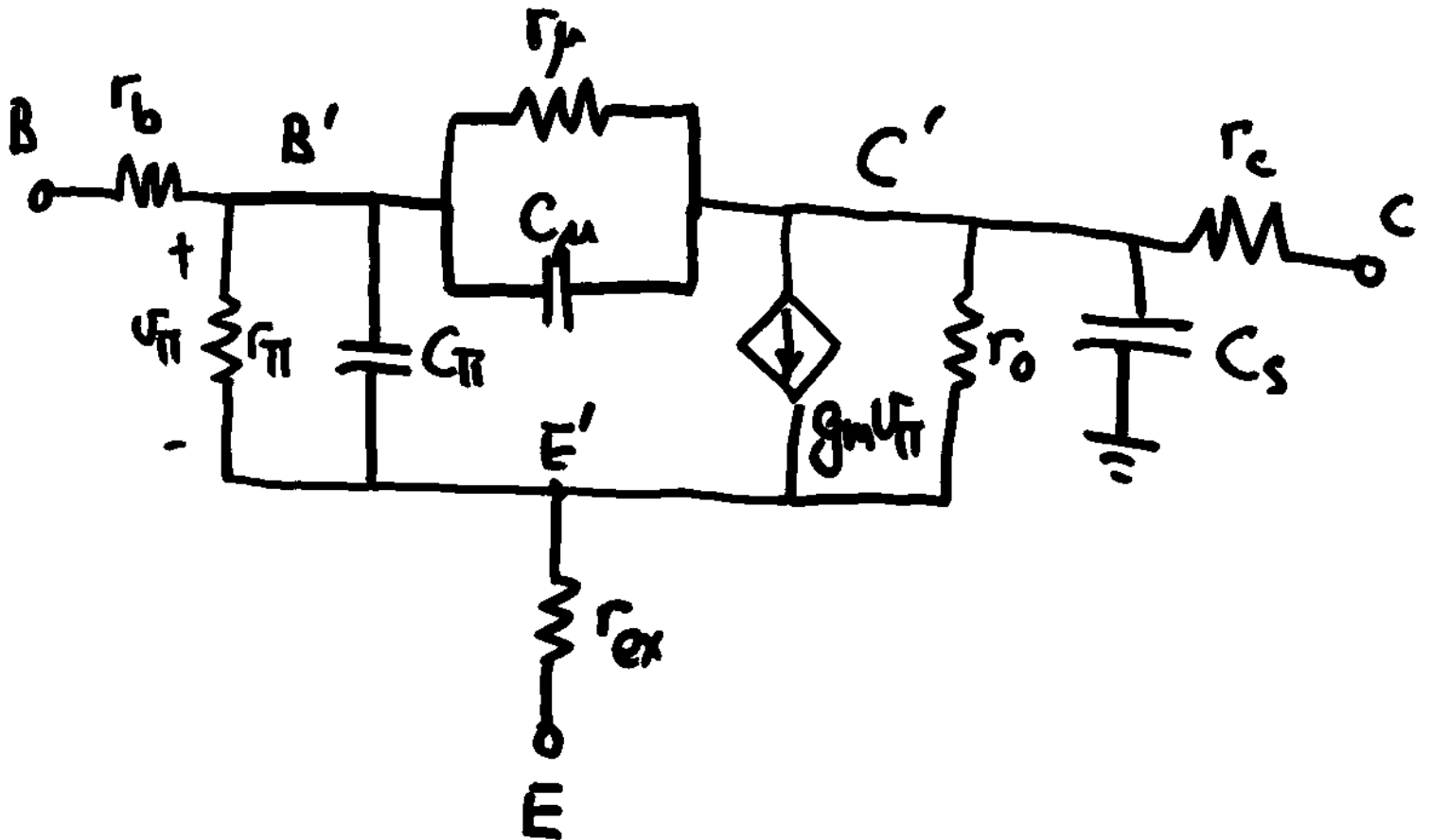
R.B. : C_j dominates

Forward Active BJT



C_s : collector-substrate capacitor
 R.B. junction capacitor

Hybrid- π Equivalent Circuit



Resistances

r_b : silicon resistance from base contact to the edge of emitter (RB in spice)
[50 - 500 Ω]

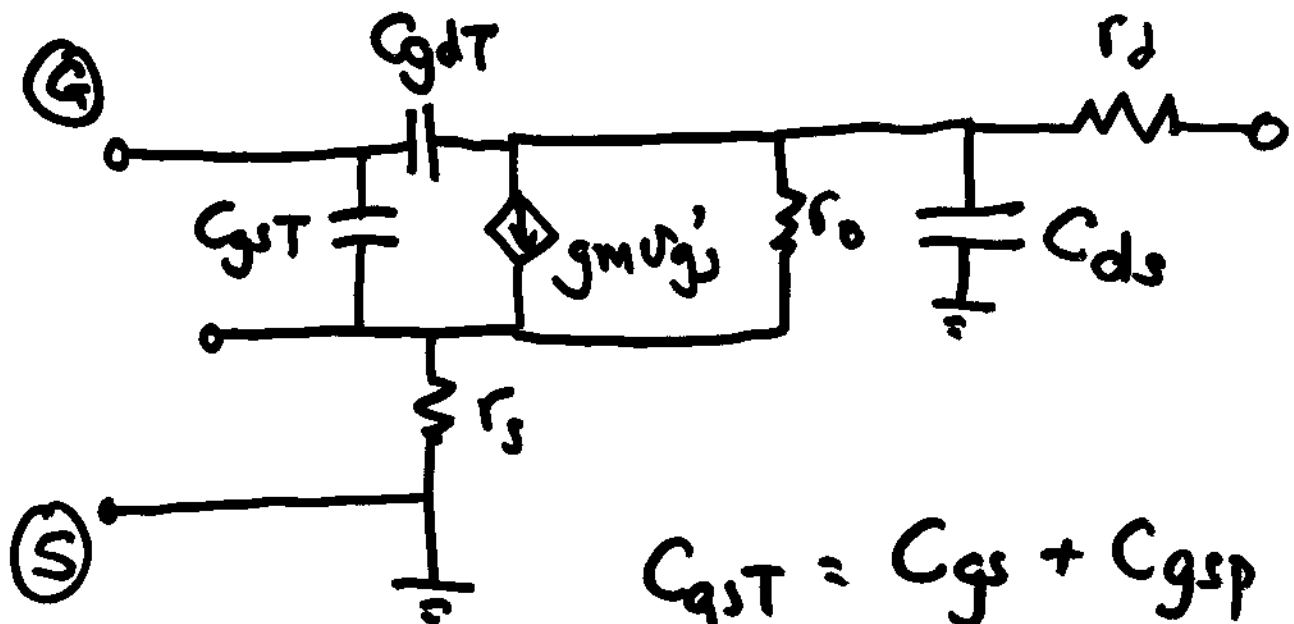
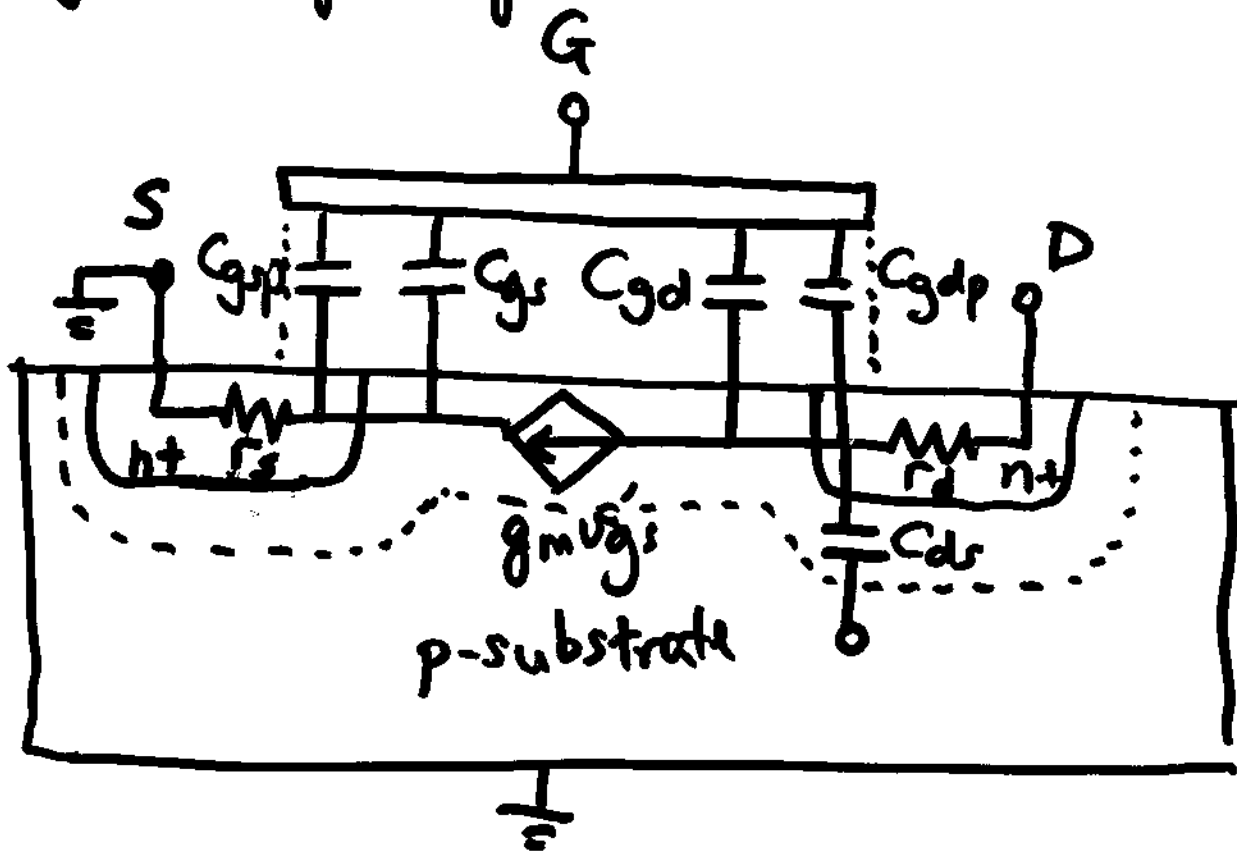
r_c : silicon resistance from collector contact to the collector-base junction (RC in spice) [$\sim 100 \Omega$]

r_{ex} : resistance in series with emitter lead (RE in spice) [1 - 3 Ω]

r_μ : reverse-biased diffusion resistance between collector and base

$$r_\mu \cong 5\beta r_o \quad (\text{ignored in text in general})$$

High Frequency MOSFET Transistor Model



$$C_{gsT} = C_{gs} + C_{gsp}$$

$$C_{gdT} = C_{gd} + C_{gdp}$$

$$\approx C_{gdp}$$

Capacitances:

① Gate inversion layer

$$C_{gs} \cong C_{gd} \cong \left(\frac{1}{2}\right) WL C_{ox} \quad \text{Non-sat}$$

$$C_{gs} \cong \frac{2}{3} WL C_{ox} \quad \text{SAT}$$

* $C_{gd} = 0$ (inversion layer disappears)

$$C_{gb} = WL C_{ox} \quad \begin{array}{l} \text{cut-off} \\ \text{[TOX in spice]} \end{array}$$

② Overlap capacitance

$$C_{gsp} = C_{gdp} = C_{ox} \underbrace{LD}_\downarrow W$$

[overlap in spice]

[CGSO & CGDO in spice]

③ Junction capacitance

Drain is R.B wrt substrate

[CBD in spice]

Resistances

1. r_d : Drain resistance
silicon resistance
 $\sim 10 \Omega$ (R_D in $\text{spi}u$)
2. r_s : Similar to r_d (R_S in $\text{spi}u$)