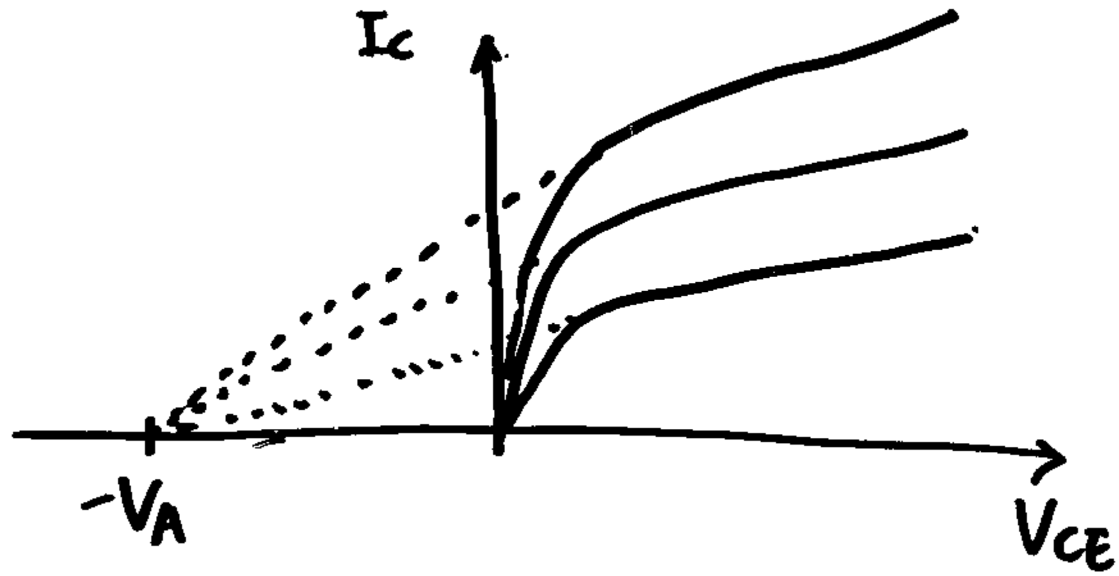
Non-idealities of BJTs



V_A : Early Voltage

50 - 300 V typically

$$\text{slope} = \frac{1}{r_o} = \left.\frac{\partial I_C}{\partial V_{CE}}\right|_{V_{BE}=\text{const}}$$

$$\approx \frac{I_C}{V_A}$$

$$I_C = \alpha I_S \left(e^{V_{BE}/V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right)$$

Leakage Currents

- CB configuration
- Emitter open
- I_{CBO} – reverse bias saturation current in B-C junction

- CE configuration
- Base open
- I_{CEO} – I_{CBO} increases base potential
  - F.B. B-E junction

$$I_{CEO} = I_{CBO} + \alpha I_{CEO}$$

$$= \frac{I_{CBO}}{1-\alpha} \cong \beta I_{CBO}$$

Breakdown voltage

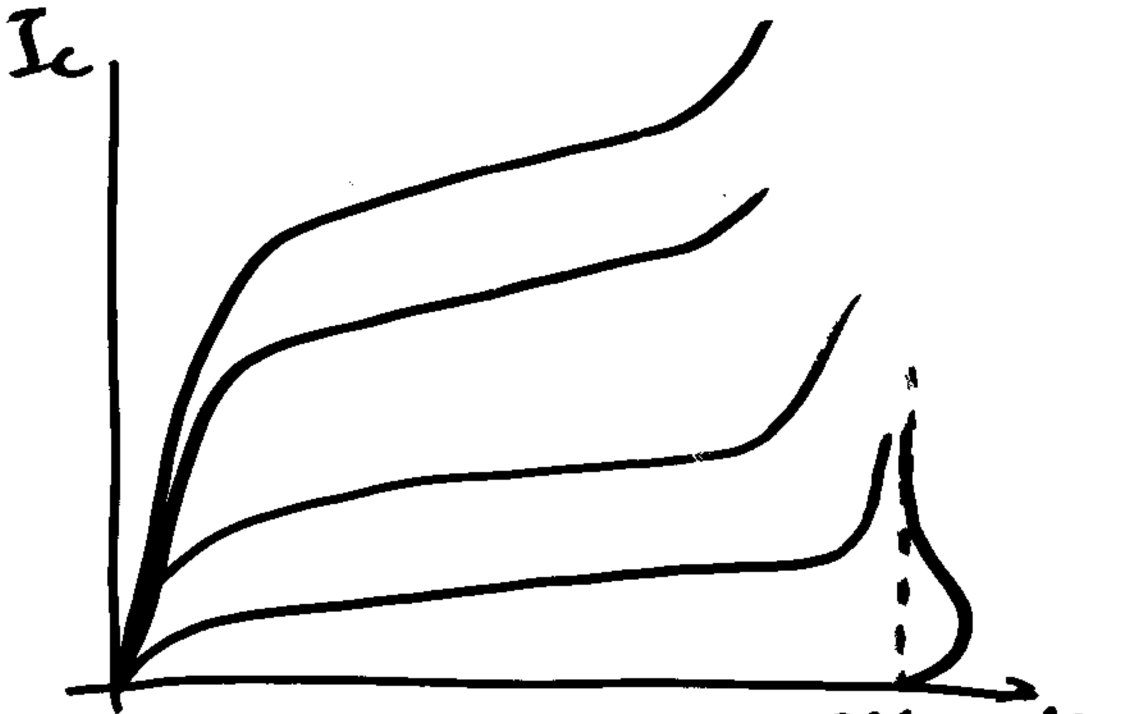
Each junction has a breakdown

BV_{CBO} - $I_E = 0$

BV_{CB} - decreases for $I_E > 0$

BV_{CEO} - $I_B = 0$

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}}$$



Thermal Effects.

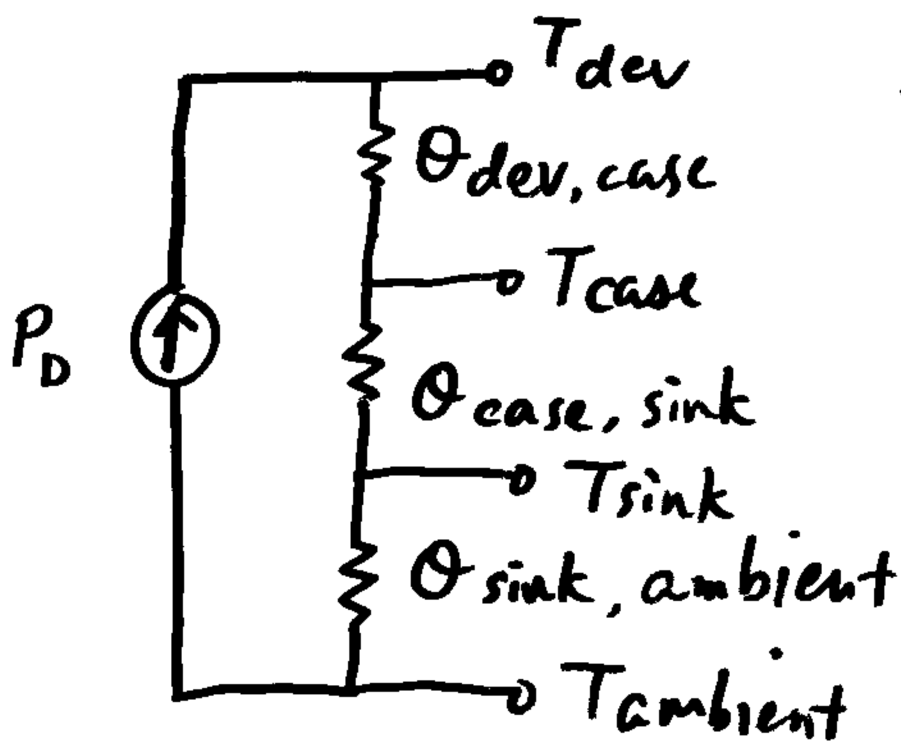
- Device / Junction gets heated
- Heat has to be dissipated to air

$$\underbrace{T_2 - T_1}_{\text{Temp. diff.}} = P\,\theta$$

- θ → thermal resistance °C/W
- P → heat flow, thermal power

Electrical Analog:

$$V_2 - V_1 = I R$$



$$T_{dev} - T_{amb} = P_D(\theta_{dev,case} + \theta_{case,sink} + \theta_{sink,amb})$$

Better Heat flow ⇒ Lower θ

- Design for low θ

① Good Thermal Contact

Larger area of contact

between chip & case

case & heat sink

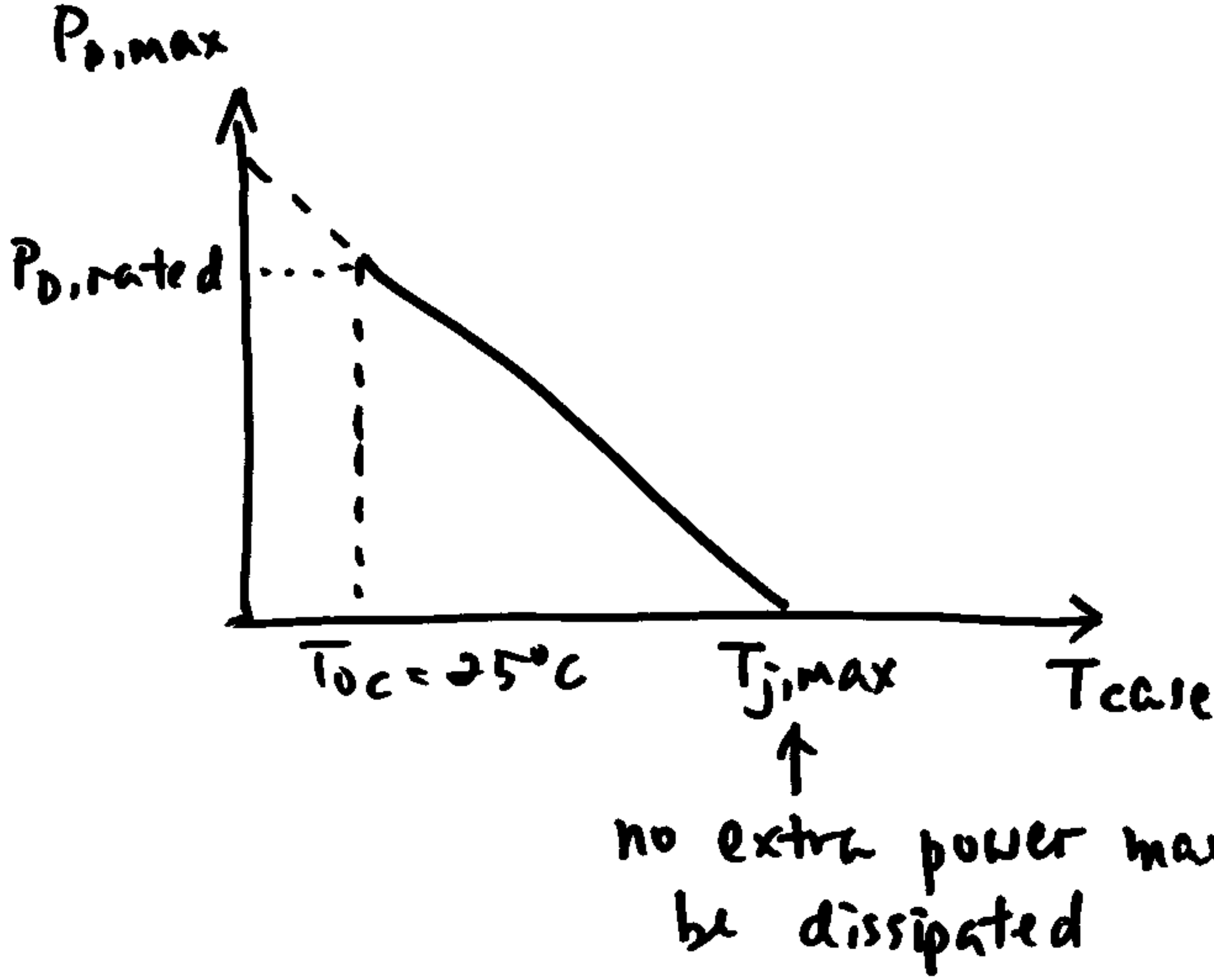
② Min. $\theta_{case-amb} = \theta_{case-sink} + \theta_{sink-amb}$

by large heat sink + fan.

Max. safe power dissipation

$$T_{j,max} = T_{case} + P_{D,max}\theta_{dev\text{-}case}$$

$$P_{D,max} = \frac{T_{j,max} - T_{case}}{\theta_{dev\text{-}case}}$$



Ex. $T_{j,max} = 175°C$, $\theta_{case\text{-}sink} = 1°C/W$

$P_{D,rated} = 20W$ $\theta_{sink\text{-}amb} = 5°C/W$

$P_{D,max}$ (with heat sink) ?