

Skewed CMOS: Noise-Immune High-Performance Low-Power Static Circuit Family¹

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Abstract

In this paper, we present a noise-immune high-performance static circuit family suitable for low-voltage operation called skewed logic. Skewed logic circuits, in comparison with Domino logic, have better scalability, and they are more suitable for low voltage applications because of better noise margin. Skewed logic has been compared with Domino logic in terms of delay, power, and dynamic noise immunity. A design methodology for skewed CMOS pipelined circuits has been developed. Comparisons between skewed and Domino circuits on a 0.25 μm 700 MHz 16 x 16 bits pipelined multiplier show superior properties of skewed circuits over Domino in terms of clock power dissipation and peak current consumption.

1. Introduction

With advances in CMOS device technology, both performance and power consumption of integrated circuits have improved dramatically. In very high performance designs, dynamic circuits like Domino [1], [2] are used due to their high speed. However, with the continuing scaling of supply voltage and transistor threshold voltage, it is more difficult to use Domino circuits because of the dependence of their noise margin on the threshold voltage variation.

This problem can be solved by using skewed logic circuits, the concept of which was introduced in [3], [4]. Skewed circuits are fully complementary static logic circuits. The sizes of PMOS and NMOS transistors are adjusted to make one of the transitions faster than the other. Changing the driving capabilities of PMOS and

NMOS transistor networks to favour one transition direction is referred to as *skewing*.

Skewed logic gates have performance comparable to that of dynamic circuits, whereas the noise immunity of skewed logic is better because it has no floating nodes. The floating node in a Domino gate can be eliminated using a keeper device. However, the keeper cannot restore the correct state of the gate if a false transition occurs due to input glitch.

Skewed logic allows a trade-off between the delay of the gate and its noise margin. Because of higher noise immunity, skewed logic is better than Domino logic for high-performance, low-voltage, and low-power applications.

Similar to dynamic circuits, skewed logic falls in the category of precharge-evaluate logic families. Fast transition is used for evaluation while slow transition can be used for precharge.

The rest of the paper is organized as follows: Section 2 describes the operation of skewed logic. Section 3 discusses pipelining with skewed logic. Section 4 presents the energy-delay comparisons for static CMOS, Domino, and skewed logic. Section 5 discusses a dynamic noise immunity model and compares static CMOS, Domino and skewed logic in terms of dynamic noise immunity. Section 6 describes a skewed CMOS multiplier example. Section 7 concludes the paper.

2. Skewed logic

Circuit topology of skewed logic gate is the same as that of classical static CMOS logic. Fig. 1a shows a NAND-NOR-NAND structure. To speed up the high-to-low transition, the sizes of NMOS transistors of the first NAND gate are increased, and the sizes of PMOS

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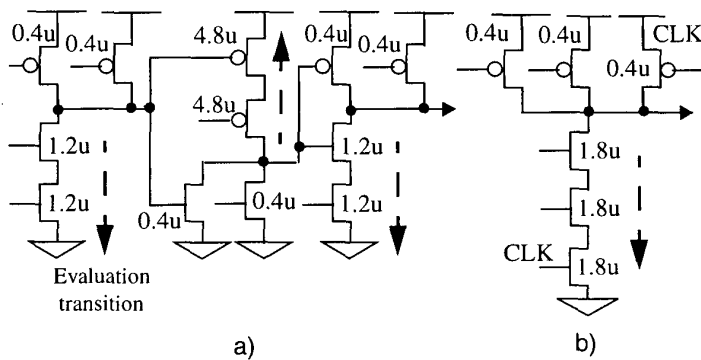


Fig. 1. Circuit topology and gate connection

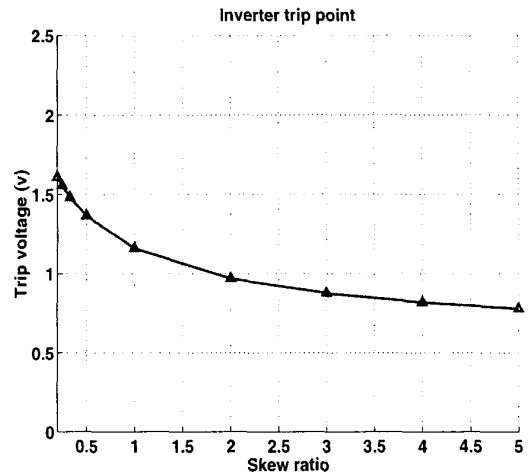


Fig. 2. Inverter trip-point dependence on the skew

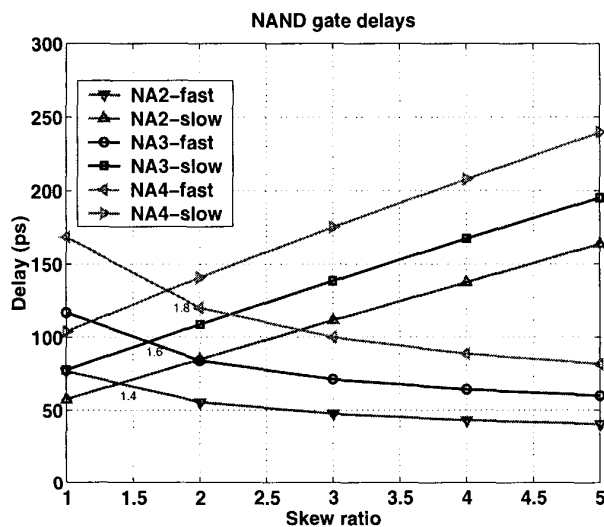


Fig. 3. NAND gate delay dependence on the skew

transistors are decreased. For fast low-to-high transition, the transistor widths of the NOR gate are changed in the opposite directions. The ratio of the worst case driving capabilities of pull-down and pull-up networks is called the *skew*.

In order to achieve performance comparable to Domino circuits, the skewed gates should operate in two phases: precharge and evaluation. During precharge, all nodes are reset to the initial state. During evaluation, the circuit performs useful work and only fast transitions can occur. To ensure that, the gate skewed for fast high-to-low transition should be followed by gate skewed for fast low-to-high transition and vice versa. An example of such a connection is shown in Fig. 1a. Circuit shown in Fig. 1b should be used if fast precharge from the clock is necessary. Precharge of pipelined skewed circuits is further discussed in Section 3.

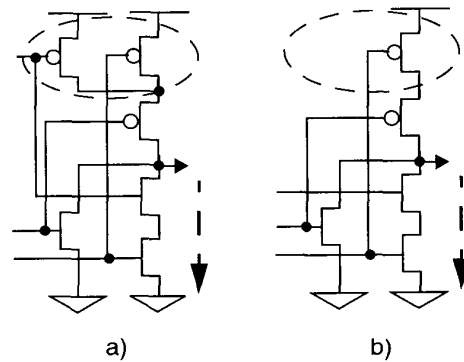


Fig. 4. Simplification of skewed circuit

Skewing of a gate affects its performance in two ways: the trip point and the driving capabilities of the transistor networks change. Fig. 2 shows the dependence of the trip point for an inverter on the skew. We used models for 0.25 μm CMOS technology with 2.5V supply voltage (V_{dd}). The skew of 1 corresponds to the case when the ratio between PMOS and NMOS transistor sizes is equal to 2.

Delay dependence of both fast and slow transitions on the skew is shown in Fig. 3 for a NAND gate that is skewed for a fast falling transition. Skew of 1 corresponds to the case where the gate has equal worst case high-to-low and low-to-high delays in the standard static CMOS logic mode, in which the worst case low-to-high transition of NAND gate has a single PMOS device activated. However, the delays shown in Fig. 3 correspond to the NAND gate operated in a precharge/evaluate fashion when the precharge transition has every PMOS transistor activated. Because of that the precharge delay of the

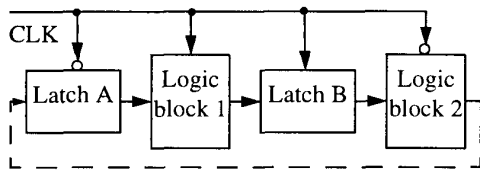


Fig. 5. Basic pipeline structure

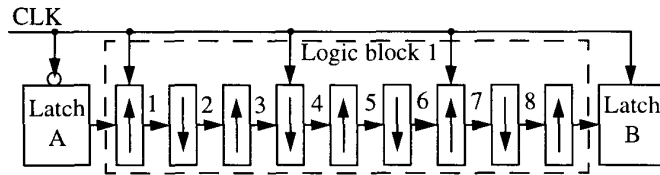


Fig. 6. Logic block structure

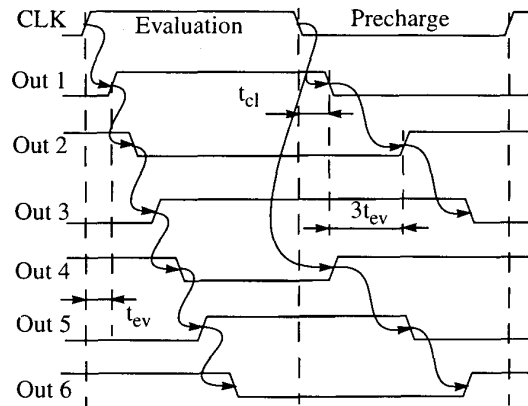


Fig. 7. Waveforms for circuit in Fig. 6

skewed NAND gate is less than the worst case delay of rising transition of static CMOS gate.

In some cases skewed gate can be simplified. Fig. 4a shows AND-NOR gate skewed for fast falling transition. In this gate parallel PMOS transistors can be collapsed into one transistor (Fig. 4b). Although such a simplification does not affect functionality of the skewed gate, it does affect noise immunity because in some situations the output can be floating.

3. Pipelining with skewed logic

A pipeline with skewed CMOS circuits can be synthesized following the same procedure as in Domino logic [5]. Fig. 5 shows a basic pipeline structure. The logic of each pipeline stage is divided into two blocks separated by latches. During the first half of the cycle, when the clock is high, logic block 1 is evaluating while latch A holds data. At the same time, logic block 2 is being precharged and latch B is transparent. During the second half of the cycle the situation is just the opposite. This technique allows propagation of data without waiting for the precharge of the next stage.

In such a pipeline, precharge and evaluation delays of each logic block should be less than a half cycle. In the case of Domino or noise tolerant precharge circuits (NTP - Fig. 1b) [6], [7] it is easy to achieve short precharge delay because each gate is connected to the clock signal. However, in the skewed circuit not all gates should be connected to the clock.

Fig. 6 shows a logic block structure for skewed logic. In this figure the fast transition directions are designated by arrows. The gates connected to the clock have the same structure as the NTP circuits in Fig. 1b. In this example, we assume that the fast (evaluation) transition delay of all gates is t_{ev} and that the slow (precharge) transition is three

times longer ($3t_{ev}$). We assume also that the delay from the clock (t_{cl}) of the gate connected to the clock is no greater than $3t_{ev}$. The sizing for such skew is shown in Fig. 1. Waveforms on the outputs of the gates are shown in Fig. 7. Precharge of first, fourth and seventh gates starts immediately after the falling edge of the clock. Hence, the precharge delay is less than half cycle.

Such a technique reduces the number of gates connected to the clock in the skewed logic circuit in comparison with Domino and NTP circuits. Therefore, skewed circuits have lower clock capacitance and lower clock power consumption. Moreover, they draw a lower peak current from the power supply.

Another advantage is the precharge process being more evenly distributed over time. Unlike Domino or NTP not all skewed gates are precharged simultaneously after clock edge. This can be seen from the above example (Figs. 6 and 7). In the beginning of the precharge half cycle only three out of nine gates are precharged. Second gate is precharged only after the precharge of the first gate is completed and so on. Distributed precharge process further reduces peak current and it simplifies physical design.

4. Energy-delay comparisons

In order to evaluate different circuits families, delay and energy per transition are measured. Various data points are obtained by changing the overall gate size.

Static CMOS gates have an optimum ratio (in terms of energy-delay product) of 1.5 between PMOS and NMOS transistor sizes [3]. Domino gates have a fixed keeper transistor size to pull-down network transistor size ratio of 1/6. This ratio is chosen for dynamic logic because insignificant changes in delay or power are observed with smaller ratios.

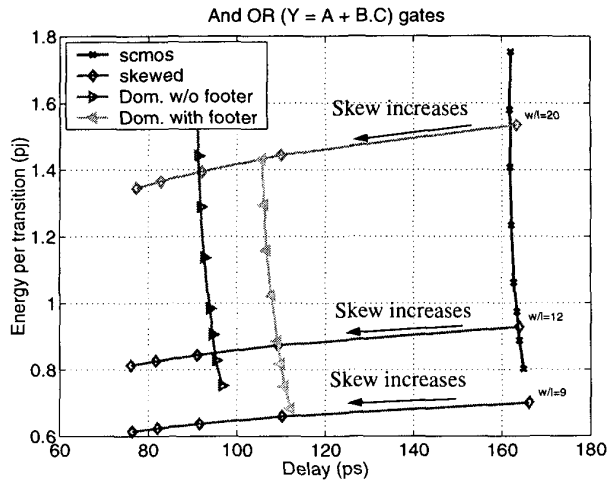


Fig. 8. AND-OR energy vs. delay

Fig. 8 compares the energy per transition vs. delay curves for two cascaded two input NAND circuits forming the AND-OR structure. This structure drives another NAND gate of the same size as a load. The curve for static CMOS gates is obtained by changing the overall sizes of the three gates. The vertical nature of these curves shows that the gate sizes are large enough that further improvement in performance by sizing alone is negligible. Similar curves are obtained for Domino gates, which consist of a Domino inverter followed by a skewed (skew ratio 4) static inverter for both Domino gates with and without footer [8]. However, footerless Domino requires additional clock generation with additional power overhead that cannot be taken into account in this simulation.

The curves for skewed gates show fast gate delay versus energy dissipation. They are obtained by varying the skew of the gates while keeping the sum of transistor widths constant. Three curves at different total widths are plotted with the skew being varied from 1 to 5. These curves indicate the degree to which the static CMOS curve can be shifted as the skew ratio increases. Substantial improvement in delay is obtained without compromising the energy per transition.

5. Dynamic noise immunity

Because of high gain of complementary CMOS circuits the static noise margin of skewed circuits - the point where the gain is unity - is close to the input trip point voltage. The dependency of the trip point of an inverter on the skew is shown in Fig. 2. Such a dependency provides a trade-off between the noise margin and fast transition time as the skew changes.

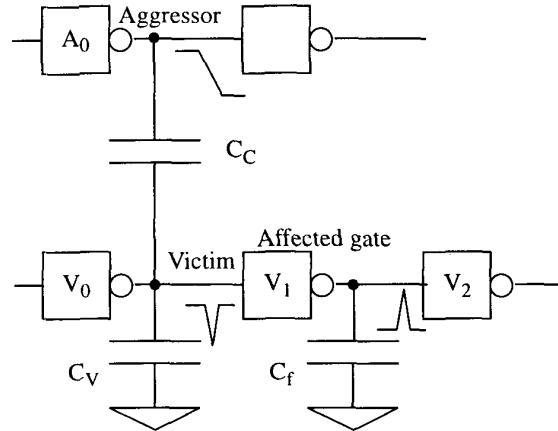


Fig. 9. Coupling noise in circuits

For high-performance precharge-evaluate circuits the static noise margin may not be the only metric for measuring the gate robustness. Static noise margins are important for rejecting voltage offset created on the output nodes due to leakage and noise on power supply lines. However, it does not adequately address the problem of capacitive coupling noise [3], [9].

In order to evaluate coupling noise we used the dynamic noise immunity model proposed in [3], [9]. In this section we present a circuit structure that is used to evaluate the robustness of a gate. Fig. 9 shows the circuit structure with coupling noise. An aggressor gate A_0 forces a transition from high to low on its output. This transition is coupled from the aggressor to a *victim node* driven by gate V_0 . The output of gate V_0 must be high for a noise problem to occur. The strength of the noise spike at the victim node is dependent on coupling coefficient:

$$K_C = \frac{C_C}{C_C + C_V}$$

The amplitude of the spike also depends on the rise or the fall time of the aggressor and the drive strength of gate V_0 .

The noise voltage induced at the output of victim gate by itself does not cause a failure until it is propagated across *affected gate* V_1 . If the output voltage of V_1 rises above the noise threshold determined by static noise margin of *succeeding gate* V_2 , we assume that a failure in functionality occurs.

We evaluate the dynamic noise immunity of standard static CMOS circuits, skewed and Domino circuits for simple inverters. The same HSPICE models for 0.25 μm CMOS technology with 2.5 V supply voltage were used for simulation

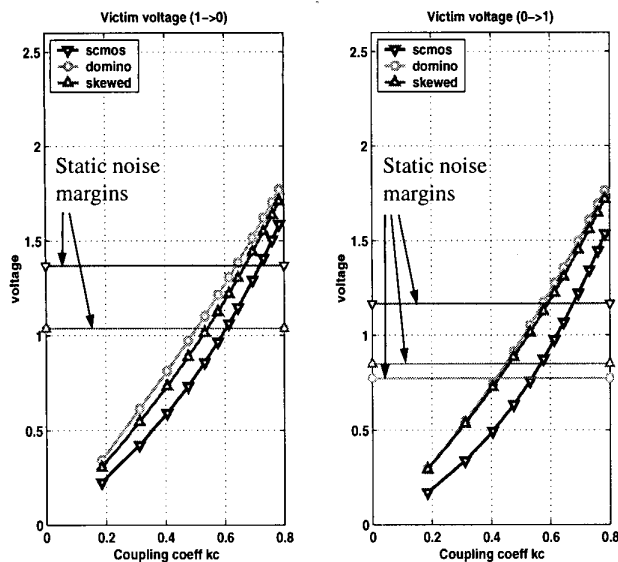


Fig. 10. Peak noise voltage on the victim node

The peak voltage of coupled noise on the victim node is shown in Fig. 10. The left and right charts show maximum voltage of coupling spike for high-to-low transition and for low-to-high transition, respectively. In the case of Domino logic, the left chart shows the effect of coupling to the dynamic node, while the right chart shows the coupling to the output of the skewed inverter following the Domino gate. For skewed gates left and right charts correspond to gates that are skewed for fast falling transition, and those that are skewed for fast rising transition, respectively.

Peak voltages versus coupling coefficient K_C are obtained under the assumption that the total victim capacitance C_V is 25 fF. Domino and skewed gates are assumed to be precharged when the aggressor transition occurs. A skew of four is imposed on the skewed gates and Domino output inverter, whereas the keeper is sized to have a size of a sixth of the pull-down network of Domino gates. All gates have similar average transistor size of 2.0 μm .

Fig. 10 also shows the static noise margins of the respective affected gates as thin horizontal lines. Static noise margins for Domino and skewed gates on the left chart coincide. All voltages are expressed with reference to the victim node voltage in steady state.

It is clear that a stronger drive provided on the victim node decreases the strength of the spike for static gates. Very high values of $C_C > 45$ fF for both falling and rising transitions are required before the trip voltage of the affected gate is crossed.

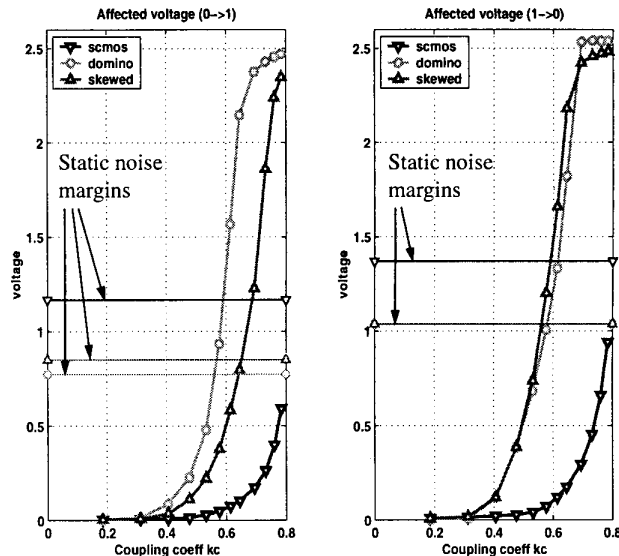


Fig. 11. Peak noise voltage on the output of affected gate

The left chart shows that Domino exhibits slightly higher peak voltage than the skewed gates primarily because the victim node is very weakly driven by a keeper device.

A coupling capacitance C_C of 22 fF is needed for the static noise margin to be exceeded for Domino for high-to-low transition, while C_C must exceed 26 fF for the case of skewed logic. For low-to-high transition, the peak noise voltages on the respective victim nodes for Domino and skewed circuits almost coincide because the victim nodes are driven by the same skewed inverter with a skew of four. Approximately 15 fF of coupling capacitance value is required to exceed the static noise margin of the affected gate in the case of Domino logic and 20 fF in the case of skewed logic.

The peak noise voltages at the output of the affected gate are shown in Fig. 11. Simulation conditions are identical to those in previous figure.

The static noise margins of the respective succeeding gate (V_2 in Fig. 9) are shown as thin horizontal lines. Static noise margins for Domino and skewed gates on the right chart coincide.

Static CMOS gates clearly offer very high degree of noise immunity for both high-to-low and low-to-high transitions. A failure occurs only when $C_C > 80$ fF.

C_C values greater than 28 fF cause a failure on the input of affected Domino gate in the case of low-to-high noise spike on the affected node. For high-to-low noise spike 30 fF coupling capacitance value is required for a failure to occur.

In comparison skewed gates need $C_C > 42$ fF to cause a failure in the case of low-to-high noise spike. In the other case the results for Domino are similar to results for skewed logic because the peak noise voltages on the respective victim nodes for Domino and skewed circuits almost coincide (right chart in Fig. 10). Approximately $C_C=30$ fF is required to cause a failure.

6. Wallace tree multiplier

In order to compare skewed logic and Domino circuits we simulated a 16 x 16 bit pipelined multiplier for both circuit styles using TSMC models for 0.25 μ m CMOS technology with 2.5V supply voltage. The multiplier consists of a Booth encoder, a Wallace tree, and the final adder. The latency of the multiplier is two cycles. During the first cycle the Booth encoder produces partial products and Wallace tree sums the partial products. Final summation is performed in the second cycle by the final carry select adder. Both circuits were optimized for highest possible performance. Simulation results are summarized in Table 1. All data are presented for highest possible clock rate.

Both Domino and skewed circuit achieve the same clock rate. Although logic power consumption of the skewed circuit is greater due to a larger number of transistors, the clock power consumption of Domino circuit is significantly larger than that of skewed circuit. Overall, skewed logic multiplier has a lower power consumption in comparison to that of Domino logic. Furthermore, a peak clock driver current of the skewed circuit is reduced by 34% compared to that of the Domino circuit because of lower clock load capacitance. Logic peak current of skewed logic is also 21% lower because precharge process is distributed over time, whereas in Domino circuits all gates are precharged simultaneously. Reduced peak current means reduced power supply/ground line noise.

Table 1: Multiplier simulation results

Parameter	Domino	Skewed logic
Clock cycle, ns	1.39	1.39
Logic power, mW	162.5	179.8
Clock power, mW	90	62
Total power, mW	252.5	241.8
Logic peak current, mA	194	154
Clock peak current, mA	584	383
Number of transistors	16389	21689
Total width, μ m	22939	23561

7. Conclusions

This paper describes a new noise immune high-performance low-power skewed static logic circuit family and its variations. Skewed circuits have better noise immunity than Domino circuits while the performance of skewed logic is comparable to that of Domino. Hence, skewed circuits are more suitable for high-performance low-power/low-voltage applications. Another advantage of skewed logic is reduced clock capacitance and clock power dissipation. Peak current of power supply/ground lines is also reduced by as much as 34%.

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