

Repeater Block Planning under Simultaneous Delay and Transition Time Constraints

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ABSTRACT

We present a solution to the problem of repeater block planning under both delay and signal transition time constraints for a given floorplan. Previous approaches have considered only meeting the target delay of a net. However, it has been observed that the repeater planning for meeting the delay target can cause signals on long interconnects to have very slow transition rates. Experimental results show that our new approach satisfies both timing constraints for an average of 79% of all global nets for six MCNC benchmark floorplans studied (at 1GHz frequency), compared with an average of 22% for the repeater block planner in [11].

1. INTRODUCTION

With the continued scaling of VLSI technology, interconnects have begun to play a dominant role in determining system performance, power, reliability and cost. To ensure timing closure of deep submicron designs, it is important to consider the impact of interconnects as early as possible in the design flow. Among the several techniques reviewed in [6], repeater insertion has been found to be one of the most effective methods for optimizing signal delay [12; 9] and slew rate [9], and for minimizing noise [2; 4]. Until recently, the option of inserting repeaters was considered only for post-placement optimization. Some recent studies [7; 11] incorporated repeater planning at the floorplanning stage. There are a few advantages in planning for repeaters at the floorplanning stage. Floorplanning, being the first step in the physical design flow, could have the most significant impact on overall solution quality. Moreover, the size of the problem is much smaller (as compared to place-and-route), permitting a more effective search of the design space.

The repeater block planning in [7; 11] was done for delay optimization alone. However, it is also of crucial importance to maintain fast transition time (the inverse of slew rate) of the signal at the receiver and along the net [9; 4] for high signal integrity. Otherwise, a slow transition on a net is highly susceptible to coupling noise injection from fast-transition signal lines in its vicinity. Moreover, if the length of the net between two successive repeaters is too long, the interconnect resistance becomes comparable to the driver resistance. This effectively decouples the receiver from the driver and makes the receiver highly susceptible to any attacking signals.

To avoid such reliability issues, design guidelines on most large designs require signal transition times to be no slower than a specified value. As a rule of thumb, the allowed signal transition time is between 10–15% of the clock cycle time for the design. The repeater planning solutions of [7; 11] did not consider the planning of repeaters for signal transition time constraint. As a result, even

though the target delay (as defined by 50% input to 50% output) of a net may be satisfied, the repeater solution may not maintain the required signal transition rate. SPICE simulations showed that the algorithm described in [11] satisfies both the constraints on 22% of the nets on the average (at a frequency of 1GHz). In contrast, the algorithm in [11] has an average completion rate of 85% when only delay constraints are considered.

In this paper, we formulate the problem of repeater block planning under both delay and rise/fall time constraints for interconnect-centric floorplanning. We introduce the concept of *independent feasible region* for repeater insertion under a signal transition constraint for a 2-pin net and derive an analytical formula for its computation. We also introduce the idea of independent feasible regions under both delay and signal transition constraints—an enabling concept to our repeater planning algorithm. Experimental results show that our algorithm meets both the rise time and delay constraints on 79% of the nets on the average (at a frequency of 1GHz). We also observe that, in general, a much larger number of repeaters is needed to meet both types of timing constraints, a strong justification for an early planning of repeater insertion.

2. PROBLEM FORMULATION

In this work, we study the following *repeater block planning problem*: Given an initial floorplan, delay constraints on each net, and the transition time requirements, find the number, location, assignment and size of the repeater blocks to be inserted in order to meet the delay and transition time requirements. While the primary objective of the *repeater block planner* is to meet the delay and transition time constraints for all nets, it is also important to keep the number of repeater blocks and the increase in chip area within tolerable limits.

We assume that repeaters may not be placed inside the circuit modules (i.e. the modules are considered to be hard IP blocks). Repeater insertion is allowed only in the available channel space defined between the circuit modules and on the common boundaries of any two adjacent modules. To reduce the total wire length of the final routing solution, our repeater block planner considers repeater insertion along non-monotone detour routes (out of the bounding box of a net), only when monotonic paths within the bounding box fail to yield a repeater insertion solution.

3. FEASIBLE REGION COMPUTATION

In this section, we introduce the idea of *common independent feasible region* (IFR(D,R)) for repeater placement under simultaneous delay and signal transition timing constraints and obtain an expression for computing its width. We define the common independent feasible region for a repeater to be the region where it can

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be placed such that both constraints of the net are satisfied, assuming that the other repeaters are also located within their respective IFR(D,R)s.

3.1 Preliminaries

First, we present the definitions and expressions that will be used in stating the main results for IFR(D,R) computation. Each driver or repeater is modeled as a switch-level RC circuit, and the Elmore delay formula [8] is used for delay and transition time computations. The notation for the physical parameters of the interconnect and repeater we use in this paper is as follows:

- r : wire resistance per unit length;
- c : wire capacitance per unit length;
- T_b : intrinsic repeater delay;
- C_b : repeater input capacitance;
- R_b : repeater output resistance.

Given a wire segment of length l with driver output resistance R and sink capacitance C , its Elmore delay is defined as

$$D(R, C, l) = K_d \times \left\{ \left(\frac{rc}{2} \right) l^2 + (Rc + rC)l + RC \right\},$$

and its maximum signal transition time [3] is defined as

$$R(R, C, l) = K_r \times \left\{ \left(\frac{rc}{2} \right) l^2 + (Rc + rC)l + RC \right\}.$$

Typical values for the constants K_d and K_r are 0.69 and 2.2, respectively [3].

Using the Elmore delay expression, the delay of a single source, single sink net N (two pin net) of length l with n repeaters can be expressed as,

$$D_{net}^N(x_1, x_2, \dots, x_n, l) = D(R_d, C_b, x_1) + D(R_b, C_s, l - x_n) + \sum_{i=2}^{n-1} D(R_b, C_b, x_i - x_{i-1}) + nT_b,$$

where R_d is the driver resistance, C_s is the sink capacitance, and x_i is the location of the i^{th} repeater.

The optimal locations of the n repeaters for delay minimization of the net as shown in [1] are

$$x_i^* = (i-1)y^* + x^* \quad i \in \{1, 2, \dots, n\},$$

where

$$x^* = \frac{1}{n+1} \left(l + \frac{n(R_b - R_d)}{r} + \frac{(C_s - C_b)}{c} \right),$$

$$y^* = \frac{1}{n+1} \left(l - \frac{(R_b - R_d)}{r} + \frac{(C_s - C_b)}{c} \right).$$

We denote the optimal delay for the net N , of length l with n repeaters by

$$D_{opt}^N(n, l) = D_{net}^N(x_1^*, x_2^*, \dots, x_n^*, l).$$

3.2 IFR for Transition Time Constraint

The independent feasible region for signal transition time requirement, IFR(R) for a repeater is defined as the region where it can be placed such that the maximum transition time at any point along the net does not exceed the allowable signal transition time.

Formally, we define the independent feasible region under signal transition time constraint (IFR(R)) for the i^{th} repeater of a net N as,

$$IFR(R)_i = (x_i^{\otimes} - W_{IFR(R)}/2, x_i^{\otimes} + W_{IFR(R)}/2) \cap (0, l),$$

such that $\forall (x_1, x_2, \dots, x_i, \dots, x_n) \in IFR(R)_1 \times IFR(R)_2 \times \dots \times IFR(R)_n$ and

$$\max \{ R(R_d, C_b, x_1), \{ R(R_b, C_b, x_{i+1} - x_i) \mid 1 \leq i < n \}, R(R_b, C_s, l - x_n) \} \leq R_{tgt}^N.$$

Here, $W_{IFR(R)}$ and R_{tgt}^N respectively denote the width of independent feasible region $IFR(R)_i$ and the target signal transition time associated with the net. Also note that, as illustrated in Figure 1, x_i^{\otimes} in the above definition represents the center of IFR(R) for the i^{th} repeater. We shall show later in Theorem 1 how x_i^{\otimes} is computed.

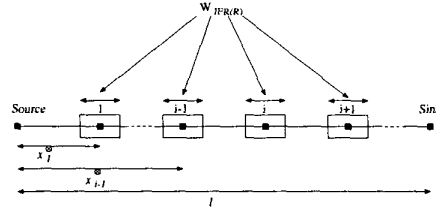


Figure 1: Independent feasible regions for signal transition time.

To allocate an equal degree of freedom to each repeater in the net we choose the IFR(R) intervals to be of equal width (see Figure 1).

Define $L(R, C, R_{tgt}^N)$ to be the maximum length of a net (having driver output resistance R , sink capacitance C) such that the signal transition time at the sink is no more than R_{tgt}^N . Using the Elmore based formulation for the signal transition time it is easy to see that,

$$L(R, C, R_{tgt}^N) = \frac{\sqrt{(Rc + rC)^2 - 2rc(RC - \frac{R_{tgt}^N}{K_r})} - (Rc + rC)}{rc}.$$

We have the following theorem for the width and location of the IFR(R) of repeaters on a net.

THEOREM 1. For signal transition time constraint, R_{tgt}^N , the width of the independent feasible region for the i^{th} repeater ($i \leq n$) of the net N is

$$W_{IFR(R)} = \frac{l_1 + (n-1)l_2 + l_3 - l}{n},$$

and

$$x_i^{\otimes} = x^{\otimes} + (i-1)y^{\otimes},$$

where $l_1 = L(R_d, C_b, R_{tgt}^N)$, $l_2 = L(R_b, C_b, R_{tgt}^N)$, $l_3 = L(R_b, C_s, R_{tgt}^N)$, $x^{\otimes} = l_1 - W_{IFR(R)}/2$ and $y^{\otimes} = l_2 - W_{IFR(R)}$.

Proof: The following inequalities must hold for the signal transition time constraint to be satisfied on all segments of the net N :

$$x_1^{\otimes} + W_{IFR(R)}/2 \leq l_1,$$

$$x_{i+1}^{\otimes} - x_i^{\otimes} + W_{IFR(R)} \leq l_2, \quad 1 \leq i \leq n-1$$

$$l - x_n^{\otimes} + W_{IFR(R)}/2 \leq l_3.$$

Summing up the $n+1$ inequalities above we obtain:

$$l + nW_{IFR(R)} \leq l_1 + (n-1)l_2 + l_3.$$

Therefore, the maximum value of the width of the IFR(R) is

$$W_{IFR(R)} = \frac{l_1 + (n-1)l_2 + l_3 - l}{n}.$$

For this choice of $W_{IFR(R)}$, the set of inequalities can be replaced by the following equations:

$$x_1^{\otimes} = l_1 - W_{IFR(R)}/2,$$

$$x_{i+1}^{\otimes} - x_i^{\otimes} = l_2 - W_{IFR(R)}, \quad 1 \leq i \leq n-1,$$

$$x_n^{\otimes} = l - l_3 + W_{IFR(R)}/2.$$

Thus, we obtain

$$x_i^{\otimes} = (l_1 - W_{IFR(R)})/2 + (i-1)(l_2 - W_{IFR(R)}). \quad \square$$

COROLLARY 1. For rise/fall time constraint, R_{igt}^N , the minimum number of repeaters needed to meet the constraint is,

$$n_R^{Min} = \lceil \frac{l-l_1-l_3}{l_2} + 1 \rceil.$$

Proof: n_R^{Min} can be obtained by setting $W_{IFR(R)}$ to 0. \square

3.3 IFR for Delay Time Constraint

In [11], the *independent feasible region* (IFR(D)) of a repeater under the delay constraint, has been defined as the region where the repeater can be placed while meeting the delay specification of the net, assuming that the other repeaters are placed within their respective independent feasible regions.

Formally, the independent feasible region under the delay constraint (IFR(D)) for the i^{th} repeater of a net \mathbf{N} can be defined as,

$$IFR(D)_i = (x_i^* - W_{IFR(D)}/2, x_i^* + W_{IFR(D)}/2) \cap (0, l),$$

such that $\forall (x_1, x_2, \dots, x_i, \dots, x_n) \in IFR(D)_1 \times IFR(D)_2 \times \dots \times IFR(D)_n$ and $D_{net}^N(x_1, x_2, \dots, x_n) \leq D_{igt}^N$. Here, $W_{IFR(D)}$ and D_{igt}^N respectively denote the width of independent feasible region $IFR(D)_i$ and the target delay associated with the net.

The width of the independent feasible region under delay constraint, denoted by $W_{IFR(D)}$, is shown to be [11]

$$W_{IFR(D)} = 2 \cdot \sqrt{\frac{D_{igt}^N - D_{opt}^N(n, l)}{rc(2n-1)}}.$$

We have the following result for the number of repeaters that can be inserted in a net to meet the delay constraint.

THEOREM 2. For delay constraint, D_{igt}^N , the number of repeaters that may be inserted to meet the constraint ranges from n_D^{Min} to n_D^{Max} , where

$$\begin{aligned} n_D^{Min} &= \max\left(0, \frac{-B - \sqrt{(B^2 - 4AC)}}{2A}\right), \\ n_D^{Max} &= \frac{-B + \sqrt{(B^2 - 4AC)}}{2A}, \\ A &= R_b C_b + T_b, \\ B &= D_{igt}^N + \frac{r}{c}(C_b - C_s)^2 + \frac{c}{r}(R_b - R_d)^2 - (rC_b + cR_b)l \\ &\quad - T_b - R_d C_b - R_b C_s, \\ C &= \frac{1}{2}rc l^2 + (rC_s + cR_d)l - D_{igt}^N. \end{aligned}$$

If $n_D^{Max} \leq 0$, the delay constraint on the net cannot be met by inserting repeaters of this type alone.

Proof: The optimal delay obtained by insertion of n repeaters is

$$\begin{aligned} D_{opt}^N(n, l) &= D(R_d, C_b, x_1^*) + D(R_b, C_s, l - x_n^*) \\ &\quad + \sum_{i=2}^{n-1} D(R_b, C_b, x_i^* - x_{i-1}^*) + nT_b. \end{aligned}$$

Substituting the expressions for x_i^* and setting D_{opt}^N to D_{igt}^N , we can rewrite the above equation as a polynomial in n as follows,

$$An^2 + Bn + C = 0.$$

Solving this quadratic equation, we obtain the range of n . The lower bound n_D^{Min} has been derived in [7]. \square

3.4 Common Independent Feasible Region

The common independent feasible region (IFR(D,R)) for repeater i of net \mathbf{N} under both delay and signal transition time constraints is defined as the maximal region where the repeater can be placed such that both the constraints can be satisfied, assuming that the other repeaters are placed within their respective common independent feasible regions. Let the number of repeaters required to meet both the constraints be $n_{D,R}$. Clearly,

$$\max(n_R^{Min}, n_D^{Min}) \leq n_{D,R} \leq n_D^{Max}.$$

Both the constraints cannot be met by repeater insertion if

$$n_R^{Min} > n_D^{Max}.$$

For a fixed value of $n_{D,R}$ in the feasible range, the IFR(D,R) for the i^{th} repeater ($IFR(D,R)_i$) on the net is the region common to both $IFR(R)_i$ and $IFR(D)_i$. Define, $W_{min} = \min(W_{IFR(R)}, W_{IFR(D)})$, $\delta_i = |x_i^* - x_i^{\otimes}|$ and $\delta_w = |W_{IFR(R)} - W_{IFR(D)}|$. The width of $IFR(D,R)_i$ is

$$W_{IFR(D,R)_i} = \begin{cases} W_{min} & ; \text{ if } \delta_i \leq \delta_w/2, \\ W_{min} - \delta_i + \delta_w/2 & ; \text{ if } \delta_w/2 \leq \delta_i \\ & \leq (W_{IFR(R)} + W_{IFR(D)})/2, \\ \text{undefined} & ; \text{ otherwise.} \end{cases}$$

It can also be shown that $\min_{1 \leq i \leq n_{D,R}} (W_{IFR(D,R)_i})$ occurs at $i = 1$ or $i = n_{D,R}$.

To fix the number of repeaters to be inserted on the net we choose the value of $n_{D,R}$ that maximizes the minimum width of $IFR(D,R)_i$. To find this $n_{D,R}$ we search over all allowable values of $n_{D,R}$. Based on the above observation, such a search can be efficiently accomplished.

4. REPEATER BLOCK PLANNING

In this section we describe our repeater block planning algorithm. The algorithm takes the initial floorplan, delay and transition time constraints on the global nets as inputs. It determines the location, assignment and size of repeater blocks to be inserted in the channel space between the circuit modules such that the delay and transition time constraints can be satisfied.

Figure 2 gives the overall flow of our repeater block planning algorithm. Step 1 divides the available channel space, as done in [7; 11], into a set of repeater block tiles, where the planning algorithm may insert repeaters to meet both types of timing constraints.

In step 2, the type and number of repeaters to be inserted in each net to satisfy its timing constraints is computed. The repeater type chosen for a net is the *smallest* size repeater that can be used, such that all the repeaters on the net have a non-empty IFR(D,R). A larger size repeater increases the maximum length of the net that can be driven by a repeater without violating the transition time constraint. However, it occupies a larger area, and has a higher input capacitance. We constrain all the repeaters on a net to be of the same size. The number of repeaters needed is then obtained by searching the common feasible range of repeater numbers for delay and transition time requirements. The chosen value of $n_{D,R}$ maximizes the minimum IFR(D,R) width (see Section 3.4).

Steps 4–6 find the set of repeater-block tiles into which each repeater can be placed. Let \mathbf{B} be the set of repeaters that need to be inserted for timing closure. For $b \in \mathbf{B}$ define \mathbf{S}_b to be the set of repeater-block tiles into which it can be placed. The set \mathbf{S}_b is called the Candidate Repeater Blocks (CRB) set of b . To construct the CRB set for each repeater we first consider the monotone routes within the bounding box of the net. In the preceding section, our discussions on IFR(D,R) were limited to a one dimensional line.

Repeater Block Planning Algorithm	
1.	Divide the channel space into repeater block tiles;
2.	Find type of repeater and $n_{D,R}$ for each net N
3.	Compute IFR(D,R) for each repeater $b \in \mathbf{B}$;
4.	foreach net N
5.	foreach repeater b in net N
6.	Obtain CRB set S_b ;
7.	If $\exists (S_b = \emptyset)$ for a net N
8.	Find shortest detour path;
9.	Obtain S_b along detour path;
10.	Generate the bipartite graph G ;
11.	While there exists a repeater to be assigned do
12.	Delete the highest cost edge of G ;
13.	Update edge costs;
14.	Assign repeater to a CRB if required;

Figure 2: Repeater block planning algorithm.

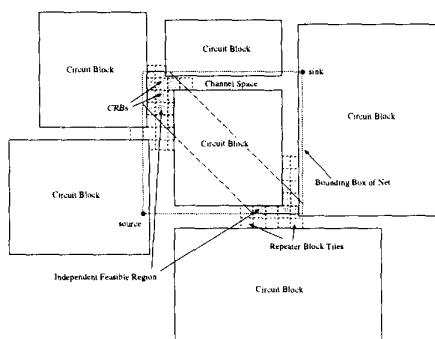


Figure 3: Creation of candidate repeater blocks.

For repeater block planning during floorplanning, we compute a two dimensional region where the repeater can be placed by taking the union of the 1-D feasible regions of all monotonic Manhattan routes between source and sink. The intersection of the two dimensional IFR(D,R) of a repeater with the repeater block tiles define the CRB set of that repeater (see Figure 3).

When at least one of the repeaters to be placed along the monotone route has an empty CRB set, *non-monotone detour routes* are considered. Steps 7–9 construct the CRB sets for repeaters to be placed along the shortest detour route. In step 8, the shortest detour path is obtained. This is done by generating a graph from the initial floorplan by extending the module boundaries and using Dijkstra's shortest-path algorithm to find the shortest path. Using the length of this path, the optimal number of repeaters ($n_{D,R}$) to be inserted to meet the timing constraints is computed. The next step computes the width of the IFR(D,R) for each repeater along this path. Step 9 uses this width to generate the CRB set for the net N .

Each repeater has several CRBs to which it may be assigned (see Figure 3). The repeater block planning algorithm must then choose a single CRB to place the repeater b . The set of all possible assignments of repeaters to CRBs is modeled as a bipartite graph $G = (V_1 \cup V_2, E)$, where V_1 is the set of repeaters, V_2 is the set of CRBs and $E \subset V_1 \times V_2$. $(b, c) \in E$ if and only if repeater b can be placed in CRB c . Step 10 constructs the bipartite graph G .

We use a *iterative deletion* [10] approach to obtain the assignment for each repeater. Steps 12–14 prunes the graph G by removing an *incompatible* repeater assignment or edge in each iteration. An edge is said to be *incompatible* if the corresponding assignment

	Description	Value
r	wire resistance per unit length ($\Omega/\mu\text{m}$)	0.075
c	wire capacitance per unit length (fF/ μm)	0.118

Table 1: Interconnect parameter values.

	Description	Repeater 1	Repeater 2
T_b	intrinsic delay (ps)	36.4	36.4
C_b	input capacitance (pF)	0.0234	0.0468
R_b	output resistance (Ω)	180	90

Table 2: Repeater parameter values.

of the repeater to the CRB results in a repeater block planning solution that has too many repeater blocks. To accomplish the task of deleting incompatible repeater assignments, the edges in G have dynamic weights. Intuitively, for an edge $e = (b, c)$ the repeater block cost is lower if the number of in-degree of the CRB c is high—implying that repeaters in this block can be shared by several nets. An edge of a higher cost implies that the repeater block assignment is likely to be incompatible with the rest, and the iterative deletion operation in Steps 12–14 seeks to remove the highest cost edge in the current G . As edges are iteratively deleted from the graph G , the expected repeater block count for the floorplan is modified. This change is reflected onto the edge costs of the graph at every iteration, thus making the edge weights dynamic. The algorithm terminates when a unique CRB has been assigned to each repeater.

5. EXPERIMENTAL RESULTS

We have implemented our repeater block planning algorithm using C on a SUN UltraSPARC II machine. In this section we present the details of our experimental set up and the results obtained. The interconnect and repeater parameters and the Elmore delay model have been described in Section 3.1. The values (see Table 1 and Table 2) used for these parameters are based on a $0.18\mu\text{m}$ technology used in [7]. The area of Repeater 2 is assumed to be twice that of Repeater 1. We have assumed the availability of two types of repeaters for our experiments. However our Repeater Block Planner can, in general, use an arbitrary number of repeater types.

We report the results of our repeater block planner for 6 MCNC [5] benchmark circuits. The relevant details of these benchmarks are shown in Table 3.

As stated in Section 2, in this work we focus on solving the problem of repeater block planning for two-pin (single source/single sink) nets. For decomposing multi-pin nets into two pin nets we choose one of the pins to be the source and all the others to be sinks. The initial floorplans of the MCNC benchmark circuits used for this work are the same as those used in [7; 11].

Since the MCNC benchmarks do not come with any timing information, we assign target delays to each two-pin net as follows. For each net we compute the optimal delay obtainable by repeater insertion T_{opt} [1] and then randomly assign a target delay between

Circuit	Modules	Nets	2-Pin Nets
apte	9	97	172
hp	11	83	226
xerox	10	203	455
ami33	33	123	363
ami49	49	408	545
playout	62	2506	2150

Table 3: Details of MCNC benchmarks.

Circuit	MET/ MET[11]	N _{REP} / N _{REP} [11]	δA / δA [11]	TCPU(s)/ TCPU(s)[11]
apte				
600MHz	124/79	441/220	0.93/0.40	14.7/9.1
800MHz	121/49	540/143	1.17/0.27	12.3/9.5
1000MHz	117/31	670/65	1.44/0.13	10.2/10.0
1200MHz	112/24	792/26	1.60/0.06	10.2/10.0
1500MHz	103/19	1194/20	2.66/0.05	17.4/10.0
hp				
600MHz	205/104	673/193	1.02/0.34	35.1/30.0
800MHz	198/56	844/90	1.48/0.17	34.1/31.2
1000MHz	185/34	1058/50	1.94/1.00	34.2/32.1
1200MHz	172/25	1239/18	2.21/0.04	35.1/33.3
1500MHz	161/16	2145/16	3.78/0.04	35.6/33.1
xerox				
600MHz	395/231	1129/282	2.18/0.61	39.9/31.0
800MHz	382/118	1392/139	2.88/0.26	35.4/32.4
1000MHz	355/79	1701/49	3.54/0.20	31.1/32.8
1200MHz	330/63	1999/28	4.19/0.16	33.6/32.8
1500MHz	275/50	3574/20	7.53/0.15	50.4/34.1
ami33				
600MHz	341/226	777/314	1.15/0.55	39.0/60.1
800MHz	327/116	984/165	1.76/0.30	45.0/61.0
1000MHz	305/69	1257/101	2.48/0.18	52.0/65.0
1200MHz	283/50	1569/64	2.99/0.12	53.1/66.0
1500MHz	252/36	2549/54	5.15/0.10	58.0/67.0
ami49				
600MHz	512/392	891/377	1.48/0.69	115.0/240.1
800MHz	497/260	1158/254	2.15/0.49	129.0/184.2
1000MHz	462/180	1409/201	2.79/0.39	148.1/203.0
1200MHz	441/134	1814/144	3.45/0.29	148.0/210.0
1500MHz	392/115	2947/136	5.73/0.27	167.0/218.1
playout				
600MHz	2055/1810	3098/1410	5.75/1.31	585.0/582.1
800MHz	1920/1400	4210/1361	5.92/1.20	581.0/577.9
1000MHz	1750/752	4710/1105	6.91/1.01	577.4/571.9
1200MHz	1680/411	5292/681	7.25/0.94	580.1/581.3
1500MHz	1590/211	6051/311	8.71/0.84	591.7/593.4

Table 4: Comparison of repeater block planning solutions.

1.05 and 1.20 times T_{opt} as was done in [7; 11]. The signal transition time target (20-80%) is assigned as 10% of the clock period.

In Table 4 we report the following results from our repeater block planning algorithm for various frequencies of operation: (i) number of nets for which both delay and transition time constraint are satisfied, MET; (ii) the total number of repeaters inserted to meet the constraints, N_{REP}; (N_{REP} is the number of repeaters of type 1 plus two times the number of type 2 repeaters.) (iii) the chip area increase, δA expressed as a percentage of the original chip area; and (iv) CPU time required, TCPU. We include in the table results obtained from the Repeater Block Planner described in [11]. For a fair comparison, the algorithm of [11] has been augmented to consider both detour paths and multiple types of repeaters.

Compared to [11], the number of nets that meet the delay and transition time requirements is significantly higher. The success rates of meeting the timing constraints range from 85% (for ami49) to 68% (for apte) at a frequency of 1GHz. In contrast, the completion rates for the same examples by the Repeater Block Planner in [11] range from 15% (for hp) to 35% (for playout). On the average the algorithm described in [11], which considers only the target delay, has a completion rate of 22%, whereas our repeater planner meets both the constraints on 79% of nets (at 1GHz). The experimental results show that the repeater block planner must consider the target signal transition time during repeater planning.

The number of repeaters needed to meet both delay and transition time requirements is significantly higher than the number of repeaters needed to meet only the delay constraints. This strongly

supports our claim that transition time constraint must be considered during the planning process, as it will be very difficult to introduce additional repeaters (or significantly size up repeaters) at a later stage, without significantly affecting the floorplan.

We also observe that the completion rate for all the benchmark circuits fall as the frequency of operation increases. For example, xerox has a completion rate of 87% at 600MHz, but only 60% at 1.5GHz. The number of repeaters that need to be inserted and the resultant chip area increase are also higher at higher frequencies. The methods used in this paper and in [7] and [11], of planning for repeater blocks, starting at an initial floorplan, seem to be inadequate. This leads us to conclude that for large designs in the ultra-high frequency domain, new and improved metrics for floorplanning will be needed.

6. CONCLUSION

We have presented a repeater block planning algorithm that uses the concept of independent feasible regions to meet both the delay and transition time constraints on a net. Experimental results show that our technique performs significantly better than repeater planning methods that consider only the delay constraint.

7. REFERENCES

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