

Short-Circuit Power Analysis of an Inverter Driving an RLC Load

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ABSTRACT

The demand for powerful computational machines using scaled technologies has brought power dissipation to the forefront. Hence, there is a need to accurately model power dissipation in such technologies where both capacitive and inductive effects are important. In this paper, we accurately model short-circuit power dissipation of an inverter driving an RLC load. A closed form expression is derived based on the analysis of the inverter in different conducting regions during an input transition. We applied the proposed model to a 0.18 μm Cu technology, and compared the result with SPICE simulation. Our model has an accuracy of 90% with respect to SPICE.

I. INTRODUCTION

With the development of sub-micron technology, more transistors are integrated on a single chip, increasing the power consumption to a level that necessitates low power design techniques. Hence, an accurate model is needed to determine the performance and power consumption of a circuit. The power consumption of a circuit can be divided into static and dynamic components. The static component is mainly due to reverse-bias diode and sub-threshold leakage currents [7]. Accurate analysis of leakage power for deep sub-micron technologies can be found in [8]. Dynamic power in turn consists of two components: switching and short-circuit. Although switching power has been well characterized, short-circuit power has not been fully studied. Sakurai et al [6] have shown that short circuit power is becoming more important for scaled technologies. However, no good short circuit power model exists under realistic loads.

Because of technology scaling, interconnects are playing a more important role in determining the performance and power dissipation of a chip. Accurate modeling for future technologies requires the consideration of inductive parasitics. In [2], an analytical expression was derived for an inverter driving a load capacitance considering the short-channel effect and using α -power law [1]. The technique applied the method of dividing the transition period into different regions based on the conducting status of each transistor. In [4], a CRC load replaced the simple capacitive load. For simplicity, the authors used Shoji's model [5], in which the transistor current is not continuous from linear region to saturation region. In this paper, we consider realistic RLC load under α -power law [1] to accurately estimate short-circuit power for deep sub-micron technologies. A closed form expression for short-circuit energy is also derived.

In section II, a detailed derivation of the short-circuit energy model is given based on analysis of the transient response of an inverter driving an RLC load. In section III, we compare short-circuit energy

from our model to the results from SPICE simulation for a 0.18 μm Cu technology. Our model has an error margin of 10%. The conclusions are given in Section IV.

II. MODEL DESCRIPTION

The circuit we analyzed in this paper is shown in Figure 1. It is an inverter driving an RLC load, with R , L , and C_L the lumped values of the load resistance, inductance, and capacitance respectively. We also considered the gate-to-drain coupling capacitance C_M of the inverter. The input voltage of the inverter is denoted by V_{in} , and the voltage at the output of the inverter is V_x . The output voltage on the load capacitance C_L is denoted by V_{out} . We derived short-circuit power model for a rising input transition. Similar expressions can be derived for falling transitions.

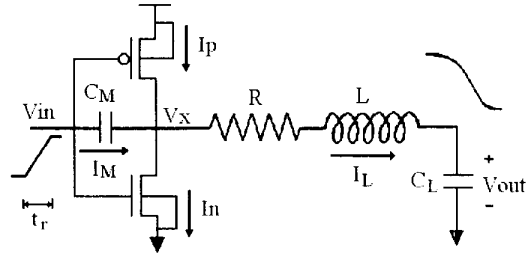


Figure 1. An inverter driving an RLC load

In the following discussions, we use normalized voltage and time. The normalized output voltage of the inverter is $u_x = V_x/V_{DD}$, and the normalized time is expressed by $x = t/t_r$, where t_r is the input transition time. The normalized input voltage is $u_{in} = V_{in}/V_{DD}$. During a rising transition, the input voltage of the inverter can be expressed as:

$$V_{in} = \begin{cases} x \cdot V_{DD}, & 0 \leq t \leq t_r, \\ V_{DD}, & t > t_r, \end{cases} \quad \text{i.e.} \quad u_{in} = \begin{cases} x, & 0 \leq x \leq 1, \\ 1, & x > 1. \end{cases} \quad (1)$$

The KCL and KVL equations for the circuit shown in Figure 1 are as follows:

$$\begin{aligned} I_p - I_n + I_M - I_L &= 0, \\ I_M &= C_M \frac{d(V_{in} - V_x)}{dt}, \\ I_L &= C_L \frac{dV_{out}}{dt}, \\ V_x - V_{out} &= RI_L + L \frac{dI_L}{dt}. \end{aligned} \quad (2)$$

From Eqn. (2), we get the differential equation for the normalized output voltage of the inverter u_x as:

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$$\begin{aligned} & \frac{C_M C_L L V_{DD}}{t_r^3} \cdot \frac{d^3 u_x}{dx^3} + \frac{C_M C_L R V_{DD}}{t_r^2} \cdot \frac{d^2 u_x}{dx^2} + \frac{(C_M + C_L) V_{DD}}{t_r} \cdot \frac{du_x}{dx} \\ & = \frac{C_L L}{t_r^2} \cdot \frac{d^2 (I_p - I_n)}{dx^2} + \frac{C_L R}{t_r} \cdot \frac{d(I_p - I_n)}{dx} + (I_p - I_n) + \frac{C_M V_{DD}}{t_r}. \end{aligned} \quad (3)$$

We use α -power law [1] for NMOS and PMOS current (I_p and I_n) in Eqn. (3) and solve it for u_x . The drain currents of transistors are:

$$\begin{aligned} I_n &= \begin{cases} 0, & x < n, \\ K_{ln}(x-n)^{\alpha_n/2} \cdot u_x, & u_x < u_{don}, \\ K_{sn}(x-n)^{\alpha_n}, & u_x \geq u_{don}, \end{cases} \\ I_p &= \begin{cases} 0, & x > p, \\ K_{lp}(1-x-p)^{\alpha_p/2} \cdot (1-u_x), & u_x > 1-u_{dop}, \\ K_{sp}(1-x-p)^{\alpha_p}, & u_x \leq 1-u_{dop}. \end{cases} \end{aligned} \quad (4)$$

where

$$\begin{aligned} K_{ln} &= I_{don} \cdot V_{DD} / (V_{don}(1-n)^{\alpha_n/2}), & K_{sn} &= I_{don} / (1-n)^{\alpha_n}, \\ K_{lp} &= I_{dop} \cdot V_{DD} / (V_{dop}(1-p)^{\alpha_p/2}), & K_{sp} &= I_{dop} / (1-p)^{\alpha_p}, \end{aligned} \quad (5)$$

$$\begin{aligned} u_{don} &= \frac{V_{don}}{V_{DD}} \left(\frac{x-n}{1-n} \right)^{\alpha_n/2}, & n &= V_{Thn} / V_{DD}, \\ u_{dop} &= \frac{V_{dop}}{V_{DD}} \left(\frac{1-p-x}{1-p} \right)^{\alpha_p/2}, & p &= |V_{Thp}| / V_{DD}. \end{aligned} \quad (6)$$

In the equations above, we use a subscript n for NMOS transistor and a subscript p for PMOS transistor. V_{Thn} and $|V_{Thp}|$ are the absolute values of the threshold voltages of the NMOS and PMOS transistors, and the normalized threshold voltages of the transistors are n and p , respectively. I_{don} and I_{dop} are the saturated drain currents of the transistors at $|V_{GS}| = |V_{DS}| = V_{DD}$. V_{don} and V_{dop} are the saturated drain voltages of the transistors at $|V_{GS}| = V_{DD}$. The normalized saturation voltages for NMOS and PMOS are denoted by u_{don} and u_{dop} . When $u_x > u_{don}$, NMOS is saturated, whereas PMOS is saturated when $u_x < 1-u_{dop}$.

The transition period of an inverter can be divided into different regions based on the conducting status of NMOS and PMOS transistors [2]. For convenience, the operation regions for a transistor with *input rising transition* [2] is shown here in Figure 2. The x -axis is the normalized time x , and the y -axis is the normalized output voltage u_x . We list the status of NMOS and PMOS for each region in Table 1.

	NMOS	PMOS	u_{oi}	Time
R1	Cutoff	Linear	x	$0 \leq x < n$
R2	Saturation	Linear	x	$n \leq x < x_{sap}$
R3	Saturation	Saturation	x	$x_{sap} \leq x < \min(x_{sam}, 1-p)$
R4	Saturation	Cutoff	x	$1-p \leq x < 1$
R5A	Saturation	Cutoff	1	$1 \leq x < x_{sam}$
R5B	Linear	Linear/cutoff	x	$x_{sam} \leq x < 1$
R6	Linear	Cutoff	1	$\max(1, x_{sam}) \leq x$

Table 1. Operation Regions

During the input rising transition, x_{sap} is the time when PMOS changes from linear operation to saturated operation, and x_{sam} is the time when NMOS changes from saturated operation to linear operation. Depending on the *input transition time*, the output voltage can be any of the curves in Figure 2.

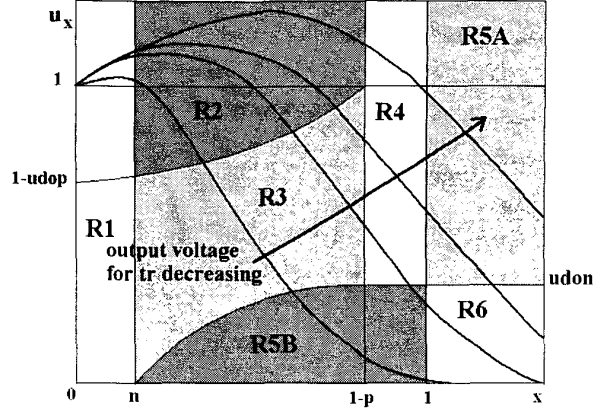


Figure 2. Operation Regions

In the following, we will derive the normalized output voltage of the inverter for each different region the transistor operates in. We use u_{oi} to represent the normalized output voltage for region i .

Region 1: When input voltage is less than NMOS threshold voltage, i.e., $0 \leq x < n$, NMOS transistor is cutoff and PMOS transistor is in linear region. Because of the gate-to-drain coupling capacitance C_M , there is an overshoot of the output voltage, and u_x is slightly greater than 1. The current flow of PMOS in this region is small and negative. From Eqn. (4), we observe that PMOS current is related to u_x in this region, and it is not possible to solve Eqn. (3) analytically. To make Eqn. (3) solvable, we make use of PMOS current at $n/2$ for I_p . Since PMOS current is small in this region, the error introduced by this approximation can be neglected [2]. Based on Eqn. (4),

$$I_p = K_{lp} \left(1 - \frac{n}{2} - p \right)^{\alpha_p/2} \cdot (1 - u_x). \quad (7)$$

Substituting Eqn. (7) into Eqn. (3) and after some manipulations, Eqn. (3) has the following form:

$$A_1 \frac{d^3 u_{oi}}{dx^3} + B_1 \frac{d^2 u_{oi}}{dx^2} + C_1 \frac{du_{oi}}{dx} + D_1 u_{oi} + E_1 = 0. \quad (8)$$

Initially, both V_x and V_{out} are at V_{DD} and there is no current flowing through the device. So, we have

$$u_{oi}|_0 = 1, \quad \frac{du_{oi}}{dx}|_0 = 1, \quad \frac{d^2 u_{oi}}{dx^2}|_0 = F_1. \quad (9)$$

The coefficients in Eqns. (8) and (9) are:

$$\begin{aligned}
A_1 &= C_M C_L L V_{DD} / t_r^3, \\
B_1 &= C_M C_L R V_{DD} / t_r^2 + C_L L \cdot K_{lp} (1-p-n/2)^{\alpha_p/2} / t_r^2, \\
C_1 &= (C_M + C_L) V_{DD} / t_r + C_L R \cdot K_{lp} (1-n/2-p)^{\alpha_p/2} / t_r, \\
D_1 &= K_{lp} (1-n/2-p)^{\alpha_p/2}, \\
E_1 &= -K_{lp} (1-n/2-p)^{\alpha_p/2} - C_M V_{DD} / t_r, \\
F_1 &= -K_{lp} (1-p)^{\alpha_p/2} t_r / C_M V_{DD}.
\end{aligned}$$

Solving Eqn. (8), we get the normalized output voltage u_{x1} in region 1:

$$u_{x1} = -E_1 / D_1 + \kappa_1 e^{q_1 x} \cdot (\cos(r_1 x) + \sin(r_1 x)) + \kappa_2 e^{q_2 x} \times (\cos(r_2 x) + \sin(r_2 x)) + \kappa_3 e^{q_3 x} \cdot (\cos(r_3 x) + \sin(r_3 x)). \quad (10)$$

Coefficients $\kappa_i (i=1,2,3)$ can be computed from the boundary conditions from Eqn. (10):

$$\begin{aligned}
\kappa_1 + \kappa_2 + \kappa_3 - E_1 / D_1 &= 1, \\
\kappa_1 (q_1 + r_1) + \kappa_2 (q_2 + r_2) + \kappa_3 (q_3 + r_3) &= 1, \\
\kappa_1 (q_1^2 + 2q_1 r_1 - r_1^2) + \kappa_2 (q_2^2 + 2q_2 r_2 - r_2^2) \\
+ \kappa_3 (q_3^2 + 2q_3 r_3 - r_3^2) &= F_1.
\end{aligned} \quad (11)$$

$$\begin{aligned}
q_i &= \text{Re}(\text{Root}[D_1 + C_1 x + B_1 x^2 + A_1 x^3 = 0, i]), \quad (i=1,2,3) \\
r_i &= \text{Im}(\text{Root}[D_1 + C_1 x + B_1 x^2 + A_1 x^3 = 0, i]).
\end{aligned} \quad (12)$$

Combining Eqns. (10), (11), and (12), we have the closed form expression for u_{x1} . The output voltage and PMOS current at the boundary between region 1 and region 2, denoted respectively by u_{1n} and $I_{p\text{min}}$, are:

$$\begin{aligned}
u_{1n} &= u_{x1} \Big|_{x=n}, \\
I_{p\text{min}} &= K_{lp} (1-p-n)^{\alpha_p/2} (1-u_{1n}).
\end{aligned} \quad (13)$$

Region 2: When $n \leq x < x_{\text{satp}}$, NMOS is saturated, and PMOS is still in linear region. It has been shown in [2] that a linear approximation for PMOS current in this region is reasonable and the PMOS current simplifies to

$$I_p = I_{p\text{min}} + S(x-n). \quad (14)$$

The gate-to-drain coupling capacitance C_M in this region and the following regions can be ignored since its effect is small; it mainly contributes to the output voltage at the beginning of the input transition. Ignoring C_M , and substituting Eqn. (14) into Eqn. (3) for PMOS current and Eqn. (4) into Eqn. (3) for NMOS current, the equations for region 2 can be simplified to:

$$\begin{aligned}
C_2 \frac{du_{x2}}{dx} &= D_2 (x-n)^{\alpha_n} + E_2 (x-n)^{\alpha_n-1} + F_2 (x-n)^{\alpha_n-2} \\
+ G_2 (x-n) + H_2,
\end{aligned} \quad (15)$$

where

$$\begin{aligned}
C_2 &= C_L V_{DD} / t_r, \quad D_2 = -K_{sn}, \\
E_2 &= -\alpha_n C_L K_{sn} R / t_r, \quad F_2 = -(\alpha_n - 1) \alpha_n C_L K_{sn} L / t_r^2, \\
G_2 &= S, \quad H_2 = I_{p\text{min}} + C_L R S / t_r.
\end{aligned}$$

Solving Eqn. (15), with the boundary condition that $u_{x2} \Big|_{x=n} = u_{1n}$, we obtain:

$$\begin{aligned}
u_{x2} &= \frac{I_{p\text{min}} t_r + C_L R S}{C_L V_{DD}} (x-n) + \frac{t_r S}{2 C_L V_{DD}} (x-n)^2 \\
&- \frac{K_{sn} R}{V_{DD}} (x-n)^{\alpha_n} - \frac{\alpha_n K_{sn} L}{V_{DD} t_r} (x-n)^{\alpha_n-1} \\
&- \frac{K_{sn} t_r}{(\alpha_n + 1) C_L V_{DD}} (x-n)^{\alpha_n+1} + u_{1n}.
\end{aligned} \quad (16)$$

The slope S of PMOS current can be obtained by equating the linear approximated PMOS current with the current from α -power law at $x_m = (1-p+n)/2$, which is the mid-point of region 2:

$$I_{p\text{min}} + S(x_m - n) = K_{lp} (1-p-x_m)^{\alpha_p/2} (1-u_{x2} \Big|_{x=x_m}). \quad (17)$$

Region 3: When $x_{\text{satp}} \leq x < \min(x_{\text{satn}}, 1-p)$, both NMOS and PMOS are in saturation. By solving Eqn. (3) in this region and matching the boundary conditions with region 2, we can obtain the solution for u_{x3} . We equate u_{x3} with NMOS saturation voltage u_{d0n} to determine if NMOS is still in saturation when PMOS is cutoff at $x=1-p$. The inverter will operate in region 4 if NMOS is still saturated. Otherwise, the inverter will operate in region 5B.

Region 4: When $1-p < x < 1$, PMOS is cutoff, while NMOS is in saturation. Similar to what we have done in the previous regions, we obtain the expression for u_{x4} . By equating u_{x4} with NMOS saturation voltage u_{d0n} , we obtain x_{satn} , when NMOS turns from saturated to linear operation. By comparing x_{satn} with 1, the next operation region of the inverter can be determined. If x_{satn} is greater than 1, then from $x=1$ to x_{satn} , the inverter will operate in region 5A. Otherwise, at time x_{satn} , the inverter will go from region 4 to region 5B.

Region 5A: When $1 < x < x_{\text{satn}}$, NMOS is still in saturation, and PMOS is cutoff. The input voltage has reached V_{DD} and will remain at V_{DD} from now on.

Region 5B: When $x_{\text{satn}} < x < 1$, NMOS is in linear region. PMOS current can be ignored in this region. It is either in cutoff or very weakly conducting.

Region 6: When $x > \max(x_{\text{satn}}, 1)$, NMOS is in linear region, PMOS cutoff. The input voltage remains at V_{DD} .

For region 5A, 5B, and 6, we can derive the normalized output voltage u_{x5A}, u_{x5B}, u_{x6} exactly the same way as we have done for the previous regions.

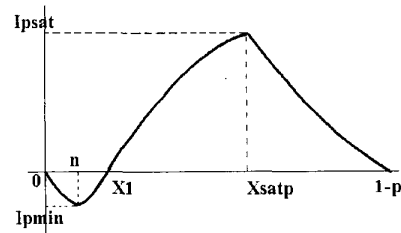


Figure 3. PMOS current

By now, we have derived the expressions of normalized output voltage for all operation regions. For rising transition, short-circuit energy consumed is the product of V_{DD} and t_r and the integration of the positive PMOS current during the transition. The waveform of PMOS current during the transition is shown in Figure 3. At x_1 , PMOS current is zero and the output voltage is V_{DD} . It can be computed by solving Eqn. (18) in region 2.

$$u_{x_2}(x_1) = 1. \quad (18)$$

From this point onward, a positive current is drawn from V_{DD} to ground through PMOS. At x_{sap} , PMOS changes from linear operation into saturated operation until it is finally cutoff at $1-p$, and x_{sap} can be computed by solving

$$u_{x_2}(x_{sap}) = 1 - u_{dop}. \quad (19)$$

The short-circuit energy is given by:

$$\begin{aligned} E_{gsc} &= V_{DD} t_r \left(\int_{x_1}^{x_{sap}} I_{p\text{lin}} dx + \int_{x_{sap}}^{1-p} I_{p\text{sat}} dx \right) \\ &= V_{DD} t_r \left(\int_{x_1}^{x_{sap}} [I_{p\text{min}} + S(x-n)] dx + \int_{x_{sap}}^{1-p} K_{sp} (1-p-x)^{\alpha_p} dx \right) \\ &= V_{DD} t_r \left[I_{p\text{min}} (x_{sap} - x_1) + \frac{1}{2} V_{DD} t_r S ((x_{sap} - n)^2 - (x_1 - n)^2) \right. \\ &\quad \left. + \frac{K_{sp} V_{DD} t_r}{\alpha_p + 1} (1 - p - x_{sap})^{\alpha_p + 1} \right]. \end{aligned} \quad (20)$$

It is obvious that to calculate short-circuit energy, only the first two regions need to be analyzed.

In Eqn. (20), V_{DD} , t_r , n , p , α_p , and K_{sp} are all constant values for a certain circuit and a rising input waveform, which can be known easily. The other parameters in Eqn. (20) are $I_{p\text{min}}$, S , x_1 , and x_{sap} . As described before, we can get them from Eqns. (13), (17), (18), and (19), respectively. So we can draw the conclusion that Eqn. (20) is a closed form expression for the short-circuit energy E_{gsc} during a rising transition.

III. COMPARISON WITH SPICE

A comparison between the results from our model and SPICE is shown in this section. We use a 0.18um Cu technology for comparison. Short-circuit energy levels computed from our model and from SPICE for different rising transition times for a minimum sized inverter with $C_L = 50\text{fF}$, $R = 100\Omega$, $L = 20\text{pH}$ are shown in Table 2. We used the method introduced in [3] to calculate short-circuit energy levels from SPICE. From Table 2, we observe that the errors introduced by our model compared to SPICE are within 10%.

t_r (ns)	Egsc_SPICE (J)	Egsc_model (J)	Error (%)
0.5	2.92638×10^{-15}	2.90023×10^{-15}	-8.936
1	8.58888×10^{-15}	8.98954×10^{-15}	4.665
2	2.38155×10^{-14}	2.54341×10^{-14}	6.800
4	6.09044×10^{-14}	6.47796×10^{-14}	6.363

$$C_L = 50\text{fF}, R = 100\Omega, L = 20\text{pH}$$

Table 2. 0.18um Cu short-circuit power comparison

The output voltage comparison between our model and SPICE for different rising times is shown in Figure 4. The x-axis is time

normalized by t_r , and the y-axis is output voltage normalized by V_{DD} . The errors of our model compared with SPICE are within 15%.

OUTPUT VOLTAGE COMPARISON WITH SPICE FOR DIFFERENT RISING TRANSITION TIMES

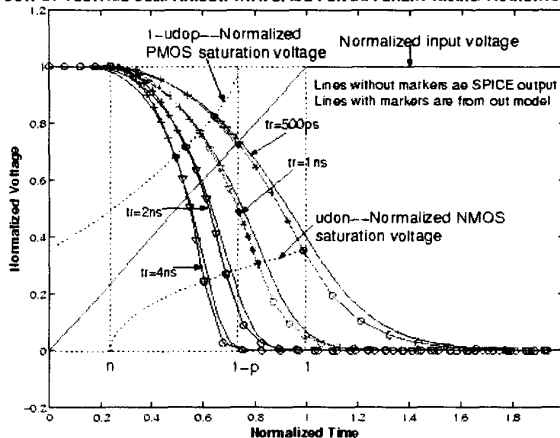


Figure 4. Output Voltage for different rise time

IV. CONCLUSIONS

In this paper, a closed form expression for short-circuit power computation is introduced for an inverter driving an RLC load. We compared our model with SPICE for 0.18um Cu technology. The short-circuit energy errors introduced by our model are within 10% of SPICE.

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