



When the tail of this ‘ $V_{dd}/2$ ’ voltage wave reaches the far end (also the driver input) (time =  $0.5T$ ), a ‘ $V_{dd}/2$ ’ wave train is regenerated at the output of the driver due to impedance match and begins to propagate to the far end. Meanwhile, the wave front of the ‘ $V_{dd}/2$ ’ voltage wave train reaches the near end, disappears, and returns its energy back to the power supply, again due to impedance match. The superposition of these two results in a ‘ $V_{dd}$ ’ voltage value at the near end from time =  $0.5T$  to time =  $1T$ . Essentially, a ‘ $V_{dd}/2$ ’ voltage wave train with wavelength equal to the length of the transmission line always exists and sustains itself, and hence the oscillation sustains itself. The oscillation signal has 50% duty because the forward and backward wave train travel time are the same.

Every time when the driver drives the near end to ‘ $V_{dd}/2$ ’, the actual voltage value at the near end is always ‘ $V_{dd}$ ’. Consequently, the voltage drop across the driver output resistance is always ‘0’; thus the driver never drains current from the power supply. In other words, the power consumption is asymptotically zero in the ideal case.

In practice, the oscillator operates similarly to the ideal case. The differences between the ideal case and the real case are:

- 1) The transmission line is not lossless because of the line resistance and the dielectric loss. The loss is compensated by the inverter, and the power consumption is therefore no longer zero and depends on the loss of the transmission line.
- 2) The driver has input and output capacitances, making the waveform at the far end not strictly square. However, the waveform at the near end is still close to square due to the non-linearity of the inverter.
- 3) The inverter driver delay is non-zero. This is because the inverter output begins to switch only when the inverter input reaches the transistor threshold voltages. However, as the rising/falling time is very short, this delay is very low as compared with the delay on the transmission line. Hence, the driver delay can be ignored in most cases.

## B. Theory

1) *Oscillation Frequency:* In ideal case, the oscillation frequency can be expressed as:

$$f = \frac{1}{2T_f} = \frac{1}{2l\sqrt{LC}}, \quad (1)$$

where  $T_f = l\sqrt{LC}$  is the time-of-flight of the transmission line.

For realistic cases with inverter gate capacitance  $C_L$  and output capacitance  $C_o$  considered as part of the transmission line, the oscillation frequency can be estimated as

$$f = \frac{1}{2T_f} = \frac{1}{2l\sqrt{L(C_o + C_L)/l}}. \quad (2)$$

If the transmission line is not very lossy (true for the top interconnect of modern VLSI), it is well known that

$$1/\sqrt{LC} = v, \quad (3)$$

where  $v$  is the speed of light in the media that is mostly determined by the dielectric constant of the media and the

profile of the conductors and the dielectrics. Obviously, as the speed of light in the material is fixed, the oscillation frequency is insensitive to any variations and also very stable.

2) *Power Consumption:* Power consumption is composed of two parts: the short-circuit power consumed by the driver  $P_{short}$  and the power loss on the lossy transmission line  $P_{loss}$ .

If we assume that the short-circuit current waveform is triangle with peak current  $I_{peak}$  for minimum size driver, and the signal rising time is  $t_{rise} = t_{fall}$ , then the short-circuit power consumption is:

$$P_{short} = nI_{peak}V_{dd}t_{rise}/T, \quad (4)$$

where  $n$  is the size of the driver with respect to the minimum size inverter,  $T$  is the clock period, and  $I_{peak}$  depends on the device model of the minimum inverters.

With phasor analysis, the power consumption on the transmission line due to loss is

$$P_{loss} = Re(V_{dd}^2/(R_s + Z_{in}/(1 + Z_{in}j\omega C_1)))/4, \quad (5)$$

where  $Z_{in}$  is the transmission line near end input impedance ( $Z_{in} = Z_c \frac{1 + Z_c j\omega C_L \tanh(\gamma l)}{\tanh(\gamma l) + Z_c j\omega C_L}$ , it is infinity in ideal case).

The total power consumption is the sum of the short circuit power and the transmission line loss, and

$$P_{total} = P_{short} + P_{loss}. \quad (6)$$

## III. CLOSELY-COUPLED R<sup>2</sup>TWO OSCILLATORS FOR GLOBAL CLOCK DISTRIBUTION

Based on the basic R<sup>2</sup>TWO oscillator, there are two derivative oscillators as the basic building blocks for clock distribution: Y-mode and  $\Delta$ -mode R<sup>2</sup>TWO oscillators.

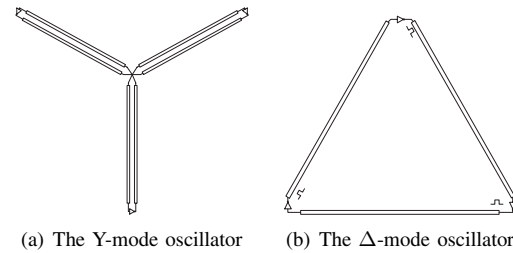


Fig. 2. The Y-mode and the  $\Delta$ -mode R<sup>2</sup>TWO oscillators

### A. Y-mode R<sup>2</sup>TWO oscillator

We connect three identical oscillators at the middle points of the transmission lines to form a ‘Y-shape’, and the resultant circuit is called a ‘Y-mode’ oscillator (Fig. 2(a)). ‘Y-mode’ oscillator can be used to reduce clock jitter because of the well-known phase averaging effect. If noise changes the phase of any one of the oscillators, the phase averaging at the tapping point can use the other two to correct the phase error. Intuitively, if one oscillator has a phase error of  $\delta t$  due to noise, the other two can help to reduce this to  $\delta t/3$ . However, the skew due to mismatch cannot be reduced as there is no skew reduction mechanism and the skew may be a little higher than that of the  $\Delta$ -mode oscillator that we discuss in the next.

### B. $\Delta$ -mode $R^2TWO$ oscillator – a new oscillator

We can also cascade three identical oscillators into a  $\Delta$ -shape as shown in Fig. 2(b) to form a new oscillator. Obviously, this  $\Delta$ -structure circuit can work as a traditional ring oscillator with frequency  $f = 1/(6T_d)$ , if we assume the total delay on each transmission line and driver segment is  $T_d$ .

However, when the drivers are reset simultaneously, each segment works exactly the same as each other, and also the same as the basic  $R^2TWO$  oscillator. Three voltage waves are trapped in the transmission lines, and get reflected and regenerated at the same time. The oscillation frequency of this  $\Delta$ -mode oscillator is therefore  $f = 1/(2T_d)$ , which is three times of that of the traditional ring oscillator.

One important property of the  $\Delta$ -mode oscillator is that it can provide near zero skew at the driver output, even if small variations exist between the three segments. Due to space limitations, the detail will be discussed in a future paper.

### C. Twin-mode oscillator circuit implementation

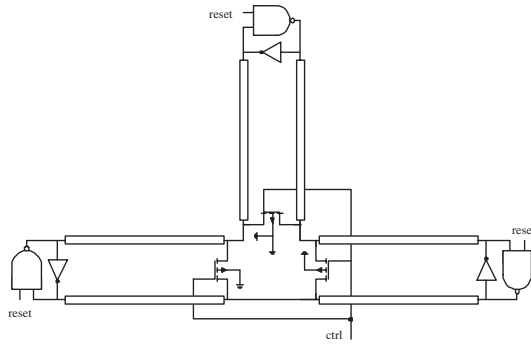


Fig. 3. The twin-mode oscillator circuit that can work in both 'Y'-mode and ' $\Delta$ '-mode.

Fig. 3 shows the implemented circuit that can work as either a Y-mode or a  $\Delta$ -mode oscillator. Each stage driver is implemented by a large size NAND gate and a smaller size auxiliary inverter. The auxiliary inverter is used to provide a positive feedback path to improve the gain of the inverter at the oscillation frequency, and may not be necessary for future nano-meter CMOS technologies where the device cut-off frequency is far higher than the expected oscillation frequency.

NMOS transistors are used as switches to switch between the Y-mode and  $\Delta$ -mode (when 'ctrl' is '1', it works in Y-mode; when 'ctrl' is '0', it works in  $\Delta$ -mode). 'Reset' signal is used for the  $\Delta$ -mode oscillator to start the oscillation with a '0'-to-'1' transition. After the oscillation has started, the NAND gates operate essentially as inverters.

### D. Clock grid for global clock distribution

As the phase averaging effects can significantly reduce the clock jitter and skew [3], closely coupled  $R^2TWO$  network can be used to further reduce jitter and skew for the proposed oscillator to be used on global clock distribution. Fig. 4 shows an example clock grid that is based on both the Y-mode and the  $\Delta$ -mode oscillators. Depending on the timing requirements,

Y-mode or  $\Delta$ -mode oscillators can be chosen. With process scaling, the transmission line lengths of the clock grid need only to be shortened to meet the requirement of the clock frequency and clock sink density increasing. This global clock distribution thus scales very well and is suitable for future generation VLSI clocking.

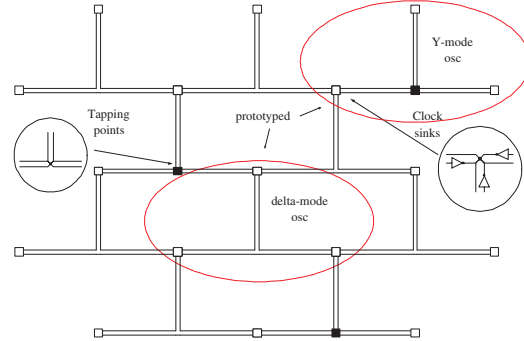


Fig. 4. The global clock grid composed of the proposed  $R^2TWO$  oscillators.

## IV. SIMULATION RESULTS

The basic  $R^2TWO$  oscillator is simulated by HSPICE with TSMC 0.18um CMOS model. The interconnect parameters used in the simulation are:  $R = 50 \Omega/\text{cm}$ ,  $L = 4 \text{ nH}/\text{cm}$  and  $C = 1.2 \text{ pF}/\text{cm}$ , which correspond to wire width  $W=10\mu\text{m}$  and length  $l = 5 \text{ mm}$  at 10GHz. The size of the transistors used in the inverter driver are  $W_n = 35\mu\text{m}$ , and  $W_p = 95\mu\text{m}$  with minimum gate length.

Fig. 5 shows the simulated waveforms at the input 'a' and output 'b' of the driver. The simulated oscillation frequency is 9.5GHz. The waveform at the output of the driver is near square. However, the waveform at the input of the driver is a saw-tooth wave. This is the result of the non-negligible gate capacitance of the driver. The power consumption is 5.48mW, which is less than 30% of the  $CV^2f$  power (18.47mW).

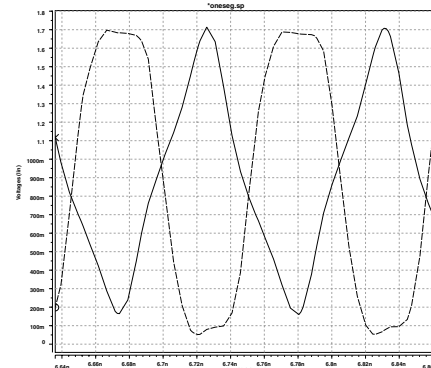


Fig. 5. The simulated waveforms of the basic  $R^2TWO$  oscillator. Dashed curve: inverter output 'b'; solid curve: inverter input 'a'.

Table I and II show how frequency is marginally affected by variations in the power supply and threshold voltages. When the power supply has more than  $\pm 10\%$  variation, the clock period changes by only 0.5ps. The two extreme cases of the threshold variations give a period difference of only 1.8ps.

## V. EXPERIMENTS

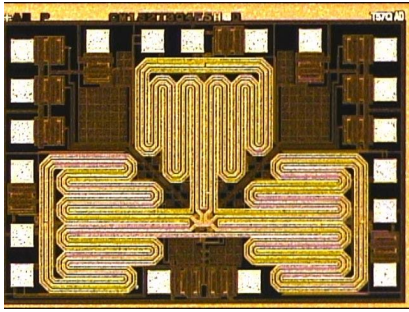


Fig. 6. The die photo of the test chip. The three serpentine top-metal coplanar transmission lines are visible.

The twin-mode R<sup>2</sup>TWO oscillator described in section III was prototyped in TSMC 0.18 $\mu$ m 1.8-V RF/Mixed-signal process with 6 Al metal layers and the thick top layer option. The chip area is around 1.9x1.3mm<sup>2</sup> (Fig. 6). The three oscillators were placed symmetrically to reduce mismatch. The on-chip co-planar transmission lines with length 5.6mm and width 10 $\mu$ m were routed in serpentine shapes to save chip area.

With 1.8V power supply, the  $\Delta$ -mode oscillator oscillates at a measured frequency of 6.550GHz, and the Y-mode oscillator oscillates at a measured frequency of 6.543GHz. (In contrast, if the  $\Delta$ -structure circuit operates like a traditional ring oscillator, the frequency is measured to be 2.0GHz.) The oscillation frequency of the Y-mode oscillator is slightly lower because the switch transistors at the tapping point provide more capacitance to the transmission line in that mode.

The phase noise figures are shown in Fig. 7. The phase noises are -116.2dBc/Hz and -116.5dBc/Hz at 1MHz offset frequency for the Y-mode and  $\Delta$ -mode oscillators, respectively. The corresponding RMS jitter is 0.66ps for the Y-mode oscillator, and 0.84ps for the  $\Delta$ -mode oscillator.

The skew is measured by off-chip skew test circuits. The maximum skew between the driver outputs is lower than 1.3ps for the Y-mode oscillator and lower than 0.9ps for the  $\Delta$ -mode oscillator.

We also vary the power supply voltage by  $\pm 10\%$  of  $V_{dd}$ , the measured period difference is only 0.43ps, which is less than 0.3% of the clock period at 1.8V supply voltage.

The total power consumption (excluding drivers) is measured to be 28.08mW for both Y-mode and  $\Delta$ -mode oscillators, and 35.28mW for the  $\Delta$ -structure traditional ring oscillator. If we use the same comparison criteria as in [1] and [8], the power saving is more than 75% at 6.5GHz.

## VI. CONCLUSION

A novel traveling-wave oscillator using wave reflection and regeneration on transmission lines and a novel clock distribution network based on it to generate multi-GHz square wave

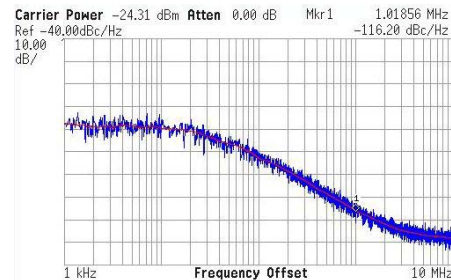
TABLE I  
THE EFFECT OF POWER SUPPLY VARIATION ON CYCLE PERIOD

V <sub>dd</sub> (V)	1.62	1.74	1.80	1.86	1.98
T(ps)	105.1	105.2	105.2	105.3	105.6

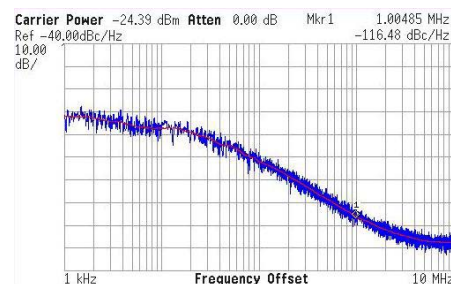
TABLE II

THE EFFECT OF DEVICE THRESHOLD VARIATION ON CYCLE PERIOD. (T: TYPICAL, S: SLOW, AND F: FAST)

Corner model (Nmos Pmos)	TT	SS	FF	SF	FS
$\Delta V_{thn}$ (V)	0	0.1	-0.1	0.1	-0.1
$\Delta V_{thp}$ (V)	0	-0.067	0.067	-0.067	0.067
T(ps)	105.2	106.1	104.3	105.6	105.1



(a) The Y-mode R<sup>2</sup>TWO oscillator phase noise



(b) The  $\Delta$ -mode R<sup>2</sup>TWO oscillator phase noise

Fig. 7. The phase noise of Y-mode and  $\Delta$ -mode oscillators.

clocks are proposed. Simulation and experiment results verify that the oscillator/clock distribution network can generate and distribute 6.5GHz full-swing clock signals with low skew and jitter, and are not power-hungry.

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