Computational Electromagnetics for High-Frequency IC Design

Dan Jiao*, Changhong Dai, Shiuh-Wuu Lee, Tawfik R Arabi, and Greg Taylor
Logic Technology Development, Intel Corporation

Abstract

In this talk, we will first discuss the need for computational electromagnetics (CEM) in high-frequency IC design. We will then review the recent advancements in CEM, present chip design challenges to CEM analysis, and analyze the shortcomings of current CEM methodology. We will then proceed to emphasize the importance of chip-design-driven CEM development, and finally present some promising full-wave electromagnetic-based solutions that can achieve full-chip analysis and design.

The Need for CEM in High-Frequency IC Design

Circuit theory, as the low frequency part of Maxwell's theory, has guided VLSI design and analysis for more than three decades. This theory is adequate as long as the physical dimension of the interconnects remains tiny compared to the wavelength of interest. Evolving into the third decade, the clock frequency of microprocessors enters the gigahertz regime and heads towards 20GHz. Since it is necessary to analyze the chip response to harmonics 5 times the clock frequency and full wave effects are starting to be observable at about 1/100th of a wavelength, it is expected that interconnects longer than 30μm would have to be analyzed with certain full wave effects incorporated. As a result, computational electromagnetics, the science of solving Maxwell's equations at both low and high frequencies, has begun to draw attention from on-chip design community.

In open literature, various researchers have discussed the necessity of digital and mixed-signal IC design with full-wave electromagnetic accuracy [1-3]. In real high frequency design, on-chip designers face the questions of whether circuit-based design methodology is still valid on critical circuits such as wires in the global clock distribution network and power delivery system that requires die-package-board co-design. To answer these questions quantitatively instead of conceptually, it is essential to investigate the validity of circuit-based IC design methodology in realistic on-chip design environment.

Interconnect design is one of the biggest design challenges in high frequency mixed-signal IC design. Anticipated by International Technology Roadmap for Semiconductors (ITRS), over one billion transistors will be integrated on a single die by the end of this decade [4]. All these transistors are connected via interconnect lines. Interconnect performance is thus expected to dominate the performance of the entire chip. To meet the design target, interconnect deign methodology has experienced a series of transitions over the past three decades. At the beginning, interconnects were modeled as lumped resistance and capacitance (RC). As on-chip designers move to faster clock frequencies enabled by process technology scaling with reduced feature sizes, lumped RC models were replaced by distributed RC models and capacitive coupling. Since early 1990's, on-chip inductive effects became more important with the increased peak current ramp rates (di/dt) and transistor speed [5-6]; and consequently inductive noise analysis has been included in the design flow of on-chip design. Anticipating the design needs as the clock

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frequency increases towards 10+ GHz within a few technology generations, in 2001, Intel began to validate RLC-based parasitic extraction at tens of GHz. Good agreement has been observed between measured data and static RLC-based modeling on purely 2D test chip structures [7]. However, significant mismatch between measurements and RLC models was observed at multi-GHz frequencies on 3D interconnect structures [7]. In contrast, full-wave electromagnetic-based modeling accurately captures the measured behavior over the entire frequency band [8]. The mismatch between RLC models and measurements was shown to be attributed to the decoupled E and H in static modeling, and the capacitance and inductance are extracted in an independent fashion. This finding demonstrates the importance of full-wave electromagnetic-based modeling and design methodology. On the other hand, consider IC analysis from simulation point of view. The interconnect interactions are both local and global. Partitioning on-chip interconnects into blocks and analyzing each of them separately can lead to erroneous design due to the nature of electromagnetic coupling. Accurate full-chip simulation, as a result, is demanded by post-layout performance verification. However, the distributed RC- or RLC-based modeling approach generates tremendous number of circuit elements, which is far beyond the limit that SPICE-like circuit simulators can handle. To circumvent such a bottleneck, a design methodology that is fundamentally different from the conventional circuit-based approaches can help. Field-based approach is thus a good alternative as it is able to bypass many bottleneck problems inherent in circuit-based design methodology. These findings and observations lead on-chip designers to the verge of the transition from circuit-based design methodology to field-based design methodology that has full-wave electromagnetic accuracy. However, is electromagnetic analysis ready to take center stage in high frequency mixed-signal IC design?

CEM State-of-the-arts

To answer this question, it is necessary to review recent advances in computational electromagnetics. Computational electromagnetics has evolved into its prime to date. Numerous fast algorithms have been developed. They can be categorized into two classes: integral equation (IE) based solvers and partial differential equation (PDE) based solvers. In IE-based solvers, fast multiple method (FMM) [9], fast QR-based methods [10-11], and FFT-based methods [12-14] have been developed that dramatically reduce the memory requirement of dense matrix solvers from $O(N^2)$ to $O(N \log N)$, and the CPU time from $O(N^3)$ (direct solver) or $O(N_i N^2)$ (iterative solver) to $O(N \log N)$ for electrodynamic problems. In PDE-based solvers, people have developed not only fast sparse matrix solvers of $O(N)$ computational complexity [15], but also numerical techniques that can completely eliminate matrix solutions [16-17]. In addition, a number of acceleration techniques applicable to both IE and PDE solvers have been developed to speed up the electromagnetic simulation [9]. These techniques include hybridization schemes that combine the advantages of different numerical schemes; higher-order schemes that solve the fields in higher-order accuracy and efficiency; reduced-order model that represents the problem into reduced order without losing accuracy and so on. Time-domain schemes have also drawn extensive attention in recent years due to their capability in broadband modeling within one run and in non-linear device modeling. Progresses have been made in finite difference time domain method (FDTD) [17], time-domain finite-element method (TDFEM) [16], and time-domain integral equation schemes (TDIE) [18-19]. The advancement of CEM has been widely applied to microwave engineering, antenna analysis, scattering analysis, wireless communications, and optoelectronics and so on. It has also been extensively applied to electrical modeling and design of packaging- and board-level signal integrity problems in recent years.

Moving towards on-chip design at next step appears straightforward. However, is the existing CEM technology amenable for on-chip design?

Modeling challenges of mixed-signal IC

On-chip structures present many modeling challenges that are less pronounced in board- and package-level problems. These challenges can be summarized as the following: (1) Conductor loss. In contrast to traditional full-wave applications in which currents only flow on the surface of the conductors, on-chip structures are transparent to fields and currents. Fields interior and exterior to conducting surfaces are equally important. In contrast to package and board interconnects that are planar-like (thickness is much smaller than the width); on-chip interconnect lines have the similar dimension in width and thickness. In addition, on-chip interconnects are generally surrounded by many adjacent lines. How the current is distributed inside each conductor is not only a function of frequency but also a function of the coupling with surrounding conductors. This hinders the use of any approximate conductor loss model. (2) Large number of non-uniform dielectric stacks and strong non-uniformity. The interconnect systems of processing technologies of 0.13μm and beyond involve 8+ metal layers. Between the metal layers are a number of interlayer dielectric media. In addition, the metal and dielectric stacks are heterogeneous. (3) The presence of silicon substrate. On-chip interconnects usually are not backed by ground planes as their packaging or board counterparts. Instead, they are exposed to silicon substrate. The substrate loss can be either low or high depending on the substrate resistivity. Using conductor loss model to handle substrate could yield significant errors. Treating substrate as lossy dielectric would lead to large number of unknowns. (4) Large number of conductors. On-chip global interconnect structures such as on-chip power grid can involve millions of interconnect lines. (5) Large aspect ratio. The length of on-chip interconnect lines can be orders of magnitude larger than the cross-sectional dimension. (6) Broadband. On-chip applications cover broadband frequencies from DC to tens of gigahertz. (7) 3D complexity. On-chip structures are complicated 3D in nature. It is difficult to take advantage of symmetry or periodicity to simplify the problems in electrical modeling.

Limitation of current CEM methodology for IC design

The aforementioned challenges result in large computational complexity of on-chip problems and prevent the direct use of existing full-wave numerical techniques in chip-level IC analysis. For instance, FDTD usually requires a time step that is constrained by the smallest spatial step to ensure stability. This hinders its application to realistic on-chip problems since on-chip interconnects feature geometries ranging from less than 0.1 micron to thousands of microns. Although this problem can be eliminated by developing an unconditionally stable FDTD scheme, the computation remains expensive due to the large number of unknowns resulting from the 3D geometries and the fine discretization required to capture skin effects of hundreds and thousands of interconnects. Full-wave based integral-equation methods generally break down at the low frequencies that lie within the frequency band of on-chip interconnects [9]. Although advanced numerical techniques [9] can be utilized to eliminate this issue, other shortcomings limit its practical usefulness. The method itself either can only be applied to the cases wherein the Green's function is available (surface integral equation based methods), or has to be formulated into a computationally intensive volume integral equation so that the complicated inhomogeneity can be modeled. Heterogeneous dielectrics present in on-chip structures destroy the regularity of stratified media. Large number of non-uniform dielectric layers

drastically increases the computational complexity of layered Green's function-based surface integral equation approach. As far as the finite element method is concerned, although it can efficiently comprehend arbitrary inhomogeneity and irregular geometry, the large scales of on-chip problems resulted from large aspect ratio and fine discretization to capture the skin effects constitute a big computational challenge.

On-chip design driven CEM development

Having realized the importance of full-wave electromagnetic-based chip design in high frequency products and the limitation of current CEM methodology in impacting the chip-level IC design, it is imperative to develop innovative CEM methods for IC design so that the continuous IC growth can stay uninterrupted. A review of recent work in on-chip full-wave modeling revealed that people in both VLSI CAD and CEM areas are making progress towards this direction [3, 14, 21-22]. We have pioneered the research and development work in full-wave electromagnetic-based IC design in Intel [7, 8, 20]. In the remaining part of this talk we will discuss some solutions.

References:

[1] R. Achar and M. S. Nskhla, Proc. IEEE, vol. 89, May 2001, pp. 693-728.
[2] A. Deutsh et al, Proc. IEEE, vol. 89, April. 2001, pp. 529-555.
[3] A. C. Cangellaris, "Towards on-chip Analysis with Electromagnetic Accuracy," EPEP'2003.
[4] International Technology Roadmap for Semiconductors, 2001 Edition.
[5] Arabi, T.R. and Suarez-Gartner, R, IEEE Microwave Symposium Digest, vol. 2, 1993, pp. 987 -990.
[6] Arabi, T.R., Murphy, A.T., and Sarkar, T.K., IEEE Transactions on MTT, vol. 40, 1992, pp. 1857 -1869.
[7] M. J. Kobrinsky, S. Chakravarty, D. Jiao, M. Harmes, S. List, and M. Mazumder, "Experimental validation of crosstalk simulations for on-chip interconnects at high frequencies using S-parameters", EPEP 2003, pp. 329-332.
[8] D. Jiao, M. Mazumder, S. Chakravarty, C. Dai, M. Kobrinsky, M. Harmes, and S. List, "A novel technique for full-wave modeling of large-scale three-dimensional high-speed on/off-chip interconnect structures," International Conference on Simulation of Semiconductor Proc. and Dev., 2003, pp. 39-42.
[9] "Fast and Efficient Algorithms in Computational Electromagnetics", edited by W. C. Chew, J. M. Jin, E. Michielssen, and J. M. Song. Norwood, MA: Artech House, 2001.
[10] S. Kapur and D. E. Long, "IES3: Efficient Electrostatic and Electromegnetic Solution", IEEE Computer Sci. and Engg. 5(4), pp. 60-67, Oct-Dec 1998.
[11] D. Gope and V. Jandhyala, "PILOT: A fast algorithm for enhanced 3D parasitic extraction efficiency", EPEP 2003, pp. 337-340.
[12] E. Bleszynski, M. Bleszynski, and T. Jaroszewicz, "AIM, Adaptive integral method for solving large-scale electromagnetic scattering and radiation problems," Radio Science, vol. 31, pp. 1225-1251, 1996.
[13] F. Ling, C. F. Wang, and J. M. Jin, "An efficient algorithm for analyzing large-scale microstrip structures using adaptive integral method combined with discrete complex image method," IEEE Trans. On MTT, vol. 48, pp. 832-839, May 2000.
[14] Z. H. Zhu, B. Song, and J. K. White, "Algorithm in fastimp: A fast and wideband impedance extraction program for complicated 3D geometries," 40th ACM/IEEE Design Automation Conference, 2003.
[15] J. M. Jin, "The Finite Element Method in Electromagnetics", John Wiley & Sons, 2nd edition, 2002.
[16] D. Jiao and J. M. Jin, "Finite element analysis in time domain", in The Finite Element Method in Electromagnetics. New York: John Wiley & Sons, 2nd edition, 2002.
[17] A. Taflove and S. C. Hagness, Computational Electrodynamics: The Finite-Difference Time-Domain Method, 2nd ed. Norwood, MA: Artech House, 2000.
[18] A.A. Ergin, B. Shanker, and E. Michielssen, "Fast evaluation of transient wave fields using diagonal translation operators," J. Comp. Phys., vol. 146, pp. 157--180, 1998.
[19] B. Shanker, A.A. Ergin, K. Aygn, and E. Michielssen, IEEE APS, vol. 2, 1999, pp. 1342--1346.
[20] D. Jiao, S. Chakravarty, M. Mazumder, C. Dai, M. J. Kobrinsky, "Efficient full-wave S-parameter-based noise analysis for high frequency design of 3D on-chip buses", 2003 Intel DTTC Conference.
[21] L. Daiel, A. Sangiovanni-Vincentelli, and J. White, "Using conduction modes basis functions for efficient electromagnetic analysis of on-chip and off-chip interconnects", Proc. 2001 DAC., pp. 563-566.
[22]A. Rong, A. C. Cangellaris, and Limin Dong, "Comprehensive broadband electromagnetic Modeling of on-chip interconnects with a surface discretization-based generalized PEEC model," EPEP2003, pp. 367-370.