From $O(k^2N)$ to $O(N)$: A Fast and High-Capacity Eigenvalue Solver for Full-Wave Extraction of Very Large Scale On-Chip Interconnects

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***Abstract*—The wave-propagation problem in an on-chip interconnect network can be modeled as a generalized eigenvalue problem. For solving such a generalized eigenvalue problem, the computational complexity of Arnoldi iteration is at best $O(k^2N)$, where k is the number of dominant eigenvalues and N is the matrix size. In this paper, we reduce the computational complexity of the Arnoldi iteration for interconnect extraction from $O(k^2N)$ to $O(N)$, thus paving the way for full-wave extraction of very large scale on-chip interconnects, of which a typical value of k is on the order of hundreds of thousands. Numerical and experimental results have demonstrated the accuracy and efficiency of the proposed fast eigenvalue solver.**

***Index Terms*—Arnoldi iteration, frequency domain, full-wave analysis, generalized eigenvalue problem, on-chip interconnects.**

I. Introduction

As THE clock frequency of microprocessors entered the gigahertz regime, full-wave models have become increasingly important since it is necessary to analyze the chip response to harmonics that are up to five times the clock frequency. In particular, full-wave-based analysis can be used to characterize global electromagnetic coupling through the common substrate and power delivery network. However, there are many modeling challenges associated with on-chip interconnect structures [1]. These challenges include large problem size, large number of nonuniform dielectric stacks with strong nonuniformity, large number of nonideal conductors, presence of silicon substrate, highly skewed aspect ratios, etc. In recent years, solutions of formulations based on both partial differential equations and integral equations have been developed to address these challenges [1]–[13]. However, driven by the continued increase of the complexity of integrated-circuit problems, there still exists a continued demand of reducing the computational complexity of full-wave modeling methods.

The wave-propagation problem in an on-chip interconnect network can be modeled as a generalized eigenvalue problem $\mathbf{A}x = \lambda\mathbf{B}x$[4], [14]–[16]. Let the matrix size of $\mathbf{A}$ and $\mathbf{B}$ be N. In general, the number of propagation modes that can be supported by an on-chip interconnect structure is much less than N[4], [14]–[16]. Therefore, what is really required is the computation of selected eigenpairs of the generalized eigenvalue system. Among all the existing eigenvalue solvers, the Arnoldi iteration [17] is particularly suited for this computing task. The Arnoldi process generates an orthonormal basis of the Krylov subspace of a significantly reduced size on which the original eigensystem is projected. The overall computational complexity of an Arnoldi process is $O(kN^2+k^2N)$, where k is the number of significant eigenvalues. The $O(kN^2)$ cost is due to the computation of $\mathbf{B^{-1}A}x$ at each Arnoldi iteration. The $O(k^2N)$ cost is attributed to the orthonormalization of the k Arnoldi vectors that span the Krylov subspace. In each Arnoldi iteration, the current Arnoldi vector is made orthonormal to all previous Arnoldi vectors.

In [15], [16], a direct matrix solver of linear time complexity was developed. The solver allowed for an efficient computation of $\mathbf{B^{-1}A}x$ in $O(N)$ complexity, leading to an efficient solution to the generalized eigenvalue problem. The $O(N)$ complexity for computing $\mathbf{B^{-1}A}x$ in $O(N)$ was achieved by eigenvalue clustering, fast system reduction with negligible computational cost, and fast linear time solution of the reduced system. As a result, the overall computational complexity of solving a generalized eigenvalue problem was reduced to $O(k^2N)$, which is linear when k is a constant that is not related to N. However, for an on-chip interconnect, which involves a large number of conducting wires, even $O(k^2N)$ complexity is too high, since k is related to N and is on the order of hundreds and thousands. However, due to the fact that the orthogonalization of Krylov subspace vectors is unavoidable in an Arnoldi process, the time complexity of Arnoldi iteration is at best $O(k^2N)$. Even if one intends to reduce the complexity further, there is no easy way forward.

The main contribution of this paper is the reduction of the computational complexity of Arnoldi iteration method for solving a generalized eigenvalue problem from $O(k^2N)$ to $O(N)$, thus paving the way for the full-wave extraction of very large scale integrated circuits. The basic idea of this paper has been outlined in [18]. In this paper, a detailed derivation of the proposed method is given. A theoretical proof is developed, and an extensive number of numerical results are given to provide a rigorous validation of the proposed method.

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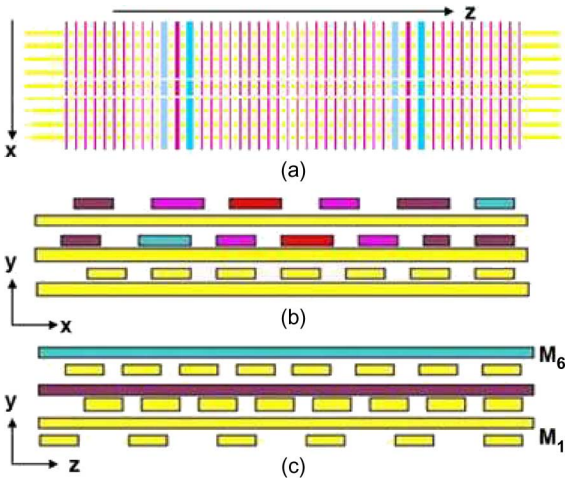


Fig. 1. Illustration of a typical on-chip interconnect structure [4].

II. Overview of the Eigenvalue-Based Analysis of On-Chip Interconnects

A typical on-chip interconnect structure is shown in Fig. 1. The generalized eigenvalue problem resulting from a finite-element-based analysis of such a structure can be written as [4], [14]

$$\begin{bmatrix} \mathbf{A}_{tt} & 0 \\ 0 & 0 \end{bmatrix} \begin{Bmatrix} e_t \\ e_z \end{Bmatrix} = \gamma^2 \begin{bmatrix} \mathbf{B}_{tt} & \mathbf{B}_{tz} \\ \mathbf{B}_{zt} & \mathbf{B}_{zz} \end{bmatrix} \begin{Bmatrix} e_t \\ e_z \end{Bmatrix} \tag{1}$$

in which the eigenvalues correspond to the propagation constants γ, and the eigenvectors characterize the transverse electric field e_t and longitudinal electric field e_z. Matrices $\mathbf{A}$ and $\mathbf{B}$ are complex valued due to the penetration of fields into on-chip conductors. The entries of $\mathbf{A}$ and $\mathbf{B}$ are given by

$$\begin{aligned}
\mathbf{A}_{tt,ij} &= \iint_{\Omega} \left[\frac{1}{\mu_r} \{\nabla_t \times \mathbf{N}_i\} \cdot \{\nabla_t \times \mathbf{N}_i\} \right. \\
&\qquad \left. - {k_0}^2 \overline{\varepsilon}_r \mathbf{N}_i \cdot \mathbf{N}_j \right] \mathrm{d}\Omega \\
\mathbf{B}_{tt,ij} &= \iint_{\Omega} \frac{1}{\mu_r} \mathbf{N}_i \cdot \mathbf{N}_j \mathrm{d}\Omega \\
\mathbf{B}_{tz,ij} &= \iint_{\Omega} \frac{1}{\mu_r} \mathbf{N}_i \cdot \nabla_t \xi_j \mathrm{d}\Omega \\
\mathbf{B}_{zt,ij} &= \iint_{\Omega} \left[\frac{1}{\mu_r} \nabla_t \xi_j \cdot \mathbf{N}_j \right] \mathrm{d}\Omega \\
\mathbf{B}_{zz,ij} &= \iint_{\Omega} \left[\frac{1}{\mu_r} \{\nabla_t \xi_i\} \cdot \{\nabla_t \xi_j\} - {k_0}^2 \overline{\varepsilon}_r \xi_i \xi_j \right] \mathrm{d}\Omega
\end{aligned} \tag{2}$$

where $\overline{\varepsilon}_r$ denotes the complex permittivity that accounts for conductivity σ, $\mathbf{N}$ represents the edge basis function used to expand the transverse field [19], ξ is the node basis function used to expand the longitudinal field [19], and Ω is the computational domain.

We can compactly write (1) as

$$\mathbf{A}x = \lambda \mathbf{B}x \tag{3}$$

where $\mathbf{A}$ and $\mathbf{B}$ are sparse and of size $O(N)$. The task here is to find k-selected eigenpairs of the large sparse matrix system shown in (3), where k is the number of significant modes. The Arnoldi iteration [17] is particularly suited for this computing task. Consider a standard eigenvalue problem $\mathbf{G}x = \lambda x$, a k-step Arnoldi process generates an orthonormal basis $\{\nu_j\}_{j=1}^{k}$ of the Krylov subspace $\kappa_k(\nu_1, \mathbf{G})$ spanned by $\nu_1, \mathbf{G}\nu_1, \ldots, \mathbf{G}^{k-1}\nu_1$, where ν_1 is an initial unit norm vector. The orthogonal projection of $\mathbf{G}$ onto $\kappa_k(\nu_1, \mathbf{G})$ is represented by a $k \times k$ upper Hessenberg matrix $\mathbf{H}_k$, the Ritz pairs of which can be used to approximate the eigenpairs of $\mathbf{G}$.

The algorithm of a k-step Arnoldi process is shown as follows:

Algorithm: A k-step Arnoldi process

$$\begin{aligned}
&1.\ \nu_1 = \nu_1 / \|\nu_1\| \\
&2.\ \text{for } j = 1, 2, \ldots, k \quad \text{do} \\
&\quad 2.1.\ w = \mathbf{G}\nu_j \\
&\quad 2.2.\ \text{for } i = 1, 2, \ldots, j \quad \text{do} \\
&\qquad h_{ij} = \nu_i^* w \\
&\qquad w = w - h_{ij}\nu_i \\
&\quad 2.3.\ h_{j+1,i} = \|w\| \\
&\qquad \nu_{j+1} = w / h_{j+1,j}
\end{aligned} \tag{4}$$

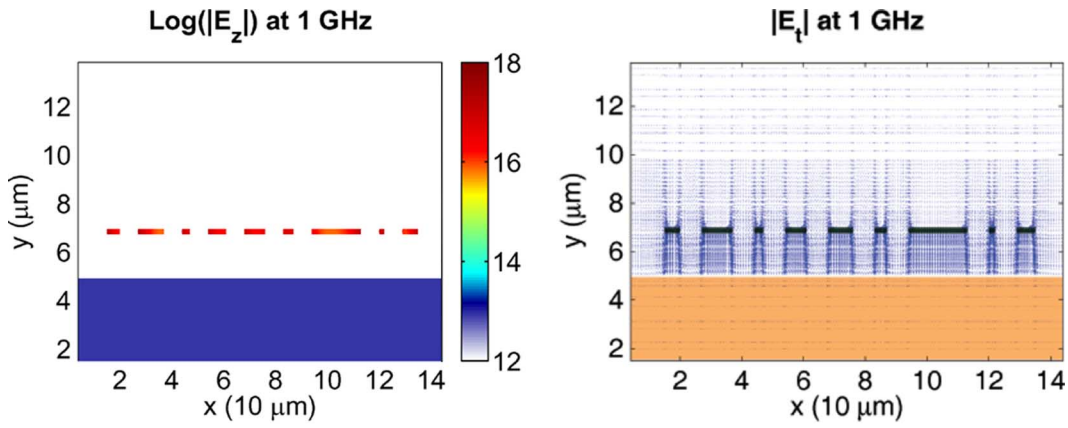
The complexity of this algorithm is $O(k^2 N)$ if $\mathbf{G}$ is sparse. However, in our problem, $\mathbf{G}$ is dense because it is equal to $\mathbf{B^{-1}A}$, and $\mathbf{B^{-1}}$ is dense, as can be seen from (3). Therefore the complexity of a straightforward implementation of the Arnoldi process is at least $O(k^2 N + kN^2)$, where the $O(kN^2)$ complexity accounts for the k dense matrix–vector multiplication operations in step 2.1 shown in (4), and the $O(k^2 N)$ complexity accounts for the cost of orthogonalization in step 2.2. The cost of step 2.1 was reduced to $O(N)$ by a recent development in [15], [16]. As a result, the complexity of the Arnoldi process is dominated by that of step 2.2. When k is large, the computation complexity of $O(k^2 N)$ could become prohibitively large. In the next section, we show a method that can remove this computational bottleneck.

III. Eigenvalue Solution of $O(N)$ Complexity

In this section, we first construct an alternative eigenvalue solution that is equivalent to the original one in terms of interconnect extraction; we then prove that the solution of the proposed alternative eigenvalue problem is local, from which we show that the dependence of an eigenvalue solution on the number of eigenvalues can be eliminated, and hence, an $O(N)$ complexity can be achieved.

A. Alternative Eigenvalue Solution

An examination of the field solution to the eigenvalue problem (1) reveals that the field distribution is global, i.e., fields spread all over the computational domain. As an example, in Fig. 2, we show the longitudinal and transverse electric field solution of (1) in a typical on-chip interconnect at 1 GHz. The interconnect involves seven layers, the dielectric constants of which are, respectively, 4, 2.9, 2.9, 2.9, 2.9, 2.9, and 4.



(a) (b)

Fig. 2. Solution of (1) in a typical on-chip interconnect. (a) Longitudinal field distribution. (b) Transverse field distribution.

These layers are, respectively, 0.137, 0.256, 0.256, 0.32, 0.384, 0.576, and 0.972 μm thick. There are nine parallel copper wires located in the third layer. The structure is backed by a silicon substrate, the conductivity of which is 10^4 S/m. The cross-sectional view of the structure is shown in Fig. 2. We show in Fig. 2(a) the magnitude of longitudinal electric field $\mathbf{E}_z$ at each discretized point in the cross section, from which the longitudinal current can be obtained by $\mathbf{J}_z = \sigma \mathbf{E}_z$. Clearly, the current is distributed all over the wires and the substrate. Fig. 2(b) shows the transverse electric field distribution, which again reveals that the field solution of (1) is global.

Since the solution of (1) is found to be global, there is no apparent way to truncate the computational domain, i.e., reduce the problem size. However, we can remodel the problem such that the field solution becomes local. The details are given as follows.

An on-chip interconnect structure of multiple conductors can be thought of as a p-port network. Its property can be characterized by network parameters such as impedance ($\mathbf{Z}$)-, admittance ($\mathbf{Y}$)-, and scattering ($\mathbf{S}$)-parameters. Take the $\mathbf{S}$-parameter extraction as an example. We first find from (1) all possible modes, i.e. field solutions, that can be supported by an interconnect. We then extract the $\mathbf{S}$-parameters of the interconnect from all these possible field solutions. The procedure can be summarized as follows:

S-Extraction Procedure

1. Solve $\mathbf{A}x = \lambda \mathbf{B}x$

   where $x = (e_t, e_z)^{\mathrm{T}}$, $\lambda = \gamma_m^2$

2. Perform Superposition

$$\mathbf{E} = \sum_{m=1}^{n} \left[\alpha_m \mathbf{e}_m(x,y)\mathrm{e}^{-\gamma_m z} + \beta_m \mathbf{e}_m(x,y)\mathrm{e}^{\gamma_m z}\right]$$

   where $\mathbf{e}_m = E_t \hat{t} + E_z \hat{z}$, $E_t = j e_t/\gamma$, $E_z = j e_z$

3. Extract $\mathbf{S}_{ij} = (V_i - Z_{\mathrm{ref}} I_i)/(V_j + Z_{\mathrm{ref}} I_j)$

   subject to $V_i + Z_{\mathrm{ref}} I_i = 0$, for $i \neq j$, $i = 1, 2, \ldots, p$

In the procedure shown above, $\hat{t}$ denotes a unit vector along the tangential direction, $\hat{z}$ denotes a unit vector along the longitudinal direction, and Z_{ref} denotes the reference impedance. An industry standard Z_{ref} is 50 Ω. Similarly, $\mathbf{Y}$-parameters of the interconnect can be extracted from the following procedure:

Y-Extraction Procedure

1. Solve $\mathbf{A}x = \lambda \mathbf{B}x$

2. Perform Superposition

$$\mathbf{E} = \sum_{m=1}^{n} \left[\alpha_m \mathbf{e}_m(x,y)\mathrm{e}^{-\gamma_m z} + \beta_m \mathbf{e}_m(x,y)\mathrm{e}^{\gamma_m z}\right]$$

3. Extract $\mathbf{Y}_{ij} = I_i/V_j$

   subject to $V_i = 0$, for $i \neq j$, $i = 1, 2, \ldots, p$

In the original eigenvalue solution defined by (1), all interconnects have the implicit boundary condition that they are matched to characteristic impedance of each mode. This is because the wave propagation along the longitudinal direction is analytically incorporated in the derivation of (1) via $\mathrm{e}^{-\gamma z}$ dependence. In other words, an exact absorbing boundary condition is imposed along the wave-propagation direction, and hence, in this direction, wave propagation has no reflections. This is equivalent to loading the interconnect structure by a matched impedance for each mode. Therefore, the circuit extraction procedure based on the original eigenvalue solution can be explicitly written as follows:

Original Extraction Procedure

1. Solve $\mathbf{A}x = \lambda \mathbf{B}x$

   subject to $V_i + Z_c I_i = 0$

2. Perform Superposition

$$\mathbf{E} = \sum_{m=1}^{n} \left[\alpha_m \mathbf{e}_m(x,y)\mathrm{e}^{-\gamma_m z} + \beta_m \mathbf{e}_m(x,y)\mathrm{e}^{\gamma_m z}\right]$$

3. Extract Circuit Parameters

where Z_c is the characteristic impedance. Comparing the above procedure to the $\mathbf{S}$-Extraction Procedure, it is clear that the original eigenvalue-solution-based circuit extraction resembles an $\mathbf{S}$-parameter-based extraction of the p-port network with reference impedance Z_{ref} chosen as Z_c. Since the solution is found to be global, it suggests that the $\mathbf{S}$-matrix of the interconnect network is dense.

It has been observed that admittance matrix $\mathbf{Y}$ arising from the modeling of on-chip interconnects is usually sparse [20]. It has also been observed that a full-wave integral-equation-based method casts a problem into a system of linear equations of the form $\mathbf{Z}I = V$, where $\mathbf{Z}$ is dense, whereas a partial-differential-equation-based method is able to model the same problem by $\mathbf{Y}V = I$, where $\mathbf{Y}$ is sparse. These observations suggest that a $\mathbf{Y}$-parameter-based extraction procedure can potentially render the solution local. Therefore, we constructed the following alternative procedure for interconnect extraction:

Alternative Extraction Procedure

1. Solve $\mathbf{A}x = \lambda \mathbf{B}x$

   subject to $V_i = 0$, for $i \neq j, i = 1, 2, \ldots, p$

2. Perform Superposition

$$\mathbf{E} = \sum_{m=1}^{n} \left[\alpha_m \mathbf{e}_m(x,y)\mathrm{e}^{-\gamma_m z} + \beta_m \mathbf{e}_m(x,y)\mathrm{e}^{\gamma_m z}\right]$$

3. Extract Circuit Parameters

A comparison of the above procedure to the $\mathbf{Y}$-Extraction Procedure clearly shows that the two procedures are equivalent, since they differ only in the ways the port boundary conditions are incorporated. In the Alternative Extraction Procedure, the port boundary conditions are incorporated at the stage of eigenvalue solution, whereas in the $\mathbf{Y}$-Extraction Procedure, the port boundary conditions are incorporated at the stage of circuit extraction. Since the incorporation of boundary conditions at an earlier stage or at a later stage should not affect the solution, the Alternative Extraction Procedure is equivalent to the Original Extraction Procedure, from the perspective that the two procedures generate the same network parameters.

As a result, instead of solving (1), the solution of which is found to be global, we transform (1) to an alternative eigenvalue solution as shown as follows:

Alternative Eigenvalue Solution

$$\begin{aligned} &\text{Solve } \mathbf{A}x = \lambda \mathbf{B}x \\ &\text{subject to } V_i = 0, \qquad \text{for } i \neq j, i = 1, 2, \ldots, p \end{aligned} \tag{5}$$

In this solution, we ground all the ports except for one port (or a few selected ports) whose modes are to be extracted, i.e., we let each port float in turn while grounding the rest of the ports. This leads to p eigenvalue problems. We then find the solution of each eigenvalue problem. The total $\mathbf{E}$ field can then be obtained as a linear combination of all these possible solutions, from which the network parameters, such as $\mathbf{S}$-parameters, can be extracted. The grounding of each port is achieved by explicitly setting the tangential electric field of corresponding edges to zero. By doing so, we enforce the port boundary condition in (5) without altering the original physical structure.

The solution of the alternative eigenvalue solution (5) is found to be local. In Fig. 3, we show the solution of (5) in the same interconnect structure shown in Fig. 2. We let the sixth conductor float and ground other conductors. We then observe the field solution extracted from (5) at 1 GHz. As shown in Fig. 3(a) and (b), both longitudinal and transverse electric fields exhibit a fast decay. In Fig. 3(c) and (d), we show the longitudinal and transverse electric field distributions at 20 GHz. Once again, a fast decay is observed.

In addition to the numerical proof shown in Fig. 3, we also theoretically proved that the solution of (5) is local, the detail of which is given in the following section.

B. Proof on the Locality of the Alternative Eigenvalue Solution

From the second row of (1), it can be seen clearly that the following equation satisfies:

$$\mathbf{B}_{zt}e_t + \mathbf{B}_{zz}e_z = 0. \tag{6}$$

In deriving (1), the following transformation was used [4], [14]

$$e_t = -j\gamma E_t \quad e_z = -jE_z. \tag{7}$$

Substituting (7) into (6), we obtain

$$E_z = -\mathbf{B}_{zz}^{-1}\mathbf{B}_{zt}(\gamma E_t). \tag{8}$$

From E_t, one can obtain the voltage at one end of the wire (a port) by performing a line integral from the terminal to the ground

$$V = \int E_t \mathrm{d}l. \tag{9}$$

Due to the fact that all field components have $\mathrm{e}^{-\gamma z}$ dependence in a structure seed [4], [14], we have

$$\gamma E_t = \frac{\partial E_t}{\partial z}. \tag{10}$$

Therefore, from γE_t, one can obtain the voltage difference between the two ends of the wire across a unit length

$$V_1 - V_2 = \int \gamma E_t \mathrm{d}l. \tag{11}$$

In addition, from E_z, one can obtain the current flowing into the wire by performing an area integral of the current density over the wire cross section

$$I = \int\int (j\omega\varepsilon + \sigma)E_z \mathrm{d}S \tag{12}$$

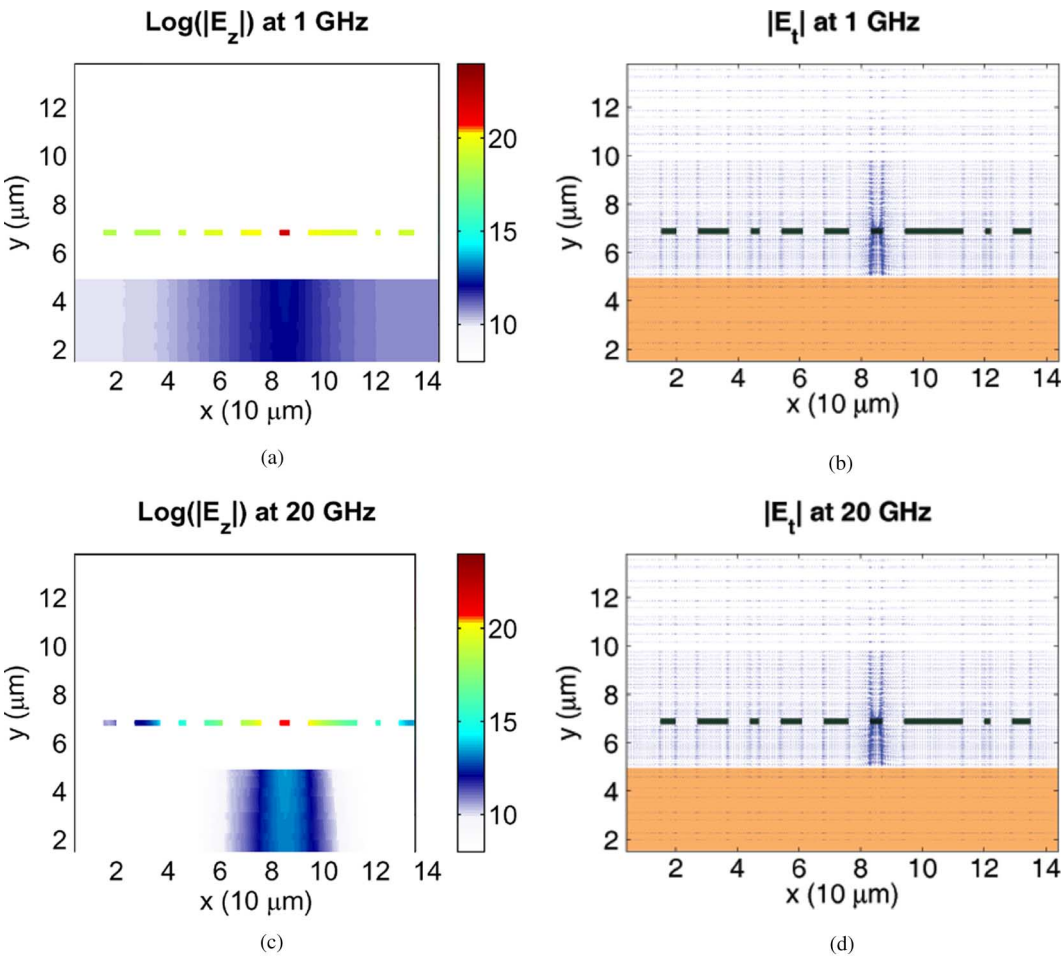


Fig. 3. Solution of (5) in a typical on-chip interconnect. (a) Longitudinal field distribution at 1 GHz. (b) Transverse field distribution at 1 GHz. (c) Longitudinal field distribution at 20 GHz. (d) Transverse field distribution at 20 GHz.

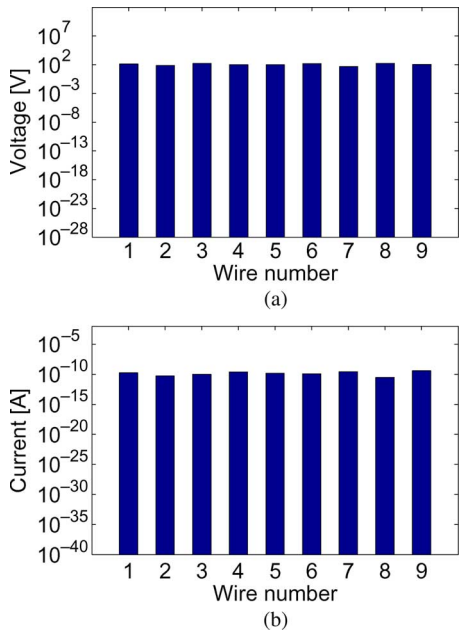


Fig. 4. Voltage and current distributions in log scale simulated from the original eigenvalue solution (1) at 1 GHz.

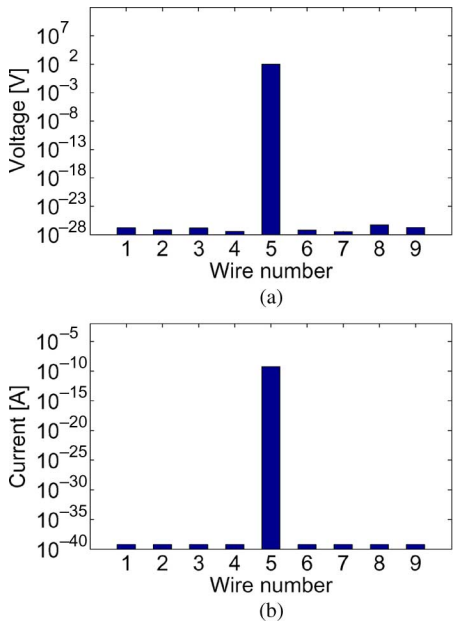


Fig. 5. Voltage and current distributions in log scale simulated from the alternative eigenvalue solution (5) with all the conductors grounded except for the fifth conductor at 1 GHz.

in which both displacement and conduction currents are included. From the aforementioned analysis, E_t in (8) relates to voltage, γE_t relates to the voltage difference across a unit length, and E_z relates to current. Therefore, although (8) is a

field-based equation, it has an analogous circuit meaning [21]. The circuit interpretation of (8) is

$$I = \frac{V_1 - V_2}{Z_{\text{in}}} \tag{13}$$

which reveals the impedance experienced by a current I given a potential difference $V_1 - V_2$ at the two ends of a wire of a unit length.

When computing the alternative eigenvalue solution (5), we ground all the ports (wires) except for one port. Once the port (wire) is grounded, the tangential electric field E_t on each edge along the grounding path is set to zero. Hence, γE_t is zero. As a result, the voltage difference across the wire length is set to zero, as can be seen from (11). Hence, from (13), the current flowing into the grounded port is zero. As a result, in the alternative eigenvalue solution (5), the currents flowing into all the ports are zero except for the port that is not grounded. Therefore, except for the wire that is excited, all the other wires do not carry current. In other words, no current is coupled to other wires no matter how close they are to the wire that is excited, because the voltage difference across the length of these wires is enforced to be zero. As a result, in the alternative eigenvalue solution (5), the current loop is forced to be formed between the active conductor and the physical ground only instead of adjacent wires and hence localized. Therefore, the locality of the alternative eigenvalue solution is proved.

As a validation of the above proof, we did the following experiment. We considered the same test-chip interconnect shown in Figs. 2 and 3. In Figs. 4 and 5, we show the voltage and current distributions simulated from the original eigenvalue solution (1) and the alternative eigenvalue solution (5) respectively. The label of x-axis in Figs. 4 and 5 denotes the index of the conductors, and the label of y-axis represents the magnitude of voltage or current. As shown inFig. 4, in the original eigenvalue solution, the voltage and current distributions over the conductors is global, i.e., no voltages and currents are significantly smaller than others. However, in Fig. 5, it is clearly shown that the current flowing into each conductor is zero except for the conductor that is not grounded. This behavior is in an excellent agreement with our theoretical proof. In addition, we compared the $\mathbf{S}$-parameters obtained from the alternative eigenvalue solution and those simulated from the original eigenvalue solution. Denoting the former by $\mathbf{S}$, and the latter by $\tilde{\mathbf{S}}$, and using Frobenius norm, the difference $||\mathbf{S}-\tilde{\mathbf{S}}||_F/||\mathbf{S}||_F$ was found to be 3.48%. Therefore, the proposed alternative eigenvalue solution localizes the field solution without sacrificing circuit-extraction accuracy.

Since the solution of the alternative eigenvalue problem is local, this property can be utilized to significantly reduce the computational complexity of an eigenvalue solution, which is described in the next section.

C. Windowing Technique

If the field solution becomes zero in the region that is away from the active conductor, there is no need to simulate fields in that region. Hence, for each eigenvalue problem defined by (5), we do not have to simulate the entire computational domain. We only have to simulate a small window in which fields are nonzero. We cannot do this in the framework of the original eigenvalue solution, since the fields are global in that scenario. By developing an alternative eigenvalue solution described in Section III-A, we essentially localize the solution of the system and hence are able to simulate a sequence of much smaller problems to obtain the solution of the original large problem without any reduction cost. One might argue that if the original solution is global, there is no way to localize it. Note that, here, we have already remodeled the problem such that the solution of our problem becomes local. A basic windowing procedure is given as follows:

Windowing Procedure

1) Adaptively determine the window size.
2) Compute the field solution inside the window based on (5).
3) Slide the window from left to right.
4) Repeat the computation until the whole structure is solved.
5) Perform superposition.
6) Extract circuit parameters.

The window size is adaptively decided by enlarging the window size progressively until the solution converges. The convergence criterion is $|\lambda_{\text{new}} - \lambda| \leq \delta$, where λ_{new} is the eigenvalue obtained from the enlarged window, and δ is a parameter determined by a required level of accuracy. As shown in Section III-B, in the proposed alternative eigenvalue solution, current loop is shrank to the loop formed between the active conductor and ground. If the ground is perfect, it is known that fields on the ground only concentrate in a small region having a size similar to the active conductor; if the ground is not perfect, it can be viewed as a resistance (R)–inductance (L) network, the area that the fields/currents can spread over is also limited so that the impedance experienced by the current can be minimized (note that larger area results in a larger ωL). Therefore, the window size is, in general, very small.

D. Complexity Analysis

Assume that L windows are used, and each window includes M number of unknowns. The proposed eigenvalue solver solves L eigenvalue problems, each having size M. In each eigenvalue problem, k is $O(1)$, since in each window, we only let one or a few conductors float while grounding all the other conductors. As a result, the computational complexity for simulating the eigenvalue problem in each window is $O(M)$. Since there are L windows in total, the total computational complexity of the proposed solver is $O(LM) \sim O(N)$, which does not depend on the total number of eigenvalues in the original system.

IV. Numerical and Experimental Validation

We simulated a number of on-chip interconnect structures to evaluate the performance of the proposed eigenvalue solver. The first example is the same structure examined in Section II, the cross section of which is shown in Figs. 2 and 3. The structure involved 9 wires and 18 ports in total. We simulated the structure using the original eigenvalue solution as well as the proposed

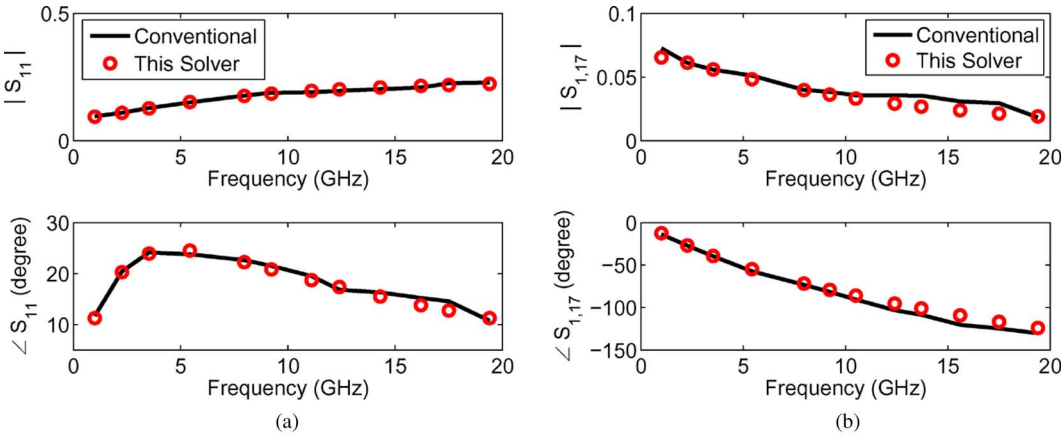


Fig. 6. Simulation of an 18-port on-chip interconnect. (a) S_{11}. (b) $S_{1,17}$.

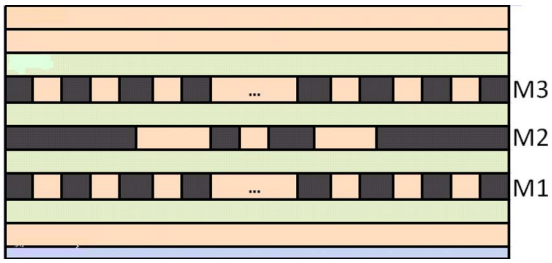


Fig. 7. Cross-sectional view of a test-chip interconnect structure.

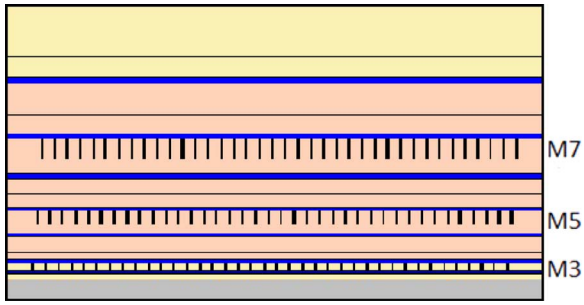


Fig. 9. Large-scale interconnect having 30–600 conductors.

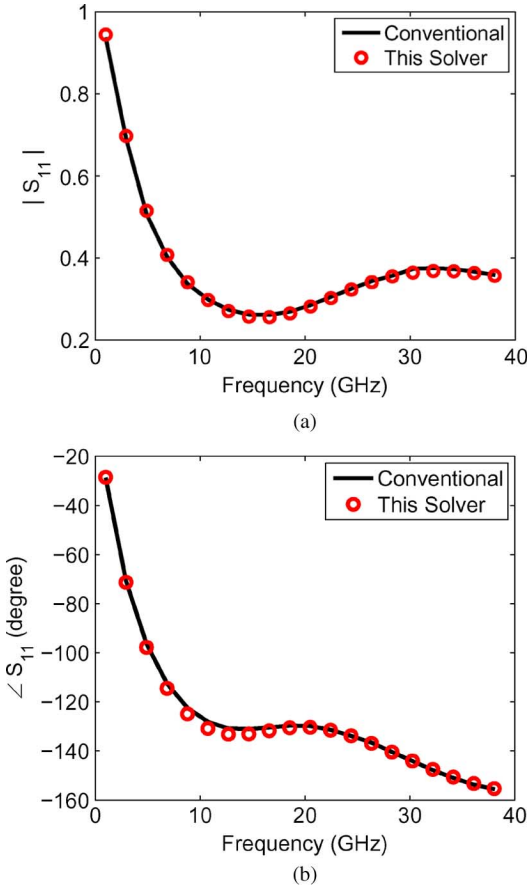


Fig. 8. Simulation of a test-chip interconnect. (a) $|S_{11}|$. (b) S_{11} phase (degree).

alternative one. In Fig. 6, we show simulated $\mathbf{S}_{11}$ and $\mathbf{S}_{1,17}$, where port 1 was located at the near end of the leftmost wire, and port 17 was located at the near end of the rightmost wire. An excellent agreement can be observed, which validates the proposed alternative eigenvalue solution.

The second example is a test-chip interconnect structure [8], the cross-sectional view of which is shown in Fig. 7. The structure was 2000 μm long, consisting of 11 inhomogeneous layers. It involved 12 parallel returns in M1 and M3 layers, respectively. These returns were 1.05 μm wide and 1 μm apart and overlapped with each other vertically. Two wires were placed in the center of M2. The far ends of the two center wires in M2 were left open. The $\mathbf{S}$-parameters at the near end of one M2 wire were extracted by the proposed fast eigenvalue solver. The physical ground was located at the bottom of the substrate. The window size was chosen between 14 and 16 μm. In total, six windows were used. As shown in Fig. 8, the simulated $\mathbf{S}$-parameters agree very well with those generated by the conventional solver reported in [4], [14], the result of which was shown to agree with the measured data.

The last example was used to test the performance of the proposed fast eigenvalue solver in solving large-scale on-chip interconnects. The structure involves seven dielectric stacks, the dielectric constants of which are, respectively, 4, 2.9, 2.9, 2.9, 2.9, 2.9, and 4. These layers are, respectively, 0.972, 0.576, 0.384, 0.32, 0.256, 0.256, and 0.137 μm thick. The third, fifth, and seventh dielectric stack is populated with 10–200 parallel conductors. The smallest problem hence involves 30 conductors, and the largest problem involves 600 conductors (see Fig. 9).

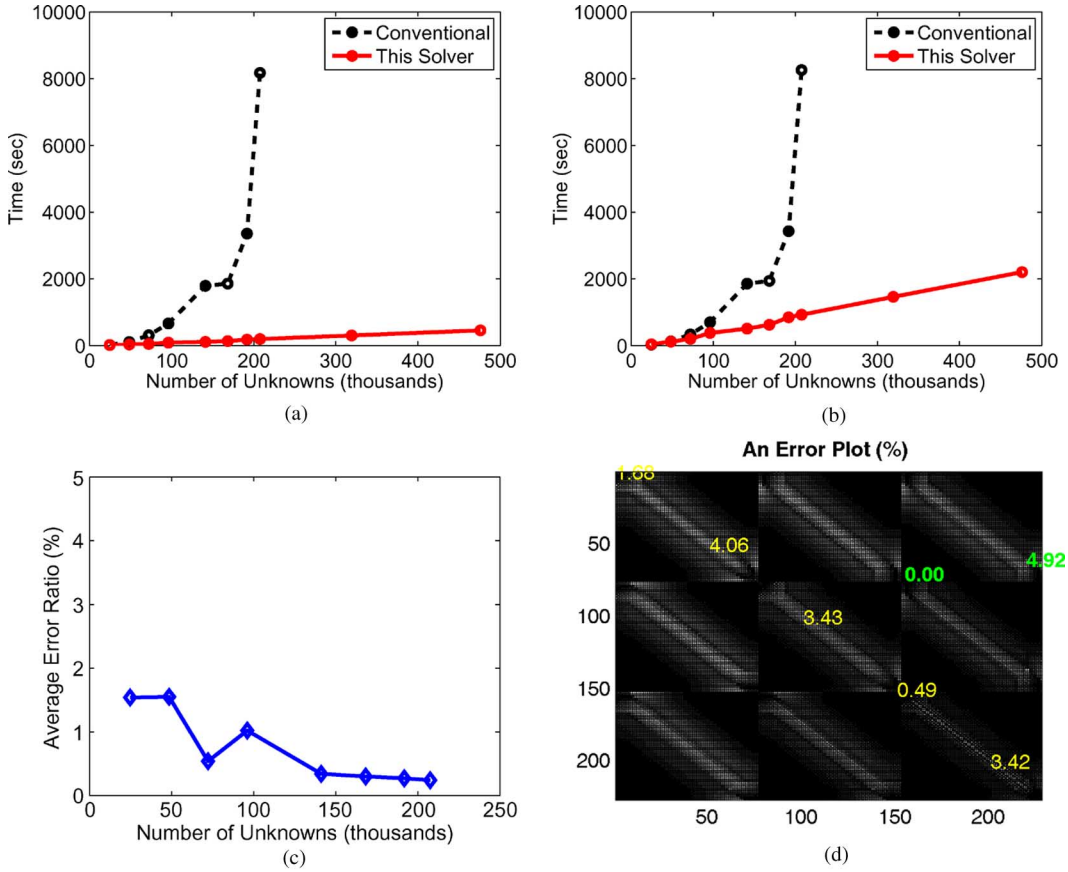


Fig. 10. Simulation of a large-scale on-chip interconnect involving 30–600 conductors. (a) Arnoldi time. (b) Total CPU time. (c) Average percentage error. (d) Error plot of $\mathbf{S}$-matrix for 114-conductor (228-port) case.

Each conductor is 0.5 μm wide and separated from each other by 2.5 μm in each metal layer. These conductors, i.e., interconnect wires, do not overlap with each other vertically. The distance from the leftmost (rightmost) conductor to the left (right) boundary is 10 μm. The computational domain was discretized into triangular elements, resulting in 24 651–476 091 unknowns. If we use the number of conductors to estimate the number of significant eigenvalues k, the range of k is from 30 to 600. We simulated the structure at 20-GHz frequency. The ground was located at the bottom. The left, right, and top boundary conditions were set to be open.

First, we used the 30-conductor case to examine the accuracy of the proposed solver with respect to window size. It was shown that when the window included 15, 21, and 27 conductors, the average error of the $\mathbf{S}$-matrix was 3.96%, 1.54%, and 0.75% respectively. The 21-conductor window was then decided as a window size across the simulations. In Fig. 10(a), we show the Arnoldi iteration time, which is the time of step 2 in (4), with respect to unknowns. Clearly, the performance of the proposed solver is linear, whereas the conventional solver developed in [16] scales as $O(k^2N)$. Since k increases with N in this case, the performance of the conventional solver is much worse than linear. In Fig. 10(b), we show the total CPU time with respect to the number of unknowns, which includes the factorization time needed for the computation of $\mathbf{B^{-1}A}$. Again, the proposed solver demonstrates a linear complexity that is independent of k. In Fig. 10(a) and (b), we include the CPU time spent on adaptively deciding the window size. In Fig. 10(c), we use the results obtained from the conventional solver as a reference and show the average error of the extracted $\mathbf{S}$-parameters with respect to the number of unknowns. The error is evaluated by using $|\mathbf{S}_{ij} - \tilde{\mathbf{S}}_{ij}|/\min\{(|\mathbf{S}_{ii}|, |\mathbf{S}_{jj}|)\}$, where $\mathbf{S}$ is generated by the conventional solver and $\tilde{\mathbf{S}}$ is generated by the proposed fast solver. Clearly, good accuracy can be observed in the entire range. In Fig. 10(d), we take the 114-conductor (228-port) case as an example and show the error of every $\mathbf{S}$-matrix element. The ports are ordered layer by layer from M3 to M7 and assigned to the near end and far end of each conductor. Excellent accuracy can be observed. In addition, we used $||\mathbf{S} - \tilde{\mathbf{S}}||_F/||\mathbf{S}||_F$ to assess the error, where subscript F denotes a Frobenius norm. The error was shown to be 4.83%. Therefore, the proposed solver reduces the computational complexity of a generalized eigenvalue problem without sacrificing accuracy. In Fig. 10(a) and (b), the results for the conventional solver were only generated up to 261 conductors, since it could not solve larger problems in reasonable run times.

For large problems, the conventional solver cannot solve them in feasible computational resources. To predict the error of the proposed fast solver in solving large-scale problems, we plotted the error as a function of window size for three different problem sizes: a 30-conductor interconnect, a 60-conductor one, and a 114-conductor one. The error is evaluated by using $|\mathbf{S}_{ij} - \tilde{\mathbf{S}}_{ij}|/\min\{(|\mathbf{S}_{ii}|, |\mathbf{S}_{jj}|)\}$ in Fig. 11(a). In Fig. 11(b), the error is evaluated by using $||\mathbf{S} - \tilde{\mathbf{S}}||_F/||\mathbf{S}||_F$. As shown

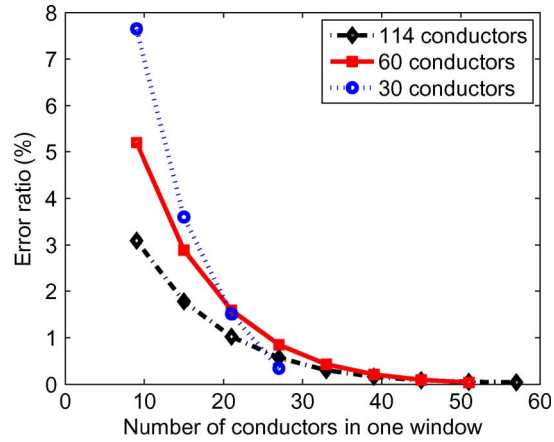


Fig. 11. S-parameter error as a function of window size. (a) Weighted error. (b) Frobenius-norm-based error.

clearly in Fig. 11, irrespective of the problem sizes, the result converges to the true solution once a certain window size is reached. In addition, the required window size to reach a good accuracy is small.

V. Summary

The computational complexity of a generalized eigenvalue problem generally depends on the number of eigenvalues k. A large-scale on-chip interconnect network involves a large number of conductors, and hence, a large number of eigenvalues. As a result, state-of-the-art eigenvalue solutions become computationally prohibitive when analyzing large-scale interconnect structures. In this paper, we transform the original eigenvalue solution to an alternative one. We show that the alternative eigenvalue solution is equivalent to the original one in terms of interconnect extraction. Most importantly, we prove that the alternative eigenvalue solution is local and hence can be utilized to significantly reduce the computational complexity of an eigenvalue analysis. As a result, we are able to decompose the original large-scale eigenvalue problem into L small eigenvalue problems, each having a constant number of dominant eigenvalues. Hence, we reduce the computational complexity of the generalized eigenvalue problem from $O(k^2N)$ to $O(N)$. Numerical experiments demonstrated superior performance of the proposed method for solving large-scale on-chip interconnects.

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