Characterization of Discrete Decoupling Capacitors for High-Speed Digital Systems

Joong-Ho Kim, Dan Jiao, Jiangqi He, Kaladhar Radhakrishnan, and Changhong Dai
Intel Corporation
5000 W. Chandler Blvd.
Chandler, AZ 85226
Tel: (480)554-3723
Fax: (480)552-1295
Email: joong-ho.kim@intel.com

Abstract

This paper describes frequency-dependent characterization of multi-terminal decoupling capacitors (2, 8, 14, and any arbitrary number of terminals) by using a full-wave tool developed at Intel. This tool can capture high frequency effects with fast CPU run time, which enables accurate modeling of the power delivery system. The full-wave S-parameters have been validated with the measurements and the modeled data obtained from a commercial tool (HFSS). Based on its fast and accurate solution, different design configurations of capacitors have been studied to identify the optimal configuration which will maximize the performance of the decoupling capacitor. To capture the frequency-dependent behavior of capacitor impedance, a higher order representation made up with 7 or 9 elements of RLGC was developed. This circuit representation was used to assess the accuracy of conventional series lumped RLC capacitor model. Finally, the responses were incorporated into a high performance microprocessor's power delivery network to investigate system performance.

Introduction

Complementary metal oxide semiconductor (CMOS) microprocessors and application specific integrated circuits (ASICs) in a modern digital system consist of a large number of internal circuits and external circuits (I/O drivers). While recent advances in CMOS technology have resulted in faster device switching speed, power supply noise induced by a large number of internal and external switching circuits has become a critical issue. Current levels continue to go up with every generation while the power supply voltage scales down as the features on the Silicon shrink. This causes the impedance target to scale down rapidly with every generation.

In the modern power delivery system, suppression of power supply noise is critical since it becomes increasingly difficult to keep the impedance of a power delivery system low especially when clock speed and power consumption increase continuously. Furthermore, to pass the FCC (Federal Communication Commission) or other regulating agency's emission standards, digital system designers have to design the power delivery system optimally to ensure minimal electromagnetic emission from the whole computer system [1]. In addition, to be competitive in the market, minimizing cost is always a high priority for designers. Therefore, an important issue in high-speed digital systems is the design of the power/ground planes and decoupling capacitors arising in power delivery networks.

One of the most effective ways to reduce the power supply noise is to use decoupling capacitors on the card, board, module, and/or chip. Decoupling capacitors are used to offset the parasitic inductance present in a power distribution network, thereby yielding a small impedance over as large a frequency range as possible [2]-[4]. Decoupling capacitors provide switching circuits with extra current required to charge the load capacitor in addition to the power supply. As a result, the power supply noise is reduced since the inductive effect in the loop current path is decreased by decoupling capacitors. Therefore, the selection of capacitor type, number and locations becomes critical for an optimal system design. For this reason, it is imperative to have fast and accurate prediction of decoupling capacitor's performance for such a system that demands the tight power supply noise margin.

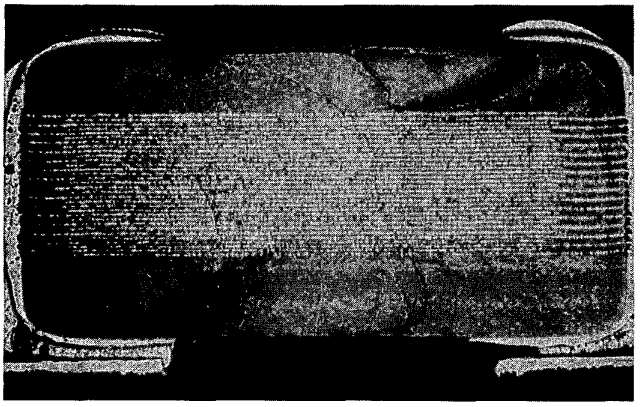
Tremendous amount of research work has been done on capacitor characterization [5]-[8]. Li et al characterized capacitors in high frequency ranges [5] and then studied on the validation of an integrated capacitor using capacitor-via-plane models and applied quasi-static type of solvers [6]. Smith et al worked on transmission line models for ceramic capacitors based on measurements and an ESR model for power delivery system [7], [8]. These researchers provided detailed information about capacitor characterization based on measurement data. However, these approaches are based on the existence of capacitor's data, and hence are not sufficient to design unknown capacitor configurations that match our requirements. Although certain extension could be implemented to roughly predict capacitor's performance based on the concepts of these methods, an accurate and fast approach that can model broadband frequency response of any kind of configuration is highly desired. Moreover, to accurately predict the electromagnetic emission at UHF range, frequency dependent responses of decoupling capacitors are needed. As a result, a full wave solver would be an ideal choice. Current existing commercial full wave solvers, however, have certain limitations when applied to tiny, but very complicated capacitor geometries. The reasons could be large mesh aspect ratio, large memory requirements, expensive CPU run time, and bad matrix condition that will lead to bad convergence.

In this paper, a full-wave solver developed at Intel [9] was employed to characterize high-density decoupling capacitors. Its accuracy and efficiency will be demonstrated as compared with measurements and numerical experiments. Furthermore, different design configurations of capacitors will be demonstrated with their frequency dependent responses. The responses will be incorporated into high performance microprocessor's power delivery network to illustrate system performance. Discussions will be then extended to whether full-wave frequency-dependent capacitor responses are

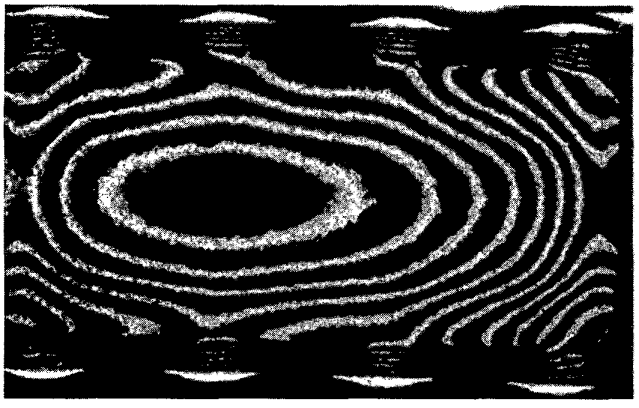
needed for a high current, and high frequency power delivery network compared to conventional single element series lumped RLC.

Full-wave Capacitor Characterization

It is well known that full-wave solvers used widely on microwave engineering and circuits are based on finite element methods (FEM), finite difference time domain (FDTD) methods or method of moments (MoM). Theoretically, these algorithms are able to provide accurate simulation results based on accurate input parameters and correct setup. However, applying full-wave commercial tools by directly using these algorithms may not achieve our goal due to the high computational complexity present in realistic engineering problems. For example, these 3D full-wave algorithms sometimes may not be able to model a typical capacitor shown in Figure 1 quickly and accurately. In addition to the reasons described in the introduction section, low accuracy in capturing the loss that directly impacts the equivalent series resistance (ESR) is another main factor. Thus, a special tool was developed internally for this particular application [9]. Especially, the tool was developed for fast and accurate design and analysis of generic multi-terminal discrete decoupling capacitors, which can simulate arbitrary number of terminals in arbitrary configurations including a large number of power/ground planes.



(a)



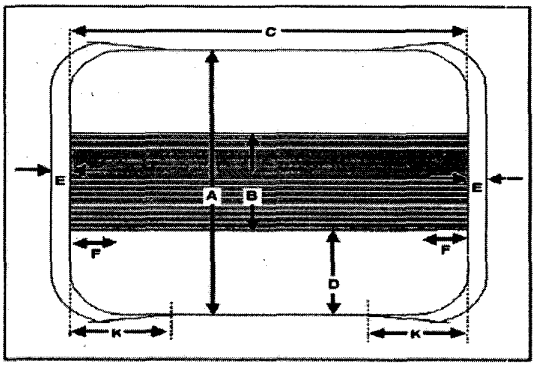
(b)

Figure 1. Cross section of decoupling capacitors: (a) 0612 two-terminal capacitor's side view and (b) 0805 eight-terminal capacitor's top view with polished top surfaces.

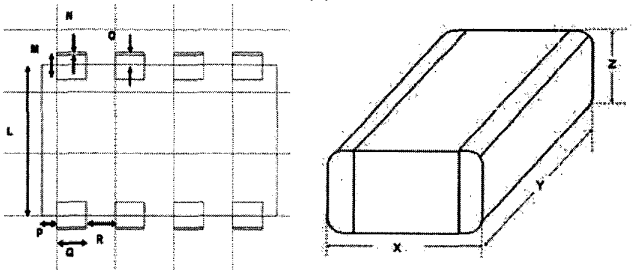
As mentioned earlier, the accuracy of simulation results relies on the accuracy of the input parameters and setup. In order to obtain an accurate model of the capacitor, all of its geometric dimensions were measured and used as inputs in the simulation model. All geometrical parameters were obtained by cross-section measurements, as shown in Figure 2. Figure 2 (a) is the side view of a typical capacitor with index for modeling, and Figures 2 (b) and (c) are the top and 3-dimesional views for an 8-terminal and 2-terminal capacitor, respectively. Based on all geometric dimensions and the material properties, the tool can now compute an $N \times N$ scattering matrix (S) for an N-terminal capacitor. For computing the equivalent impedance of the capacitor, the S matrix is converted into an $N \times N$ admittance matrix (Y). Imposing equal potential at terminals connected to power planes and ground planes respectively, the Y matrix can be reduced to an 1×1 impedance matrix as follows:

$$Zcap = \frac{1}{\sum Y_{ij}} \quad (1)$$

, where rows (i) and columns (j) for ground ports set to zeros.



(a)



(b) (c)

Figure 2. Geometry of capacitors for modeling: (a) side view, (b) eight-terminal capacitor's top view, and (c) two-terminal capacitor's 3-D view.

The full-wave tool developed at Intel was extensively tested with commercial full-wave software and validated with measured data. For the purpose of validation, an AVX 0612 0.47 μF 2-terminal capacitor was chosen, the complete geometry of which is shown in Figures 2 (a) and (c). In order to view the figure clearly, no specific parameters are presented. Two-port measurements using HP 8753D Vector Network Analyzer (VNA) were done for characterizing a frequency-dependent response of the capacitor in the range of 30 kHz to 3 GHz. Using SOLT (Short, Open, Load, and

Through) calibration, the two-port measurements were made with Cascade Microtech 250 μm GS and SG probe sets. However, since the capacitor itself cannot be measured directly, a test fixture structure shown in Figure 3 was attached for the measurement purpose. By neglecting very small voltage drop due to the separation between Ports 1 and 2, only a transfer S-parameter (S_{21}) can be used to extract such the small impedance of a capacitor (<< 25 ohms) since the two-port measurements reduce the error due to the series probe connection impedance and the transfer impedance becomes self impedance as the ports are closer [10]. Based on the two-port measurements, the unknown capacitor impedance can be computed as follows [10]:

$$Zcap = 25\frac{S_{21}}{1-S_{21}} \qquad (2)$$

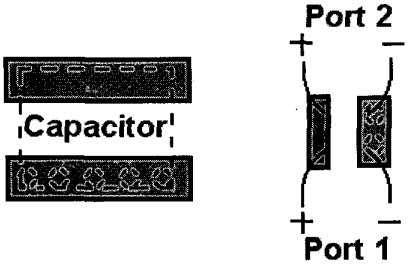


Figure 3. Test fixture structure for capacitor measurements.

Figure 4 shows the impedance comparison for an AVX 0612 0.47 μF 2-terminal capacitor between the measurements and simulation results. Based on the vendor's given material property parameters such as metal conductivity (σ), dielectric constant (ε), and loss tangent ($tan\ \delta$), the capacitor excluding the fixture structure was modeled and simulated with the measured geometry shown in Figure 2. The measurements included the fixture structure shown in Figure 3. As a result, there is a discrepancy in the high frequency results, which is caused by a horizontal and vertical inductance and resistance of the test fixture. To eliminate this effect, the resistance and inductance of the fixture were measured with the capacitor pad shorted. It is important to note that the fixture size needs to be as small as possible and its dielectric constant should be much smaller than that of the capacitor to make sure that the static capacitance of the fixture is negligible. Once the resistance and inductance of the fixture are measured by shorting the capacitor pads, the capacitance of the capacitor with its parasitic equivalent series resistance (ESR) and equivalent series inductance (ESL) can be de-embedded. As shown in Figure 4, ESL between the measurements and modeled simulation results shows a good correlation after de-embedding the test fixture. However, the measured and simulated capacitance and ESR still reveal a slight discrepancy and the simulation result shows a peak parallel resonance around 100 MHz which is not observed in the measurement. This could be due to some inaccuracies in the metal conductance and dielectric constant and loss tangent values that are fed into the simulation tool. As mentioned earlier, while geometry information was obtained by cross-section measurements, the material property parameters were obtained from the vendor's datasheet. As a result, while the modeling result shows 0.47 μF capacitance which matches the vendor's datasheet, the actual capacitance is measured to be around 0.43 μF. As another factor, the layers of capacitors are not uniformly flat, as shown in Figure 1 (b), which is not included in the simulation. By considering the null series resonance occurring around 20 MHz, the measured ESR is higher than the modeled ESR. As loss effects caused by metal resistivity and dielectric loss tangent increase, the impedance magnitude at null and peak resonant frequencies increases and decreases significantly, respectively [11]. As a result, the measured peak resonance occurring around 100 MHz was almost suppressed due to the high loss effect.

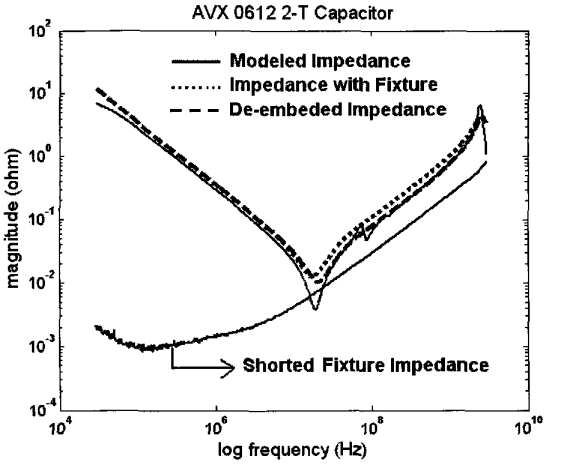


Figure 4. Impedance magnitude of AVX 0612 0.47 μF 2-terminal capacitor with and without test fixture structure.

As another example, to test the accuracy of the in-house full-wave tool for multi-terminal capacitors, the tool was compared with a commercial full-wave solver (HFSS). Figure 5 shows the metal layers of a 0805 8-termainal capacitor. To reduce overall inductance of the capacitor, all terminals are alternating in positive and negative polarities. Due to the large CPU run time associated with HFSS, the capacitor geometry was simplified to only include eight metal layers for power/ground planes. With the same input parameters shown in Figures 2 (a) and (b), both tools computed a 8×8 scattering matrix and an equivalent impedance. Figure 6 plots the magnitude of the capacitor impedance as a function of frequency using both methods. From the figure, we can see that the Intel developed tool shows very good correlation with the HFSS results while using a small fraction of the simulation time used by HFSS. We can now feel comfortable about extending the tool to model the entire capacitor structure, which includes hundreds of layers and a very high dielectric constant. This is something that cannot be done using a commercial full-wave solver like HFSS due to the large CPU run time and memory requirements. To compute the impedance response of the structure shown in Figure 5, the tool took less than 20 minutes. In addition, the tool can characterize realistic capacitors in large size, null resonance of which occurs at low frequency. As mentioned in the previous section, keeping the CPU run time low is important in order to enable parameter sweeps to identify the optimal capacitor.

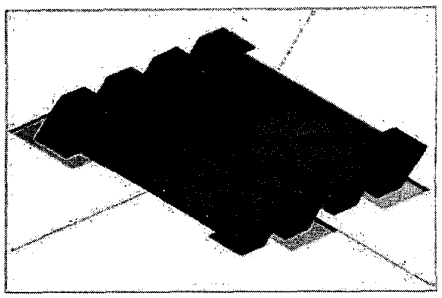


Figure 5. Power/ground plane layers of 0805 8-terminal capacitor.

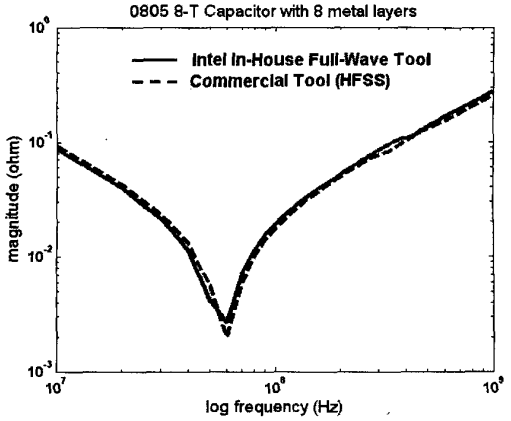


Figure 6. Impedance magnitude of 0805 8-terminal capacitor with eight power/ground metal layers.

Parametric Study for the Optimum Design of Capacitor

Once the in-house full-wave tool was validated with the measurements and commercial full-wave software, different design configurations of multi-terminal capacitors were extensively studied for the optimum performance of capacitors. Based on the geometrical parameters shown in Figure 2, the sensitivity of geometrical parameters was tested by sweeping the different input parameters. Figure 7 shows the impedance comparison as the parameters of interest are varied as 0.5X, X, and 2X while keeping other parameters fixed. Although the static capacitance of a capacitor can be simply estimated in proportion to the area and number of power/ground plane pairs, ESL needs to be more carefully considered. The ESL of a capacitor can be roughly explained by Figure 8. The total loop inductance of a capacitor (ESL) is the sum of $2L_v - 2M + L_h$, where L_v, L_h, and M denote vertical, horizontal, and mutual inductances, respectively. In order to examine the performance of a capacitor with respect to the configurations, several key parameters are adjusted to check the input impedance variation. Figure 7 (a) shows the impedance variation with increased number of layers. It is observed that as the number of power/ground plane pairs increases, the capacitance increases linearly as expected, but L_h reduces and becomes negligible. As a result, the ESL becomes close to $2L_v - 2M$. Figure 7 (b) illustrates capacitor performance vs. the width of capacitor, which is indicated as parameter "C" in Figure 2. By increasing the parameter 'C' with other parameters fixed, M reduces due to large separation between power and ground terminals, and therefore the overall ESL is increased. Meanwhile, because of the increased area between power and ground planes, the overall capacitance value is increased. In Figure 7 (c), by increasing "D", both L_v and M increases with the same capacitance; however, the sum of vertical and mutual inductance ($2L_v - 2M$) increases in proportion to the length of the parameter "D" which is the reason why all the capacitor manufacturers try to minimize "D". Figure 7 (d) shows impedance changing with variable "E". Because AC current always flow in its lowest impedance path, increasing of variable "E" (in the direction of outward capacitor) will not make any ESL and capacitance change, and that is why the impedance magnitudes are close in that graph. Figure 7 (e) shows the impact of impedance with respect to the variation of parameter "Y". It is clearly observed that both capacitance and ESL are both improved for decoupling capacitor purposes. While Figures 7 (a)-(e) focused on the parameters in a 2-terminal capacitor, Figure 7 (f) shows that the impedance variation as a function of the terminal width ("Q") in an IDC (8-terminal) capacitor. In the graph, as "Q" is increased, "R" is decreased to keep the pitch between the terminals constant. As expected, the terminal width has no impact on the capacitance of the structures. However, by increasing the terminal width, the mutual coupling between terminals of alternating polarities is increased which reduces the overall inductance. In addition the wider terminals also reduce the ESR of the capacitor. These effects can be seen from the graph in Figure 7 (f). The low ESL of IDC capacitors is one of the reasons why they are preferred over 2-terminal capacitors for high frequency decupling in power delivery application.

As a summary of these parameter sweepings, there are three strategies we can apply for better capacitor design. First, in order to increase capacitance without the additional side effect of ESL, the number of plane layers or dielectric constant need to be increased. Secondly, to reduce the ESL without losing capacitance, the shortest distance of the parameter "D" should be designed and manufactured. Third, to increase capacitance and to reduce inductance at the same time, the parameter "Y" in Figure 2 needs to be longer for both two-terminal capacitors and for multi-terminal capacitors. In addition, to maximize the effect of mutual inductance between terminals in multi-terminal capacitors, the separation "R" needs to be as small as possible.

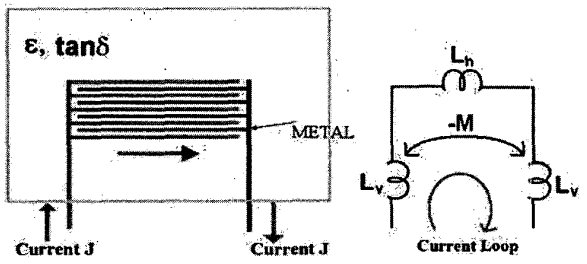


Figure 8. Equivalent loop inductance representation of a capacitor.

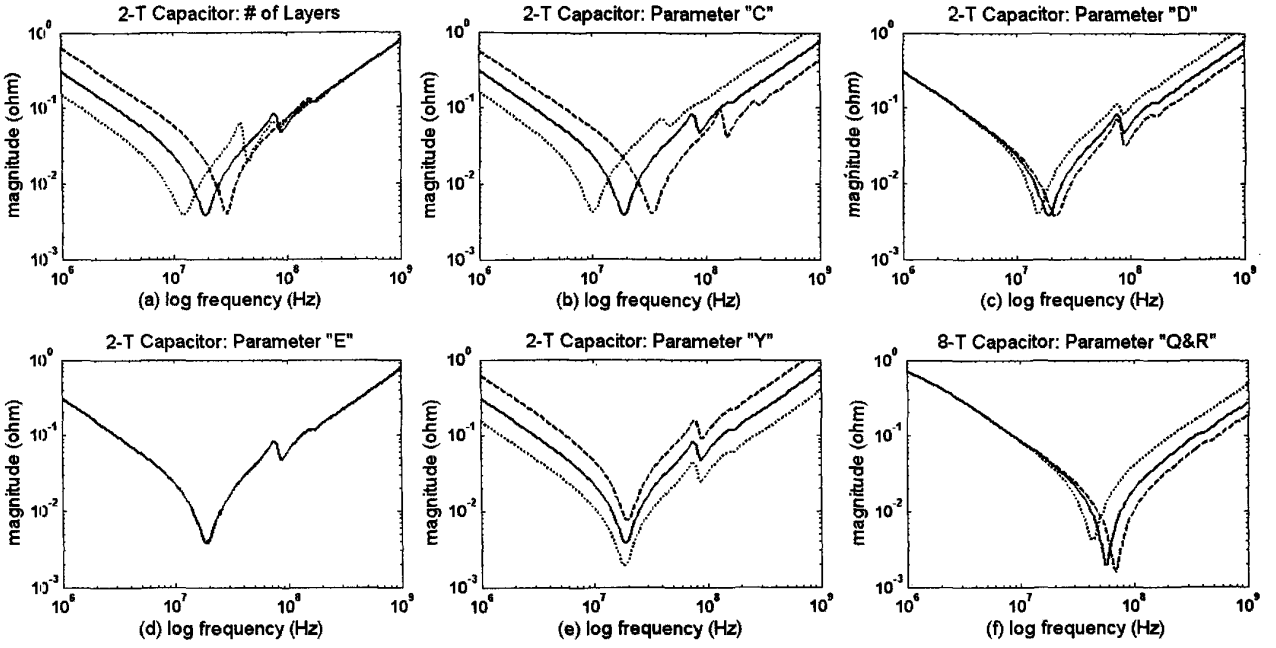


Figure 7 Input impedance with different design configurations: slide line-1X, dashed line-0.5X, and dotted line-2X of a parameter.

Higher-Order Model of a Capacitor and Applications

Conventionally, the typical model of a capacitor mounted on the package and board is a series lumped RLC network, creating series null resonant frequency. By the first approximation, capacitance, ESR, and ESL are extracted and modeled for the time domain analysis as frequency-independent parameters. Figure 9 shows the comparison of input impedance with different representations.

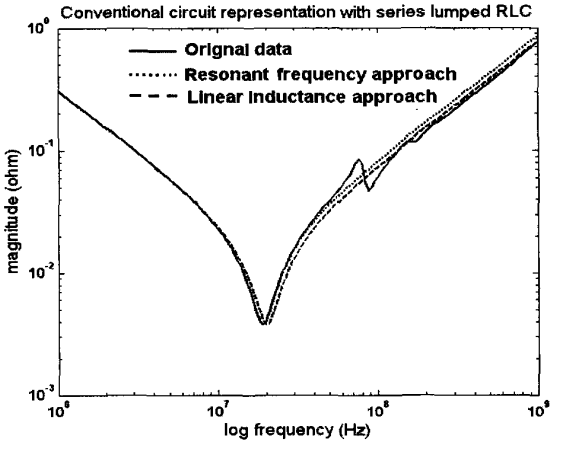


Figure 9 Input impedance with conventional series lumped RLC representations.

The first scheme is the full-wave S-parameter approach using the frequency dependent output directly obtained from the in-house full-wave solver. The second one used an equivalent series RLC representation where both ESR and ESL were obtained based on the null resonance frequency, and the last one applies linear inductance approach to obtain ESR at the null resonant frequency and ESL at the highest frequency. Although the magnitude in the low frequency range might match well, the resonant points and high frequency response are shifted. Especially, the frequency-independent representations do not capture the actual resistive response, where ESR is varied over the frequency range. The frequency-dependent ESR due to dielectric and skin losses is dominant in low and high frequency ranges, respectively. This may greatly impact design strategies for high frequency IO power delivery systems that require high ESR capacitors to reduce package natural resonance or coupled resonance generated between different kinds of bypass capacitors, or between package capacitor's ESL and on-chip capacitance.

To capture the frequency-dependent behavior of a capacitor, new circuitry has been applied with a higher-order representation, as shown in Figure 10. A parallel RC circuit represents the capacitance and dielectric loss that are dominant in a low frequency range. For representing the skin loss, a parallel RL circuit was used with a series lumped RLC. However, this representation does not include a higher order resonance as the conventional way shown in Figure 9 does not. To capture such a parallel resonant frequency, an additional parallel RLC circuit can be added, as shown in Figure 10 (b). All parameters can easily be extracted by using least-square approximations based on the circuit topology shown in Figure 10.

Figure 11 shows frequency-dependent impedance profile represented using the new circuitry shown in Figure 10. The figure contains not only magnitude but also real and imaginary parts to demonstrate the frequency dependency of a capacitor. As shown in the figure, the higher-order representation captures the frequency dependency of the

capacitance, ESL and the real part of impedance (ESR), which exhibits significantly variation as a function of frequency. In addition, the higher-order model based on Figure 10 (b) considers the discontinuity caused due to the parallel peak resonant frequency. Depending on the size and geometry of a capacitor or the number of layers, several series and parallel resonant frequencies are visible within the frequency range of interests. For practical applications requiring the small number of circuit elements, here, only the first dominant series and parallel resonant frequency were considered and modeled.

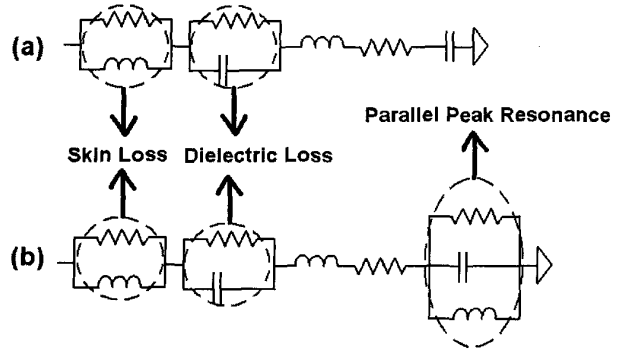


Figure 10 Equivalent circuit representation of a capacitor using higher-order approximation.

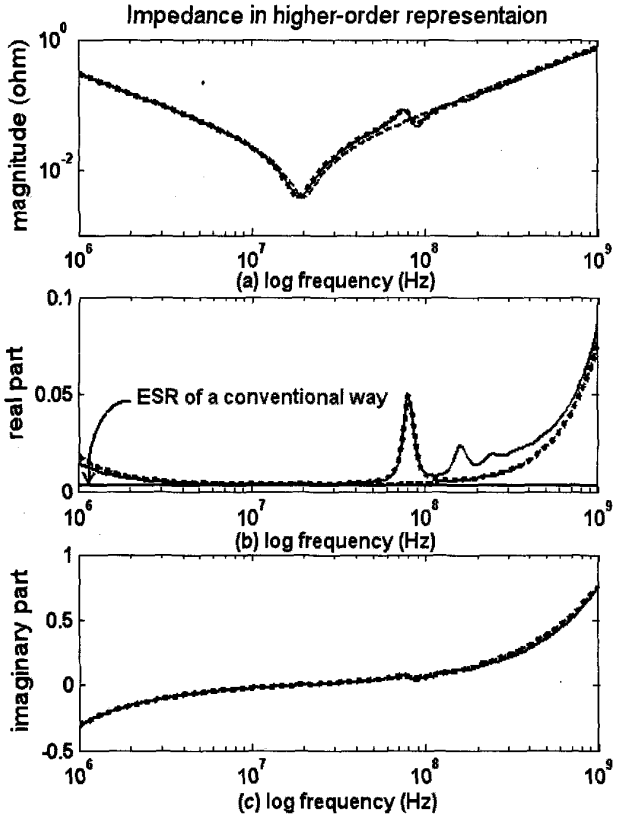


Figure 11. Input impedance of a capacitor using higher-order approximation: solide line - original data, dashed line - Figure 10 (a), and dotted line - Figure 10 (b).

To further investigate the concern mentioned above, a typical lumped power delivery network is used. Figure 12 shows the topology of the network. For a modern computer system operating at high frequency, switching circuits cause waves to propagate between power and ground planes in the package and board. These waves reflect from the edges of the package and board and cause resonant frequencies over the frequency range. Therefore, different decoupling capacitors should be used over the wide frequency range, depending on the package structure. Based on the resonant frequency, the decoupling capacitors can be categorized into low-frequency, mid-frequency, and high-frequency capacitors, and incorporated at appropriate places throughout the system, for filtering the frequency components of current changes caused by circuit switching. Typically, low-frequency and mid-frequency capacitors are mounted on the package and board, and high-frequency capacitors are buried in the chip as trench capacitors called on-chip capacitors, as shown in Figure 12.

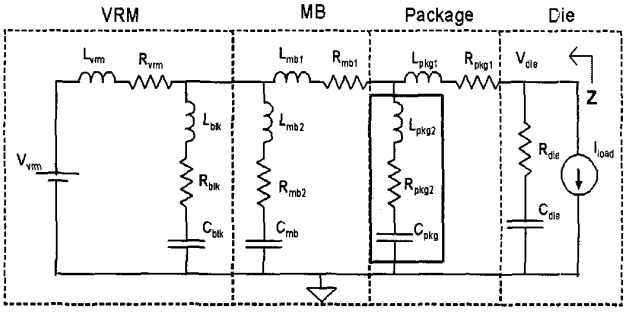


Figure 12 Typical computer system power delivery network.

Input impedance of power delivery network looking back from the circuit load shown in Figure 12 has been examined. The package decoupling capacitor is highlighted by the colored box that was switched in the 4 different schemes as described in Figures 9 and 11. Their input impedance is compared in Figure 13 with impedance computed using the original full-wave S-parameter of the capacitor. It can be seen from Figure 13 (a) that there is a large discrepancy between the full-wave S-parameter and other two schemes computed based on the conventional lumped RLC model at high frequency range, particularly at the highest resonant frequency that is coupled with the on-chip capacitor. On the contrary, the impedance computed based on the higher-order models results in better correlation within this frequency range, as shown in Figure 13 (b). Therefore, for a fixed impedance target, the higher-order model will require fewer capacitors compared with the conventional single element ESL, ESR and C approach. This phenomenon could be due to the higher ESR at high frequency range and higher order mode effects that cannot be captured by the conventional approach.

In a modern high-speed digital system, the noise budgets are typically measured in millivolts and it becomes critical to have accurate models for decoupling capacitors. As one of the most important components in a power delivery network, if decoupling capacitors are neither designed nor modeled properly, it could cripple the overall performance of the power delivery system.

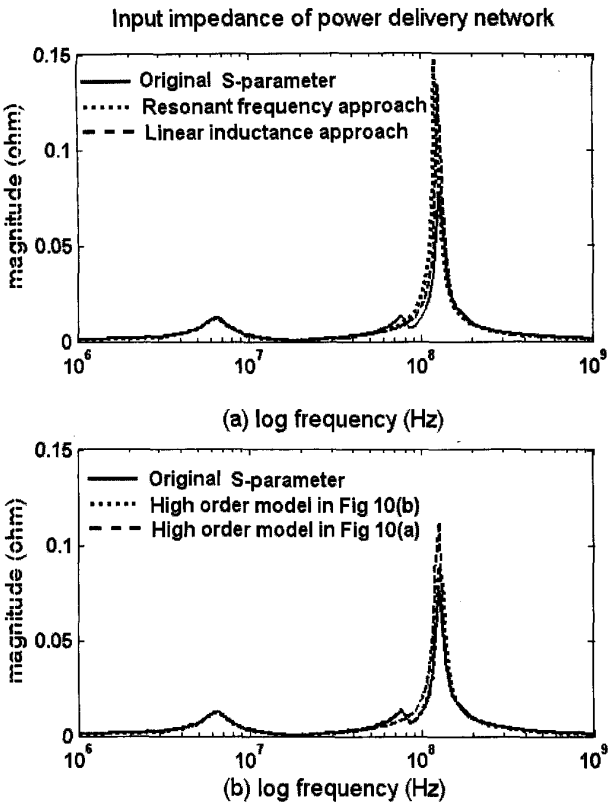


Figure 13. Input impedance of a typical computer system power delivery network: (a) conventional series lumped RLC model and (b) higher-order model.

Conclusions

Fast full-wave characterization of decoupling capacitors has been conducted. The accuracy and efficiency of the Intel developed full-wave solver has been validated by the comparisons with measurements and numerical experiments. Capacitor characterization with different design configurations has been demonstrated for the optimum design of capacitors. New higher-order circuit representations for capacitor components vs. single lumped element (ESR, ESL, and C) approaches have been compared. Full-wave S-parameter captures high frequency effects and therefore it predicts power delivery system impedance more accurately in high frequency region. The result shows that the ESL of a capacitor is dominated by capacitor terminal inductance and that the impact of planar layer section is a secondary effect. For fixed impedance target, the higher-order circuit approach can result in less number of capacitors required compared with a single lumped RLC.

The capacitor designs for a fixed target are not presented in this paper. With this tool, however, it is possible to find out the best capacitor configuration to match the requirements. For example, one can always increase the number of layers to increase the capacitance, and one can see the ESL and ESR changing with this incremental change or simply watch the overall frequency response. Material changes and process changes effects should be easily incorporated after one characterizes these parameters in term of electrical properties.

Acknowledgments

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