Rapid Modeling and Simulation of Integrated Circuit Layout in Both Frequency and Time Domains From the Perspective of Inverse

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***Abstract*— In this article, starting from full-wave partial differential equation (PDE)-based Maxwell's equations where E and H are coupled, we derive a closed-form model of the inverse of Maxwell's system of equations in the physical layout of an integrated circuit, package, and board. In this model, we decompose the inverse rigorously into R, C, L, and full-wave components, with neither numerical computation nor approximation, and for an arbitrary physical layout. As a result, each component can be found independently and then superposed to obtain the total response of a layout to any circuit stimuli. The time marching and point-by-point frequency sweeping are also avoided for the RC component as this component's time and frequency dependencies are analytically revealed in the proposed model. Moreover, the full-wave component is efficiently represented by a small number of high-frequency modes. Using the proposed model, not only many accuracy issues related to existing layout modeling can be addressed but also we drastically speed up layout modeling and simulation and provide circuit designers with an effective model for layout automation. In addition, we develop fast and large-scale algorithms to find each component of the inverse rapidly, where many steps are made analytical, thus further saving CPU run time. The proposed work has been applied to large-scale layout extraction and analysis. Superior performance has been demonstrated in accuracy, efficiency, and capacity.**

***Index Terms*— Broadband modeling, fast solvers, finite difference methods, full-wave analysis, integrated circuits (ICs), inverse, large-scale analysis, layout extraction, layout modeling, layout simulation, Maxwell's equations, model order reduction, RC extraction, simulation.**

I. Introduction

ACCURATE and large-scale layout models are of critical importance to the design of integrated circuits (ICs), packages, and boards. A physical design tool built upon inaccurate or erroneous layout models, no matter how superior it is in machine learning and optimization algorithms, will fail to generate a working layout within feasible run time.

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In prevailing layout modeling, static or quasi-static field solvers are employed to extract C-, R-, and L-based circuit models of the physical layout of an IC, package, or board [1]–[10]. These models are then stitched together to perform a circuit simulation. There are many ways to stitch the C models with the RL-models that are extracted independently of each other. Which one correctly captures the physics, such as distributed effects and 3-D effects in the physical layout, is unknown even at relatively low working frequencies, where static physics is dominant. As another example, the substrate is considered to be one of the main sources for interference and crosstalk. However, the global effect of the substrate is not well captured in existing layout models.

There exist, also, full-wave methods for layout modeling, such as the finite difference method [11], [12], the finite element method [13]–[18], and the integral equation-based method [19]–[25]. In these methods, no RLC extraction is performed, full-wave Maxwell's equations are directly solved to analyze the physical layout, and hence, the accuracy at high frequencies can be ensured. However, the direct field-based representation of the layout and the resulting field solution remain too abstract to be put into practical use by circuit designers for circuit diagnosis and performance optimization. A full-wave model is expected to reduce to the static- and quasi-static-based RLC models at low frequencies; however, this relationship is not established by existing full-wave solvers. In fact, full-wave solvers break down at low frequencies because of finite machine precision and the loss of frequency-dependent terms [26]–[29]. In addition, because full-wave solvers model more physics than their static and quasi-static-based counterparts, they are considered slower in CPU run time and smaller in the problem size they can handle.

From the aforementioned, it can be seen that in static- or quasi-static-based approaches, a forward model of the layout in a SPICE-compatible format, i.e., RLC-model, is constructed. This step is called extraction in the circuit community. After extraction, circuit simulation is performed on the extracted circuit model of the layout to analyze the layout response. In contrast, in a full-wave approach, no extraction is performed; the forward model of the layout is nothing but the discretized Maxwell's equations in the layout, which is then directly solved in the frequency or time domain. Both approaches focus on the forward model of the layout. This is understandable because given a system of equations in an

arbitrary layout, its solution or inverse generally is not known, and it has to be numerically found.

In this article, different from prevailing approaches where the forward model of the layout is constructed and then simulated, we analytically derive a closed-form model of the inverse of Maxwell's system of equations in the physical layout. We also derive such an inverse from full-wave Maxwell's equations where **E** and **H** are coupled so that we bypass the inaccuracy issue arising from stitching circuit models independently extracted from decoupled **E** and **H** equations. Moreover, the resultant model is correct from zero to high frequencies where Maxwell's equations are valid. More importantly, in the proposed inverse model, we are able to analytically decompose the layout response into R, C, L, and full-wave components with neither numerical computation nor approximation. As a result, each component can be obtained separately and then summed up to obtain a total layout response. This decomposed yet rigorous model greatly helps circuit diagnoses since now designers are able to analyze each component one by one and identify which component is the root cause for the design failure. Such a decomposition also facilitates efficient layout modeling and simulation since if an IC is dominated by RC effects, then we do not have to compute the full-wave component, and vice versa. Meanwhile, it makes parallelization straightforward. Unlike existing full-wave models, the proposed inverse model naturally reduces to its RLC-based counterpart at low frequencies, and it also avoids the inaccuracy issues caused by stitching R, L, and C elements in an empirical way. Furthermore, it reveals the relationship between a full-wave model and a static model of the layout in a single model and in a closed form.

In addition, we develop fast algorithms to obtain each component of the inverse rapidly. The time marching and point-by-point frequency sweeping are also avoided for the R and C components of the layout response as their time and frequency dependencies are analytically known in the proposed inverse model. The proposed work has been applied to large-scale layout extraction and analysis. Its performance in accuracy, efficiency, and capacity has been demonstrated.

This article is a significant expansion of [30]. In this article, we present a detailed derivation of the inverse of Maxwell's system of equations in the layout and show how it can be decomposed into R, C, L, and full-wave components. The analytical methods for finding the null-space governing the RC component are presented in both uniform and nonuniform grids. A fast algorithm for finding the full-wave component is developed, which significantly extends this work to analyze higher-frequency and larger-scale layouts. Many new and realistic examples are simulated to examine the performance of the proposed work. The rest of this article is organized as follows. In Section II, we introduce the background of this work and the difference between this work and existing work. In Section III, we present the proposed inverse model and its computation-free decomposition. In Section IV, we elaborate the analytical methods for finding the null-space vectors of the curl–curl operators, and explain how to efficiently find the RC component of the layout response. In Section V, we develop an efficient method for finding full-wave modes. In Section VI, extensive numerical results are presented to demonstrate the accuracy, efficiency, and capacity of the proposed work in layout modeling and simulation. We summarize this article in Section VII.

II. Background

A. Discretization of Full-Wave Maxwell's Equations in a Physical Layout

Consider an arbitrary layout of analog and mixed-signal ICs, packages, and boards, which consists of interconnects, RF/analog components, substrates, materials, and so on. The physical phenomena in such a layout from dc to high frequencies are governed by Maxwell's equations as the following:

$$\begin{aligned} \nabla \times \mathbf{E} &= -\mu_r \mu_0 \frac{\partial \mathbf{H}}{\partial t} \\ \nabla \times \mathbf{H} &= \sigma \mathbf{E} + \varepsilon \frac{\partial \mathbf{E}}{\partial t} + \mathbf{J} \end{aligned} \tag{1}$$

where μ_0 is free-space permeability, μ_r is relative permeability, ε is permittivity, σ is conductivity, $\mathbf{J}$ is current density, and $\mathbf{r}$ denotes a point in a 3-D space.

We discretize the entire physical layout into a grid to capture the geometry and inhomogeneous materials. A Cartesian grid is used instead of irregular meshes because it is natural for discretizing a majority of the layout structures, and also it removes the step of 3-D meshing that can be computationally expensive. Using an FDTD method [12], [31] to discretize (1) and also to eliminate the magnetic field unknown, we can obtain the following linear system of equations:

$$\mathrm{diag}\{\epsilon\}\frac{d^2 e}{dt^2} + \mathrm{diag}\{\sigma\}\frac{de}{dt} + \mathbf{S}e = -\frac{dJ}{dt} \tag{2}$$

where e denotes a vector consisting of the tangential electric field along each edge of the grid whose number is N_e, J is a vector of current density, and $\mathrm{diag}\{\epsilon\}$ and $\mathrm{diag}\{\sigma\}$ are diagonal matrices of permittivity and conductivity, respectively. $\mathbf{S}$ in (2) is a sparse matrix, and $\mathbf{S}e$ represents a discretized $\nabla \times [\mu^{-1} \nabla \times \mathbf{E}]$ operation.

Equation (2) has an obvious frequency-domain counterpart as the following:

$$-\omega^2 \mathrm{diag}\{\epsilon\} e(\omega) + j\omega \mathrm{diag}\{\sigma\} e(\omega) + \mathbf{S}e(\omega) = -j\omega J(\omega) \tag{3}$$

which we denote in short by

$$\mathbf{Y}(\omega) e(\omega) = \mathbf{I}(\omega) \tag{4}$$

where

$$\mathbf{Y}(\omega) = \mathbf{D} + \mathbf{S} \tag{5}$$

and

$$\mathbf{D} = -\omega^2 \mathrm{diag}\{\epsilon\} + j\omega \mathrm{diag}\{\sigma\} \tag{6}$$

is diagonal.

B. Difference Between the Proposed Work and Existing Layout Modeling and Simulation Methods

In existing layout modeling and simulation methods, static- and quasi-static-based approaches do not solve a full-wave system, such as (2) or (3). Instead, they solve an electrostatic equation for C-extraction [2], [3], [5]–[7]; a quasi-magnetostatic equation for RL extraction [4], [8]. The R, C, and L elements are then stitched together to build a SPICE model of the layout, upon which a circuit simulation is performed.

In full-wave-based modeling and simulation methods, the system of equations, such as (2) and (3), is directly solved without performing an RLC extraction. However, the direct field-based representation of the layout and the resulting field solution are abstract for circuit designers to put into practical use. Furthermore, even for layouts dominated by static effects, one still has to solve the entire full-wave equation, i.e., no terms can be dropped directly from (2) and (3) to simplify the analysis. Moreover, a full-wave model should reduce to the static- and quasi-static-based RLC models at low frequencies; however, a brute-force solution of (2) and (3) does not reveal such a relationship. In fact, full-wave solvers break down at low frequencies. Many methods have been studied to extend the full-wave solvers to low frequencies, which add extra computational cost [26]–[29]. Some stitch static and quasi-static solvers with the full-wave solutions. However, it is unknown how to stitch them in a rigorous way. Furthermore, the capacity of existing full-wave solvers is limited when a full-chip and/or complete-package analysis is required.

In this article, our approach is to derive a closed-form model of the inverse of $\mathbf{Y}$. Since this model starts from the full-wave Maxwell's equations, it is valid from zero to high frequencies. In this inverse model, we analytically identify R, C, L, and full-wave components. This approach has not been explored in previous methods. It naturally reduces to a static RLC-model at low frequencies and reveals that the complete layout model is an exact summation of the RLC-model and the full-wave model in the inverse. For layouts dominated by static effects, no extra computation is needed for finding the full-wave component, and vice versa. We also develop fast methods to find each component of the inverse efficiently.

III. Proposed Closed-Form Model of the Inverse of $\mathbf{Y}$ and Its Decomposition Into R, C, L, and Full-Wave Components

Using the new single-grid patch-based formulation of the FDTD developed in [34], $\mathbf{S}$ in (2) can be written as a summation of a rank-1 matrix of each patch over all patches in a grid regardless of whether the grid is 2-D or 3-D. To elaborate, for each patch, we generate one row vector $\mathbf{S}_e^{(i)}$ shown as the following:

$$\mathbf{S}_e^{(i)} = \left[-\frac{1}{L_i} \quad \frac{1}{L_i} \quad \frac{1}{W_i} \quad -\frac{1}{W_i}\right] \oplus \text{zeros}(1, N_e) \tag{7}$$

where $\oplus$ denotes an extended addition based on the global indexes of the four local $\mathbf{E}$ unknowns of patch i, and L_i and W_i are, respectively, the two side lengths of patch i. We also generate one column vector $\mathbf{S}_h^{(i)}$ in each patch. In a uniform grid, the following is true:

$$\mathbf{S}_h^{(i)} = \left(\mathbf{S}_e^{(i)}\right)^T. \quad \text{(Uniform grid).} \tag{8}$$

In a nonuniform grid, for better accuracy, we should replace the length in $\mathbf{S}_h^{(i)}$ by an average length across the two patches sharing the $\mathbf{E}$ edge. Hence

$$\mathbf{S}_h^{(i)} = \left[-\frac{1}{L_{i1}^{\text{ave}}} \quad \frac{1}{L_{i2}^{\text{ave}}} \quad \frac{1}{L_{i3}^{\text{ave}}} \quad -\frac{1}{L_{i4}^{\text{ave}}}\right]^T \oplus \text{zeros}(N_e, 1) \quad \text{(Nonuniform grid)} \tag{9}$$

where the subscripts $i1, \ldots, i4$ denote the four edge indexes in the ith patch, and the superscript ave denotes an average length.

Multiplying $\mathbf{S}_h^{(i)}$ by $\mathbf{S}_e^{(i)}$ and adding the resultant rank-1 matrix of each patch, we obtain a global $\mathbf{S}$ as the following:

$$\mathbf{S} = \sum_{i=1}^{N_h} {\mu_i}^{-1} \left(\mathbf{S}_h^{(i)}\right)\left(\mathbf{S}_e^{(i)}\right) \tag{10}$$

where N_h is the patch number, which is also the number of magnetic field unknowns. The above-mentioned equation can also be rewritten as

$$\mathbf{S} = \mathbf{S}_h \mathbf{D}_{1/\mu} \mathbf{S}_e \tag{11}$$

in which $\mathbf{S}_h$'s ith column is $\mathbf{S}_h^{(i)}$, whereas $\mathbf{S}_e$'s ith row is $\mathbf{S}_e^{(i)}$ and $\mathbf{D}_{1/\mu}$ is a diagonal matrix of μ^{-1}.

$\mathbf{S}$ has a null-space, which is evident from (11) as $\mathbf{S}_h$'s column number N_h is less than row number N_e. Since $\mathbf{S}$ represents a discretized $\nabla \times \mu^{-1} \nabla \times$ operation, the null-space represents a gradient field in the grid. Let it be $\mathbf{V}_0$. It satisfies

$$\mathbf{S}\mathbf{V}_0 = 0. \tag{12}$$

Let $\mathbf{V}_h$ be its complementary space. The number of vectors in $\mathbf{V}_0$ and $\mathbf{V}_h$ is equal to the matrix size of $\mathbf{S}$. Therefore, the solution of (3) can be rigorously expanded in the space of $[\mathbf{V}_0 \quad \mathbf{D}^{-1}\mathbf{V}_h]$ as the following:

$$e = \underbrace{\mathbf{V}_0 y_0}_{\text{RC-effects}} + \underbrace{\mathbf{D}^{-1}\mathbf{V}_h y_h}_{\text{RL and full-wave effects}}. \tag{13}$$

Here, we use $[\mathbf{V}_0 \quad \mathbf{D}^{-1}\mathbf{V}_h]$ instead of $[\mathbf{V}_0 \quad \mathbf{V}_h]$ because in this way, after testing (3) by $\mathbf{V}_0^T$ and $(\mathbf{D}^{-1}\mathbf{V}_h)^T$, we can decouple the solution of y_0 from that of y_h, which will become clear in the sequel. Otherwise, the two are coupled, and it becomes difficult to develop an explicit inverse model. In addition, since $\mathbf{D}$ is diagonal, computing $\mathbf{D}^{-1}$ is trivial. The $\mathbf{V}_0$ component of e has a zero curl; hence, it represents the RC component of the layout response, as noted in (13). In contrast, the $\mathbf{V}_h$ component characterizes the inductance and full-wave effects.

$\mathbf{V}_0$ can be found by solving the eigenvectors of $\mathbf{S}$ corresponding to zero eigenvalues; however, this is computationally expensive. In this article, we develop an analytical method for finding $\mathbf{V}_0$ solely based on the mesh information, thus removing the cost of numerically computing $\mathbf{V}_0$. The details are given in Section IV. As far as $\mathbf{V}_h$ is concerned, if we use the eigenvectors of $\mathbf{S}$ corresponding to the nonzero eigenvalues, we can also find an analytical way to obtain them.

However, the number of such $\mathbf{V}_h$ can be too many to use even for an electrically small structure. For example, a static field distribution can also be decomposed into many of such $\mathbf{V}_h$ modes since the static field distribution can also have a rapid space variation. In contrast, if using the eigenvectors of a quadratic eigenvalue problem governing (2), the number of $\mathbf{V}_h$ required is small since each of these eigenvectors is a source-free solution of the original problem. The weight of these modes in the field solution is inversely proportional to the magnitude of the eigenvalue [32]. Nevertheless, solving the quadratic eigenvalue problem can also be computationally expensive. In this article, we develop an efficient solution for finding $\mathbf{V}_h$, and the details of which are given in Section V.

Now, assuming $\mathbf{V}_0$ and $\mathbf{V}_h$ have been obtained, we show how to derive a closed-form model of the inverse. To find the solution of y_0, we can substitute (13) into (3) and multiply (3) from the left-hand side by $\mathbf{V}_0^T$, obtaining

$$\mathbf{V}_0^T(\mathbf{D}+\mathbf{S})(\mathbf{V}_0\boldsymbol{y}_0+\mathbf{D}^{-1}\mathbf{V}_h y_h) = -j\omega\mathbf{V}_0^T J. \tag{14}$$

If $\mathbf{V}_0^T\mathbf{S}=0$, then the above-mentioned equation can be readily simplified to

$$\mathbf{V}_0^T\mathbf{D}\mathbf{V}_0\boldsymbol{y}_0 = -j\omega\mathbf{V}_0^T J. \tag{15}$$

However, we find the above-mentioned equation is only true in a uniform grid. This is because in a uniform grid, $\mathbf{S}$ is symmetric; hence, from $\mathbf{S}\mathbf{V}_0 = 0$, taking a transpose, we obtain $\mathbf{V}_0^T\mathbf{S}=0$. This is not the case in a nonuniform grid, as can be seen from (9). A nonuniform grid is unavoidable in discretizing a physical layout. If using a uniform grid, then the number of discretzation cells could be too many to be computed efficiently due to the presence of various fine features in the layout. This problem is solved in this article by finding a left null-space of $\mathbf{S}$ and also analytically. This left null-space is denoted by $\mathbf{V}_{0a}$, which satisfies

$$\mathbf{V}_{0a}^T\mathbf{S}=0 \tag{16}$$

while preserving the property of

$$\mathbf{V}_{0a}^T\mathbf{V}_h = 0. \tag{17}$$

The analytical approach for finding $\mathbf{V}_{0a}$ is detailed in Section IV.

Multiplying $\mathbf{V}_{0a}^T$ on both sides of (3) and utilizing (16) and (17), we obtain

$$\mathbf{V}_{0a}^T(-\omega^2\mathrm{diag}\{\epsilon\}+j\omega\mathrm{diag}\{\sigma\})\mathbf{V}_0\boldsymbol{y}_0 = -j\omega\mathbf{V}_{0a}^T J \tag{18}$$

which is a system of equations for $\boldsymbol{y}_0$ only, and hence, we can solve the above-mentioned equation without concerning about the $\boldsymbol{y}_h$ component. We further decompose the solution of the above-mentioned equation into

$$\mathbf{V}_0\boldsymbol{y}_0 = \mathbf{V}_{0d}\boldsymbol{y}_{0d}+\mathbf{V}_{0c}\boldsymbol{y}_{0c} \tag{19}$$

where $\mathbf{V}_{0d}$ is in the null-space of $\mathrm{diag}\{\sigma\}$, denoting the field outside the conductors, and $\mathbf{V}_{0c}$ is $\mathbf{V}_{0d}$'s complementary space in $\mathbf{V}_0$. These two column spaces can again be analytically obtained without any computation, and the details of which are given in Section IV. The left null-space $\mathbf{V}_{0a}$ can also be decomposed into $\mathbf{V}_{0\mathrm{da}}$ and $\mathbf{V}_{0\mathrm{ca}}$, in the same way as $\mathbf{V}_0$ is decomposed into $\mathbf{V}_{0d}$ and $\mathbf{V}_{0c}$. Substituting (19) into (18), the resulting rows of equations corresponding to $\mathbf{V}_{0\mathrm{da}}$ can be written as

$$\mathbf{V}_{0\mathrm{da}}^T(-\omega^2\mathrm{diag}\{\epsilon\}+j\omega\mathrm{diag}\{\sigma\})(\mathbf{V}_{0d}\boldsymbol{y}_{0d}+\mathbf{V}_{0c}\boldsymbol{y}_{0c}) = -j\omega\mathbf{V}_{0\mathrm{da}}^T J \tag{20}$$

and the rest corresponding to $\mathbf{V}_{0\mathrm{ca}}$ can be written as

$$\mathbf{V}_{0\mathrm{ca}}^T(-\omega^2\mathrm{diag}\{\epsilon\}+j\omega\mathrm{diag}\{\sigma\})(\mathbf{V}_{0d}\boldsymbol{y}_{0d}+\mathbf{V}_{0c}\boldsymbol{y}_{0c}) = -j\omega\mathbf{V}_{0\mathrm{ca}}^T J. \tag{21}$$

Since $\mathrm{diag}\{\sigma\}\mathbf{V}_{0d}=0$ and $\mathbf{V}_{0\mathrm{da}}^T\mathrm{diag}\{\sigma\}=0$, (20) can be rewritten as

$$\mathbf{V}_{0\mathrm{da}}^T(j\omega\mathrm{diag}\{\epsilon\})\mathbf{V}_{0d}y_{0d}+\mathbf{V}_{0\mathrm{da}}^T(j\omega\mathrm{diag}\{\epsilon\})\mathbf{V}_{0c}y_{0c} = -\mathbf{V}_{0\mathrm{da}}^T J. \tag{22}$$

Also, because $\mathrm{diag}\{\sigma\}\mathbf{V}_{0d}=0$, (21) becomes

$$\mathbf{V}_{0\mathrm{ca}}^T(j\omega\mathrm{diag}\{\epsilon\})\mathbf{V}_{0d}y_{0d}+\mathbf{V}_{0\mathrm{ca}}^T(j\omega\mathrm{diag}\{\epsilon\}+\mathrm{diag}\{\sigma\})\mathbf{V}_{0c}y_{0c} = -\mathbf{V}_{0\mathrm{ca}}^T J. \tag{23}$$

Because in the conductor, the displacement current is much smaller than the conduction current, and (23) can be accurately approximated as

$$\mathbf{V}_{0\mathrm{ca}}^T(j\omega\mathrm{diag}\{\epsilon\})\mathbf{V}_{0d}y_{0d}+\mathbf{V}_{0\mathrm{ca}}^T\mathrm{diag}\{\sigma\}\mathbf{V}_{0c}y_{0c} = -\mathbf{V}_{0\mathrm{ca}}^T J. \tag{24}$$

Notice that the displacement current ignored in the above-mentioned equation is the displacement current inside conductors. This can be done because for $\omega\epsilon$ to be higher than σ inside a good conductor of 10^7 conductivity, the frequency has to be higher than 10^{17} Hz. In addition, when the working frequency is really that high, the curl of electric field is not zero any more, and hence, there is no need to find the $\mathbf{V}_0$ solution.

In order to solve y_0, we first solve the imaginary part of y_{0d}, $\mathrm{Im}[y_{0d}]$, from (22) as

$$\mathrm{Im}[y_{0d}] = \frac{\left(\mathbf{V}_{0\mathrm{da}}^T\mathrm{diag}\{\epsilon\}\mathbf{V}_{0d}\right)^{-1}\left(\mathbf{V}_{0\mathrm{da}}^T J\right)}{\omega}. \tag{25}$$

Denote it in short by $y_{0d,i}/\omega$. We then substitute $\mathrm{Im}[y_{0d}]$ into (24) to solve y_{0c}, which is

$$y_{0c} = \left(\mathbf{V}_{0\mathrm{ca}}^T\mathrm{diag}\{\sigma\}\mathbf{V}_{0c}\right)^{-1}\left(-\mathbf{V}_{0\mathrm{ca}}^T J+\mathbf{V}_{0\mathrm{ca}}^T\mathrm{diag}\{\epsilon\}\mathbf{V}_{0d}y_{0d,i}\right). \tag{26}$$

After getting y_{0c}, we substitute it back to (22) to obtain the real part of y_{0d}, which is

$$\mathrm{Re}[y_{0d}] = -\left(\mathbf{V}_{0\mathrm{da}}^T\mathrm{diag}\{\epsilon\}\mathbf{V}_{0d}\right)^{-1}\left(\mathbf{V}_{0\mathrm{da}}^T\mathrm{diag}\{\epsilon\}\mathbf{V}_{0c}y_{0c}\right). \tag{27}$$

Equations (25)–(27) make the complete solution of y_0 in (19).

Multiplying $(\mathbf{D}^{-1}\mathbf{V}_{h1})^T$ on both sides of (3) (where $\mathbf{V}_{h1}^T\mathbf{V}_0=0$), we obtain

$$\left(\mathbf{V}_{h1}^T\mathbf{D}^{-1}\mathbf{Y}\mathbf{D}^{-1}\mathbf{V}_h\right)y_h = -j\omega\mathbf{V}_{h1}^T\mathbf{D}^{-1}J \tag{28}$$

from which y_h can be solved.

Summarizing the results in (25)–(28), we obtain a final model of the inverse of $\mathbf{Y}$ as

$$\begin{aligned}\mathbf{Y}^{-1} &= \underbrace{\mathbf{V}_{0d}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\mathrm{da}}^{T}}_{\text{C component}}/(-j\omega) \\ &+ \underbrace{\mathbf{V}_{0d}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\mathrm{da}}^{T}\mathrm{diag}\{\epsilon\}\mathbf{V}_{0c}\mathbf{D}_{\sigma,0}^{-1}\mathbf{V}_{0\mathrm{ca}}^{T}\left(\mathbf{I}-\mathrm{diag}\{\epsilon\}\mathbf{V}_{0d}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\mathrm{da}}^{T}\right)}_{\text{R component}} \\ &\underbrace{+\mathbf{V}_{0c}\mathbf{D}_{\sigma,0}^{-1}\mathbf{V}_{0\mathrm{ca}}^{T}\left(\mathrm{diag}\{\epsilon\}\mathbf{V}_{0d}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\mathrm{da}}^{T}-\mathbf{I}\right)}_{\text{R component}} \\ &- j\omega\underbrace{\mathbf{D}^{-1}\mathbf{V}_{h}\left(\mathbf{V}_{h1}^{T}\mathbf{D}^{-1}\mathbf{Y}\mathbf{D}^{-1}\mathbf{V}_{h}\right)^{-1}\mathbf{V}_{h1}^{T}\mathbf{D}^{-1}}_{\text{L and full-wave component}} \end{aligned} \tag{29}$$

in which

$$\mathbf{D}_{\epsilon,0} = \mathbf{V}_{0\mathrm{da}}^{T}\mathrm{diag}\{\epsilon\}\mathbf{V}_{0d} \tag{30}$$

$$\mathbf{D}_{\sigma,0} = \mathbf{V}_{0\mathrm{ca}}^{T}\mathrm{diag}\{\sigma\}\mathbf{V}_{0c} \tag{31}$$

are both frequency independent. From (29), we can clearly identify the C, R, L, and full-wave components of the layout response. For the RC component, their frequency, and hence time dependence, are also analytically revealed. In the following, we present fast algorithms for computing each component.

It is also worth mentioning although (2) is free of matrix solution in its explicit time marching, direct simulation of (2) is computationally prohibitive for large layouts because a tremendous number of time steps must be simulated due to the extremely small space step. Meanwhile, even though the simulation can be carried out, the field-based solution is not circuit intuitive and is difficult to be used to guide the design. In addition, one cannot separately obtain each component of the layout response, such as in the proposed method.

On the Truncation Boundary Condition: The integrated circuit layout problem is, in general, a closed-region problem, where a perfect electric conductor (PEC) or first-kind boundary condition, or a perfect magnetic conductor (PMC, also known as the Neumann or second-kind boundary condition) is imposed. For structures that have strong radiation, an absorbing boundary condition (ABC) may need to be used. However, the numerical system inside the solution domain remains the same as (2), such as that shown in [35]. Specifically, with an ABC, such as a perfectly matched layer (PML), (2) becomes

$$\mathrm{diag}\{\epsilon\}\frac{d^2\,e}{dt^2}+\mathrm{diag}\{\sigma\}\frac{de}{dt}+\mathbf{S}e=-\frac{dJ}{dt}-\mathbf{S}_h h_b \tag{32}$$

where h_b denotes the magnetic field adjacent to the solution domain in the PML region. Notice that in the FDTD, an electric field is obtained from the curl operation on its four surrounding magnetic fields. For an electric field located at the interface between PML and the solution domain, its solution at the next time instant requires a magnetic field solution in the PML region at the previous time step. This is what the $\mathbf{S}_h h_b$ term stands for in (32). As can be seen from (32), the left-hand side system matrix remains the same as that in the solution domain, and hence, the proposed inverse model is equally applicable. We only need to build the inverse model for the solution domain, whereas the fictitious absorber can be simulated as it is. In this article, we use the first- or second-kind boundary conditions to truncate the solution domain, as the structures simulated do not have strong radiations. Other boundary conditions will be incorporated into our future work.

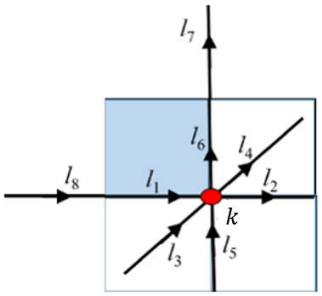

Fig. 1. Illustration of the null-space vector at a node.

IV. Analytical Method for Finding $\mathbf{V}_0$ and Efficient Computation of the RC Component of Layout Response

We find an analytical method to generate $\mathbf{V}_0$ from the mesh information without the need for solving an eigenvalue problem of $\mathbf{S}$. The number of $\mathbf{V}_0$ modes is the total number of nodes in the grid n minus 1

$$\#\mathbf{V}_0 = n - 1. \tag{33}$$

Each node has a null-space vector, whose number of nonzero entries is the number of edges connected to the node. Such a vector can be generated in the following way.

1) If the electric field reference direction along an edge enters the node, $(1/l_i)$ appears on the row corresponding to the global e index of this edge.
2) If the electric field reference direction along the edge leaves the node, $-(1/l_i)$ appears on the row corresponding to the global index of this e edge.

Here, l_i is the length of the ith edge, at which the ith electric field unknown is located. In the above-mentioned equation, we use a positive sign for edges whose directions enter the node and a minus sign for edges leaving the node. Certainly, an opposite sign convention can also be used. An edge's direction here is referred to as the electric field reference direction defined on the edge. The aforementioned description could be abstract, take the node k shown in Fig. 1 as an example, and its associated null-space vector can be written as

$$\mathbf{V}_{0,k} = \left[\frac{1}{l_1}, -\frac{1}{l_2}, \frac{1}{l_3}, -\frac{1}{l_4}, \frac{1}{l_5}, -\frac{1}{l_6}\right]^T \oplus \mathrm{zeros(Ne, 1)} \tag{34}$$

in which $\oplus$zeros(Ne, 1) again denotes adding the preceding nonzero entries associated with each edge at the rows corresponding to the global index of the edge, in a vector of length N_e. Because $\mathbf{S}$ has a format shown in (10), when multiplying $\mathbf{S}$ by the $\mathbf{V}_{0,k}$, only those patches that contain the six edges associated with the node are involved in the product of $\mathbf{S}\mathbf{V}_{0,k}$. The number of such patches is 12 in a 3-D grid and 4 in a

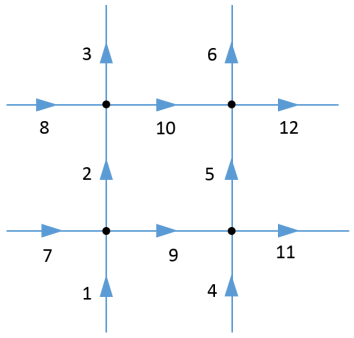

Fig. 2. Illustration of the null-space vector for PEC boundary nodes.

2-D grid. On each of these patches, $\mathbf{S}_e^{(i)}\mathbf{V}_{0,k} = 0$, and hence, $\mathbf{S}\mathbf{V}_{0,k} = 0$ is satisfied. To see this point clearly, take the blue patch shown in Fig. 1 as an example, its $\mathbf{S}_e^{(i)}$ can be written as

$$\mathbf{S}_e^{(i)} = \left[\frac{1}{l_6}, -\frac{1}{l_6}, \frac{1}{l_1}, -\frac{1}{l_1}\right] \oplus \text{zeros}(1, N_e). \tag{35}$$

When multiplying the above-mentioned equation by $\mathbf{V}_{0,k}$, we obtain

$$\mathbf{S}_e^{(i)}\mathbf{V}_{0,k} = \frac{1}{l_6 l_1} - \frac{1}{l_6 l_1} = 0. \tag{36}$$

The same is true for all other patches that own node k.

When there is a PEC boundary condition, all the null-space vectors generated for the nodes on the PEC boundary should be added up, thus becoming one vector. This is because all the nodes on the PEC have the same potential. For example, in Fig. 2, if the PEC includes all the four nodes, then the null-space vector corresponding to the PEC can be written as

$$v_0 = \begin{bmatrix} 1/l_1 \\ 0 \\ -1/l_3 \\ 1/l_4 \\ 0 \\ -1/l_6 \\ 1/l_7 \\ 1/l_8 \\ 0 \\ 0 \\ -1/l_{11} \\ -1/l_{12} \end{bmatrix}. \tag{37}$$

For a nonuniform grid, since $\mathbf{S}$ is not symmetric anymore, the aforementioned $\mathbf{V}_0$ satisfies $\mathbf{S}\mathbf{V}_0 = 0$, but it does not make $\mathbf{V}_0^T\mathbf{S}$ vanish. Thus, we also find a way to analytically generate the left null-space of $\mathbf{S}$, $\mathbf{V}_{0a}$. For each node, there is also one $\mathbf{V}_{0a}$ vector. The nonzero entries in this vector are at the same entries as those in $\mathbf{V}_0$. However, different from $\mathbf{V}_0$, we need to use an average length to build $\mathbf{V}_{0a}$ instead of the original length of the edge. The rule to generate a $\mathbf{V}_{0a}$ vector is as follows.

1) If the electric field reference direction along an edge enters the node, $(1/l_i^{\text{ave}})$ appears on the row corresponding to the global e index of this edge, where l_i^{ave} denotes the average length of edge i and its adjacent edge connected to the node along the same direction;
2) If the electric field reference direction along an edge leaves the node, $-(1/l_i^{\text{ave}})$ appears on the row corresponding to the global e index of this edge, where l_i^{ave} denotes the average length of edge i and its adjacent edge connected to the node along the same direction.

Using the node k shown in Fig. 1 as an example, its $\mathbf{V}_{0a}$ vector can be written as

$$\mathbf{V}_{0a,k} = \left[\frac{2}{l_1+l_2}, -\frac{2}{l_1+l_2}, \frac{2}{l_3+l_4} - \frac{2}{l_3+l_4} \right. \\ \left. \frac{2}{l_5+l_6}, -\frac{2}{l_5+l_6}\right]^T \oplus \text{zeros(Ne, 1)}. \tag{38}$$

When computing $\mathbf{V}_{0a,k}^T\mathbf{S}$, $\mathbf{V}_{0a,k}^T$ is multiplied by $\mathbf{S}_h$. In a nonuniform grid, $\mathbf{S}_h^{(i)}$ has a form shown in (9), where the average length is used. Take the blue patch shown in Fig. 1 as an example, its $\mathbf{S}_h^{(i)}$ can be written as

$$\mathbf{S}_h^{(i)} = \left[\frac{2}{l_5+l_6}, -\frac{2}{l_6+l_7}, \frac{2}{l_1+l_2} - \frac{2}{l_1+l_8}\right]^T \oplus \text{zeros}(N_e, 1). \tag{39}$$

When multiplying $\mathbf{V}_{0a,k}^T$ by the above-mentioned equation, we obtain

$$\mathbf{V}_{0a,k}^T\mathbf{S}_h^{(i)} = \frac{2}{l_1+l_2}\frac{2}{l_5+l_6} - \frac{2}{l_1+l_2}\frac{2}{l_5+l_6} = 0. \tag{40}$$

As can be seen, the average length is used in $\mathbf{V}_{0a,k}$ to vanish $\mathbf{V}_{0a,k}^T\mathbf{S}_h^{(i)}$.

In (19), we further decompose $\mathbf{V}_0$ into two sets: $\mathbf{V}_{0d}$ and $\mathbf{V}_{0c}$. $\mathbf{V}_{0d}$ is composed of all the null-space vectors obtained at the nodes outside conductors, i.e., whose node conductivity is zero, and additional $\#c$ vectors, where $\#c$ is the number of conductors in the layout. In these $\#c$ vectors, each vector corresponds to one conductor, which is the sum of the null-space vectors generated at the nodes inside and on the surface of the conductor. $\mathbf{V}_{0d}$ can be written as

$$\mathbf{V}_{0d} = \left[\underbrace{\{\mathbf{V}_{0,i}(\sigma_i = 0)\}}_{nd-1 \text{ vectors}} | \underbrace{\left(\sum_{\mathbf{r}_k \in \Omega_{c,1}} \mathbf{V}_{0,k}\right) | \ldots | \left(\sum_{\mathbf{r}_k \in \Omega_{c,\#c}} \mathbf{V}_{0,k}\right)}_{\#c \text{ vectors}}\right] \tag{41}$$

where in the first set, nd denotes the number of dielectric nodes, σ_i denotes the conductivity at node i, and $\mathbf{r}_k \in \Omega_{c,k}$ $(k = 1, 2, \ldots, \#c)$ represents the nodes in the kth conductor, including those falling onto the kth conductor's surface. Each summation in (41) results in a vector containing all the edges exterior to the conductor and perpendicular to the conductor surface, which has one and only one node falling onto the conductor. All the entries corresponding to the edges, thus, electric field unknowns, inside the conductors are canceled in the summation because of opposite signs. From (41), it can be seen that $\mathbf{V}_{0d}$ satisfies

$$\text{diag}\{\sigma\}\mathbf{V}_{0d} = 0. \tag{42}$$

Each vector in $\mathbf{V}_{0c}$ is the null-space vector corresponding to one node inside or on the surface of the conductors. The number of $\mathbf{V}_{0c}$ for each conductor is $\mathrm{nc}_i - 1$, where nc_i denotes the number of nodes in the ith conductor. Hence

$$\mathbf{V}_{0c,k} = \mathbf{V}_{0,k}(\sigma_k \neq 0) \tag{43}$$

and for each conductor, one node is excluded for generating the above-mentioned equation since there is one vector considered in (41).

The left null-space $\mathbf{V}_{0a}$ can also be decomposed into $\mathbf{V}_{0\mathrm{da}}$ and $\mathbf{V}_{0\mathrm{ca}}$, in the same way as $\mathbf{V}_0$ is decomposed into $\mathbf{V}_{0d}$ and $\mathbf{V}_{0c}$. $\mathbf{V}_{0\mathrm{da}}$ contains all the null-space vectors obtained at the nodes outside conductors plus $\#c$ vectors. Each vector in $\#c$ vectors corresponds to one conductor, which is the weighted sum of the $\mathbf{V}_{0a}$ vectors from the nodes inside and on the surface of the conductor. The weights are chosen such that the summation eliminates the edges inside and on the surface of each conductor, which makes $\mathbf{V}_{0\mathrm{da}}$ have only nonzeros entries in the dielectric part, and thus

$$\mathrm{diag}\{\sigma\}\mathbf{V}_{0\mathrm{da}} = \mathbf{V}_{0\mathrm{da}}^T \mathrm{diag}\{\sigma\} = 0. \tag{44}$$

This weight (for the $\mathbf{V}_{0a}$ vector at a conductor node) can be readily found as $l_x^a l_y^a l_z^a$, where $l_{x,y,z}^a$ represents the average length of the two edges connected to the node along the x-, y-, and z-directions, respectively. $\mathbf{V}_{0\mathrm{ca}}$ is the subset of $\mathbf{V}_{0a}$ generated at the node inside or on the surface of the conductors, which is similar to $\mathbf{V}_{0c}$.

As shown earlier, $\mathbf{V}_{0d}$, $\mathbf{V}_{0c}$, $\mathbf{V}_{0\mathrm{da}}$, and $\mathbf{V}_{0\mathrm{ca}}$ in (29) are all found analytically in this article from mesh information, hence greatly saving the computational cost. Furthermore, the number of nonzero entries in each $\mathbf{V}_{0d}(\mathbf{V}_{0\mathrm{da}})$ and $\mathbf{V}_{0c}(\mathbf{V}_{0\mathrm{ca}})$ vector is bounded by the number of edges connected to a single node, thus very sparse; $\mathbf{D}$ is diagonal. As for $\mathbf{D}_{\epsilon,0}$ and $\mathbf{D}_{\sigma,0}$ shown in (30), after substituting the analytical null-space vectors into their expressions, we find the two matrices are nothing but the Laplacian operator formulated for the dielectric region, and the conductor region, respectively, i.e., discretized $\nabla(\epsilon \cdot \nabla)$ and $\nabla(\sigma \cdot \nabla)$ using a finite difference method. Hence, their matrix solutions can be obtained efficiently using either an iterative solver, such as a multigrid method [38], or an advanced direct solver [6], both of which have been achieved in linear complexity. Hence, the $\mathbf{V}_0$ component can be found rapidly in this article.

V. Efficient Method for Finding $\mathbf{V}_h$ and Fast Computation of the L and Full-Wave Components of Layout Response

For many of the IC layouts, we find the $\mathbf{V}_0$ solution is sufficient to obtain an accurate layout response at their current operating frequencies. However, when frequency increases, and/or the layout becomes larger such as the layout of packages and boards, the $\mathbf{V}_h$ part becomes important in the layout solution, and we need to find an efficient way to obtain it. In this section, we show how to obtain the high-order space $\tilde{\mathbf{V}}_h = \mathbf{D}^{-1}\mathbf{V}_h$ fast in order to solve (28) with little computational cost.

The solution of (2) is governed by a quadratic eigenvalue problem

$$(\lambda^2 \mathbf{D}_\epsilon + \lambda \mathbf{D}_\sigma + \mathbf{S})\upsilon = 0 \tag{45}$$

where $\mathbf{D}_\epsilon$ and $\mathbf{D}_\sigma$ are, respectively, diagonal matrices of permittivity and conductivity, λ is an eigenvalue whose unit is rad/s, and υ is the corresponding eigenvector. The eigenvectors corresponding to nonzero eigenvalues of (45) can be used as $\mathbf{V}_h$. These eigenvectors are also frequency- and time-independent. Compared with using the nonnull-space eigenvectors of $\mathbf{S}$, we find that using the eigenvectors of (45), the resulting number of $\mathbf{V}_h$ modes to synthesize the layout solution is very small. This is because each eigenvector of (45) represents a source-free solution in the original physical problem satisfying all the material and boundary conditions. In contrast, the eigenvector of $\mathbf{S}$ is a source-free solution in an empty computational domain, which does not represent the solution well in the actual problem. The eigenvalue of (45) has a clear physical meaning, which is the complex resonance frequency of the layout. For a prescribed frequency, the weight of an eigenmode of (45) in the field solution is inversely proportional to the difference between the eigenvalue and the solving frequency. In other words, the contribution of those eigenvectors that resonate at a higher frequency is little to the layout response at a lower working frequency. Hence, the number of $\mathbf{V}_h$ computed in this way is small, thus making the whole solution efficient. However, solving (45) is known to be computationally expensive, especially when conductor loss is involved, which is true in the problem studied in this article. Most of the eigenvalues and eigenmodes are complex valued, and due to the large discrepancy in the norm of the underlying matrices, the solution of (45) is also error prone. In this article, based on our prior work in [36] and [37], we develop a fast algorithm to extract $\mathbf{V}_h$ without solving (45).

In this fast algorithm, we solve (2) in a small time window using an explicit time marching. In this way, there is no matrix solution involved. The computational complexity is linear (optimal) at every time step. Although the time step is restricted by the smallest space step for stability, we do not need to perform the time marching for a long time since we can identify $\mathbf{V}_h$ from a short time simulation. We collect the solution of (2) every SG step, which is chosen based on $\mathrm{SG} \leq 1/((10 f_{\max})\Delta t)$, where $f_{\max}$ is the maximum frequency present in the system, and Δt is the time step required by the stability criterion. At the first sampling step, we record the solution e, normalize it, and store it as a column vector in $\mathbf{X}$; in the following sampling steps, we orthogonalize the newly obtained solution with existing columns in $\mathbf{X}$ and store the resultant in $\mathbf{X}$. Using such $\mathbf{X}$, we transform (45) to a much smaller eigenvalue problem of

$$(\lambda^2 \mathbf{D}_{\epsilon r} + \lambda \mathbf{D}_{\sigma r} + \mathbf{S}_r)\upsilon_r = 0 \tag{46}$$

where

$$\mathbf{D}_{\epsilon r} = \mathbf{X}^T \mathbf{D}_\epsilon \mathbf{X} \tag{47}$$

$$\mathbf{D}_{\sigma r} = \mathbf{X}^T \mathbf{D}_\sigma \mathbf{X} \tag{48}$$

$$\mathbf{S}_r = \mathbf{X}^T \mathbf{S} \mathbf{X}. \tag{49}$$

The (46) can further be transformed to a generalized eigenvalue problem as the following:

$$\mathbf{A}\begin{bmatrix} \upsilon \\ \lambda\upsilon \end{bmatrix} = \lambda\mathbf{B}\begin{bmatrix} \upsilon \\ \lambda\upsilon \end{bmatrix} \tag{50}$$

in which

$$\mathbf{A} = \begin{bmatrix} -\mathbf{S}_r & 0 \\ 0 & \mathbf{D}_{\epsilon r} \end{bmatrix}$$
$$\mathbf{B} = \begin{bmatrix} \mathbf{D}_{\sigma r} & \mathbf{D}_{\epsilon r} \\ \mathbf{D}_{\epsilon r} & 0 \end{bmatrix}. \tag{51}$$

The size of (50) is $2p$, where p is the column size of $\mathbf{X}$, i.e., the number of time domain solutions that have been collected.

There exists a big difference in the norms of $\mathbf{S}$, $\mathbf{D}_\epsilon$, and $\mathbf{D}_\sigma$; directly calculating (50) may not be accurate. In order to solve that based on [39], we multiply scaling factors ρ to make $\mathbf{A}$ and $\mathbf{B}$ balanced in norm. Hence, we transform the matrices to

$$\tilde{\mathbf{A}} = \begin{bmatrix} -\mathbf{S}_r & 0 \\ 0 & \rho^2\mathbf{D}_{\epsilon r} \end{bmatrix}$$
$$\tilde{\mathbf{B}} = \begin{bmatrix} \rho\mathbf{D}_{\sigma r} & \rho^2\mathbf{D}_{\epsilon r} \\ \rho^2\mathbf{D}_{\epsilon r} & 0 \end{bmatrix} \tag{52}$$

and (50) to

$$\tilde{\mathbf{A}}\begin{bmatrix} \upsilon \\ \dfrac{\lambda}{\rho}\upsilon \end{bmatrix} = \frac{\lambda}{\rho}\tilde{\mathbf{B}}\begin{bmatrix} \upsilon \\ \dfrac{\lambda}{\rho}\upsilon \end{bmatrix}. \tag{53}$$

The above-mentioned scaling does not change the upper part of the eigenvectors. The original eigenvalues can be obtained by multiplying the eigenvalues of (53) by ρ. From the expression of each matrix, we know that $\|\mathbf{S}\| \approx (1/l^2\mu)$, $\|\mathbf{D}_\sigma\| = \sigma$, and $\|\mathbf{D}_\epsilon\| = \epsilon$, where l is feature size. Based on this information, we can determine the scaling factor ρ [39]. For example, for a μm-scale circuit, we choose $\rho = 10^{12}$ based on the scaling technique given in [39].

Since we need to select eigenmodes corresponding to the nonzero eigenvalues to build $\mathbf{V}_h$, there should be an estimation of the magnitude of the smallest nonzero eigenvalue. From (45), the magnitude of the eigenvalues can be analyzed from the norm of each matrix. Specifically, the eigenvalues can be estimated as $(-\|\mathbf{D}_\sigma\| \pm (\|\mathbf{D}_\sigma\|^2 - 4\|\mathbf{D}_\epsilon\|\|\mathbf{S}\|)^{1/2})/2\|\mathbf{D}_\epsilon\|$. Using this method, for a microscale circuit whose feature size is at the level of μm, the magnitude of the eigenvalues can be found in the range of 10^{10} and 10^{18}. Therefore, for those eigenvalues smaller than 10^{10}, we can identify them as zero eigenvalues and exclude their eigenmodes from $\tilde{\mathbf{V}}_h$.

When we march on in time, we find eigenvalues repeatedly show up from the small eigenvalue problem (53). The reason for this can be found from [36]. Although a lossless problem is studied in [36], the same theoretical reason applies to the lossy problem studied in this article. There are two criteria we use to terminate the time-domain solution collection process. First, we need to make sure that the eigenmodes corresponding to the repeating eigenvalues become dominant in the field solution. If the weight of the modes corresponding to the repeating eigenvalues is larger than that of the other modes based on an accuracy parameter ϵ_1, they can be collected as $\mathbf{V}_h$. To calculate the weight of the modes, we denote the upper half of the eigenvectors of (53) corresponding to the repeating eigenvalues by $\mathbf{V}_{\text{re}}$ and other eigenvectors by $\mathbf{V}_{\text{nre}}$. Let $\Phi = [\mathbf{V}_{\text{re}}, \mathbf{V}_{\text{nre}}]$. First, we orthogonalize $\mathbf{V}_{\text{re}}$ to be unitary $\tilde{\mathbf{V}}_{\text{re}}$. Next, we remove $\mathbf{V}_{\text{nre}}$'s $\tilde{\mathbf{V}}_{\text{re}}$ component, as $\tilde{\mathbf{V}}_{\text{nre}} = \mathbf{V}_{\text{nre}} - \tilde{\mathbf{V}}_{\text{re}}\tilde{\mathbf{V}}_{\text{re}}^H\mathbf{V}_{\text{nre}}$. Then, from $\Phi_{\text{new}} = [\tilde{\mathbf{V}}_{\text{re}}, \tilde{\mathbf{V}}_{\text{nre}}]$, the coefficient w is calculated as

$$w = \left(\Phi_{\text{new}}^H\Phi_{\text{new}}\right)^{-1}\left(\Phi_{\text{new}}^H e\right) \tag{54}$$

where $w = [w_{\text{re}}, w_{\text{nre}}]$. If the weight ratio

$$\left(w_{\text{re}}^H w_{\text{re}}\right)/\left(w_{\text{nre}}^H w_{\text{nre}}\right) > \epsilon_1 \tag{55}$$

$\mathbf{V}_{\text{re}}$ would be counted as $\mathbf{V}_h$.

The second criterion is used to ensure the accuracy of $\mathbf{V}_h$. At every SG steps, we compare the eigenvalues from two adjacent steps: q and $q+1$. If the difference between the eigenvalues is less than a prescribed error tolerance ϵ_2, which is

$$\frac{|\lambda^q - \lambda^{q+1}|}{|\lambda^q|} < \epsilon_2 \tag{56}$$

the corresponding eigenmode can be identified as an accurate $\mathbf{V}_h$ mode. After (55) and (56) are satisfied, the solution collection process is terminated.

Let the mode extracted from the aforementioned procedure be $\tilde{\mathbf{V}}_h$. It may contain a $\mathbf{V}_0$ component due to numerical error, i.e., it is not purely a high-order mode we look for. Writing it as

$$\tilde{\mathbf{V}}_{h,i} = U_0 u_{0,i} + \mathbf{D}^{-1}\mathbf{V}_{h,i}u_{h,i} \tag{57}$$

the second component is the one we want to find. Here, U_0 is comprised of only two vectors

$$U_0 = [U_{0,C} \quad U_{0,R}] \tag{58}$$

where $U_{0,C}$ is the C component of the layout solution

$$U_{0,C} = \mathbf{V}_{0d}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\text{da}}^T/(-j\omega)J \tag{59}$$

and $U_{0,R}$ is the R component of the layout solution

$$\begin{aligned} U_{0,R} = {} & \mathbf{V}_{0d}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\text{da}}^T\text{diag}\{\epsilon\}\mathbf{V}_{0c}\mathbf{D}_{\sigma,0}^{-1}\mathbf{V}_{0\text{ca}}^T \\ & \times\left(\mathbf{I} - \text{diag}\{\epsilon\}\mathbf{V}_{0d}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\text{da}}^T\right)J \\ & + \mathbf{V}_{0c}\mathbf{D}_{\sigma,0}^{-1}\mathbf{V}_{0\text{ca}}^T\left(\text{diag}\{\epsilon\}\mathbf{V}_{0d}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\text{da}}^T - \mathbf{I}\right)J \end{aligned} \tag{60}$$

both of which have been found when computing the $\mathbf{V}_0$ component of the field solution.

Multiplying (57) by the left null-space U_{0a}^T, which is similar to U_0^T except that it is in the $\mathbf{V}_{0a}$ space, and thus

$$U_{0a,C} = \mathbf{V}_{0\text{da}}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\text{da}}^T/(-j\omega)J \tag{61}$$

and

$$\begin{aligned} U_{0a,R} = {} & \mathbf{V}_{0\text{da}}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\text{da}}^T\text{diag}\{\epsilon\}\mathbf{V}_{0c}\mathbf{D}_{\sigma,0}^{-1}\mathbf{V}_{0\text{ca}}^T \\ & \times\left(\mathbf{I} - \text{diag}\{\epsilon\}\mathbf{V}_{0d}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\text{da}}^T\right)J \\ & + \mathbf{V}_{0\text{ca}}\mathbf{D}_{\sigma,0}^{-1}\mathbf{V}_{0\text{ca}}^T\left(\text{diag}\{\epsilon\}\mathbf{V}_{0d}\mathbf{D}_{\epsilon,0}^{-1}\mathbf{V}_{0\text{da}}^T - \mathbf{I}\right)J. \end{aligned} \tag{62}$$

The multiplication results in

$$U_{0a}^T\mathbf{D}\tilde{\mathbf{V}}_{h,i} = U_{0a}^T\mathbf{D}U_0 u_{0,i}. \tag{63}$$

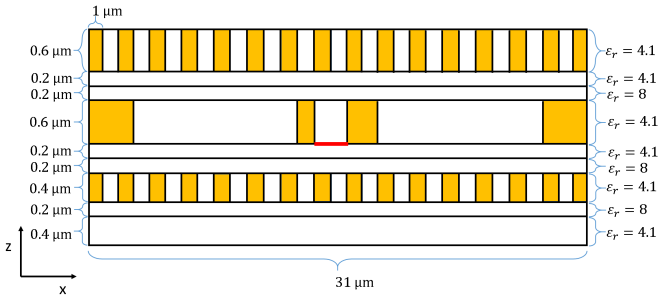

Fig. 3. Illustration of a 3-D on-chip interconnect layout.

Hence

$$u_{0,i} = \left(U_{0a}^T \mathbf{D} U_0\right)^{-1} U_{0a}^T \mathbf{D} \tilde{\mathbf{V}}_{h,i}. \tag{64}$$

As a result, we can obtain a pure $\mathbf{V}_h$ part from the contaminated $\tilde{\mathbf{V}}_h$ as the following:

$$\tilde{\mathbf{V}}_h = \tilde{\mathbf{V}}_h - U_0 \left(U_{0a}^T \mathbf{D} u_0\right)^{-1} \left(U_{0a}^T \mathbf{D} \tilde{\mathbf{V}}_h\right) \tag{65}$$

which satisfies $\mathbf{V}_{0a}^T \mathbf{D} \tilde{\mathbf{V}}_h = 0$, and, thereby, $\mathbf{V}_{0a}^T \mathbf{V}_h = 0$. Then, we can apply this $\tilde{\mathbf{V}}_h$ in (28) to obtain the $\mathbf{V}_h$ part of the solution. Since $\mathbf{V}_0^T \mathbf{V}_h = 0$ is not satisfied but $\mathbf{V}_{0a}^T \mathbf{V}_h = 0$ is satisfied, if we use $\tilde{\mathbf{V}}_h$ as the testing column space in (28), there is a term $\mathbf{V}_h^T \mathbf{V}_0 y_0$ left, which cannot be vanished. However, this term is known, which can be moved to the right-hand side of (28). Hence, y_h can still be readily solved. After we solve y_h, the final solution is combined as

$$e = \mathbf{V}_{0d} y_{0d} + \mathbf{V}_{0c} y_{0c} + \tilde{\mathbf{V}}_h y_h \tag{66}$$

which contains the complete R, C, L, and full-wave components. The number of $\mathbf{V}_h$ modes is usually small for IC layouts; thus, (28) has a very small dimension, whose solution can be readily computed.

VI. Layout Modeling and Simulation Results

In this section, we simulate a variety of IC layouts to examine the performance of the proposed work. For all the examples, the top and bottom boundaries are truncated by the PEC, and the other four sides are terminated by PMC.

A. Bus Wire

A 3-D on-chip interconnect example is simulated, which is shown in Fig. 3. The sizes along the x-, y-, and z-directions are 31, 10, and 3 μm, respectively. The yellow regions are conductors. Their conductivity is 5.7×10^7 S/m. The material and geometrical data are specified in Fig. 3. The current source is imposed across the red line. In Table I, we list the capacitance obtained from the proposed inverse model in comparison with the reference result obtained from a brute-force finite-difference solution in the frequency domain. Excellent agreement is observed.

TABLE I

Capacitance Computed at the Near (Port 1) and Far End (Port 2)

Capacitance (F)	This Method	Reference
C_{11}	1.0356×10^{-15}	1.0356×10^{-15}
C_{12}	1.0356×10^{-15}	1.0356×10^{-15}

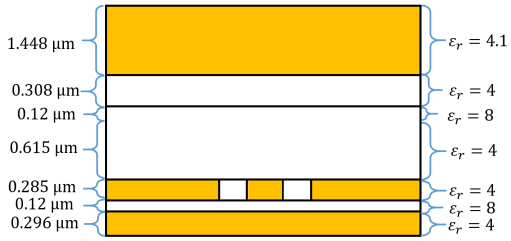

Fig. 4. Structure of a test-chip interconnect.

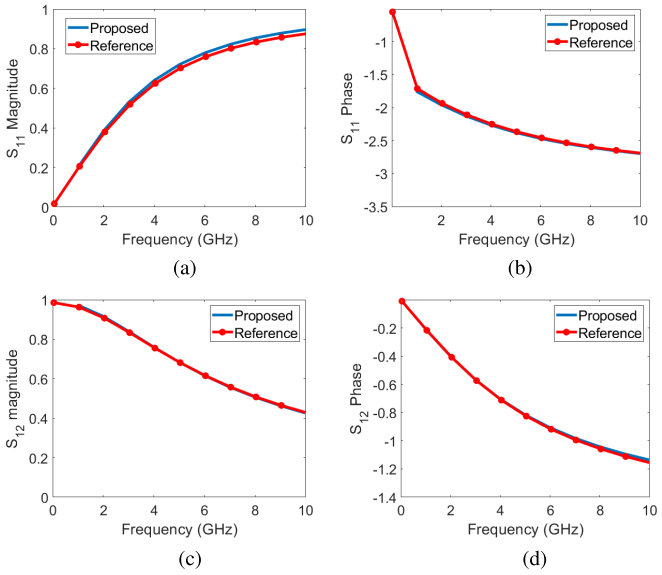

Fig. 5. S-parameters of the test-chip interconnect of 100-μm length. (a) $|S_{11}|$. (b) S_{11} phase (radians). (c) $|S_{12}|$. (d) S_{12} phase (radians).

B. Test-Chip Interconnect

A test-chip interconnect is simulated, whose structure is shown in Fig. 4. The yellow regions are conductors, the conductivity of which is 5.7×10^7 S/m. The dimension along the x-, y- and z-directions is 300, 100, and 3.912 μm, respectively. The current source is launched from the bottom ground plane to the conductor in the metal-3 layer. We compare the S-parameters extracted from our method from 45 MHz to 10 GHz with the measured data in Fig. 5, which is the result of the $\mathbf{V}_0$ mode solution. As can be seen, they agree very well with each other. This verifies the accuracy of the proposed method.

When we increase the frequency up to 100 GHz, we find that the RC component is not sufficient anymore in producing good accuracy. As can be seen from Fig. 6, without considering $\mathbf{V}_h$, the entire solution error becomes worse and worse when the frequency is increased, and it becomes 16.9% at 50 GHz and even exceeds 40% at 100 GHz. Here, the entire

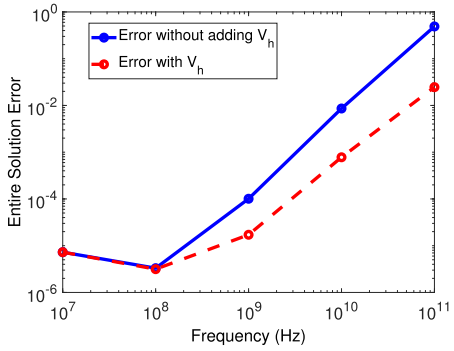

Fig. 6. Entire solution error before and after adding the $\mathbf{V}_h$ part of the solution as a function of frequency for the test-chip interconnect example.

TABLE II

FIRST 20 EIGENVALUES FROM THE PROPOSED FAST EIGENVALUE SOLUTION COMPARED WITH THOSE FROM THE ORIGINAL EIGENVALUE SOLUTION FOR THE INTERCONNECT EXAMPLE

Eigenvalue from brute-force solution (rad/s)	Eigenvalue from fast solution (rad/s)
$-5.2774\times10^{11}\pm1.3077\times10^{12}$j	$-5.2812\times10^{11}\pm1.3075\times10^{12}$j
$-4.7621\times10^{11}\pm1.3428\times10^{12}$j	$-4.7623\times10^{11}\pm1.3428\times10^{12}$j
$-5.4773\times10^{11}\pm2.8958\times10^{12}$j	$-5.2391\times10^{11}\pm2.9010\times10^{12}$j
$-5.1701\times10^{11}\pm2.9430\times10^{12}$j	$-5.1427\times10^{11}\pm2.9423\times10^{12}$j
$-5.5160\times10^{11}\pm4.3458\times10^{12}$j	$-5.3063\times10^{11}\pm4.3972\times10^{12}$j
$-5.2938\times10^{11}\pm4.3995\times10^{12}$j	$-5.3063\times10^{11}\pm4.3972\times10^{12}$j
$-6.3684\times10^{10}\pm5.3430\times10^{12}$j	$-6.3678\times10^{10}\pm5.3431\times10^{12}$j
$-5.3620\times10^{11}\pm5.7451\times10^{12}$j	$-5.3561\times10^{11}\pm5.7433\times10^{12}$j
$-5.4049\times10^{11}\pm6.9653\times10^{12}$j	$-5.4235\times10^{11}\pm6.9603\times10^{12}$j
$-5.4333\times10^{11}\pm8.0397\times10^{12}$j	$-5.4189\times10^{11}\pm8.0346\times10^{12}$j

solution error is measured by

$$\text{Entire Solution Error} = \frac{\|e - e_{\text{ref}}\|}{\|e_{\text{ref}}\|} \tag{67}$$

where e is from the proposed solution that contains all electric field unknowns in the layout, whereas e_{ref} is a brute-force solution obtained by solving (3) as it is. Hence, we employ the algorithm described in Section V to extract $\mathbf{V}_h$ modes and add the $\mathbf{V}_h$ component into the solution of e. In the time-marching procedure, we use a Gaussian derivative source with $\tau = 10^{-11}$ s. Δt is chosen to be 10^{-15} s for the time-domain stability. Other simulation parameters are chosen as $\epsilon_1 = 10^{-5}$, $\epsilon_2 = 10^{-2}$, and SG = 100. From the procedure, we identify 30 $\mathbf{V}_h$ modes. After adding the $\mathbf{V}_h$ part of the solution, we obtain the entire solution error shown by the red line in Fig. 6. The error is significantly reduced from 16.9% to 1.06% at 50 GHz and from 40% to 2% at 100 GHz. Only 32 steps of sampling are performed in the time-marching procedure, and hence, the time window simulated is short, and, thereby, the overall simulation is efficient. The proposed algorithm also allows one to achieve even higher accuracy by performing the time marching in a longer time window and, hence, extracting more $\mathbf{V}_h$ modes. For example, using 400 steps of sampling, we find 231 $\mathbf{V}_h$ modes, using which the accuracy of the field solution is further reduced from 1.06% to 0.04% at 50 GHz.

In Table II, we list the first 20 eigenvalues, sorted based on the imaginary part's magnitude, found from the proposed fast solution in comparison with those computed from a brute-force eigenvalue solution of (45). The excellent agreement can be observed, which validates the proposed fast algorithm for finding physically important eigenvectors.

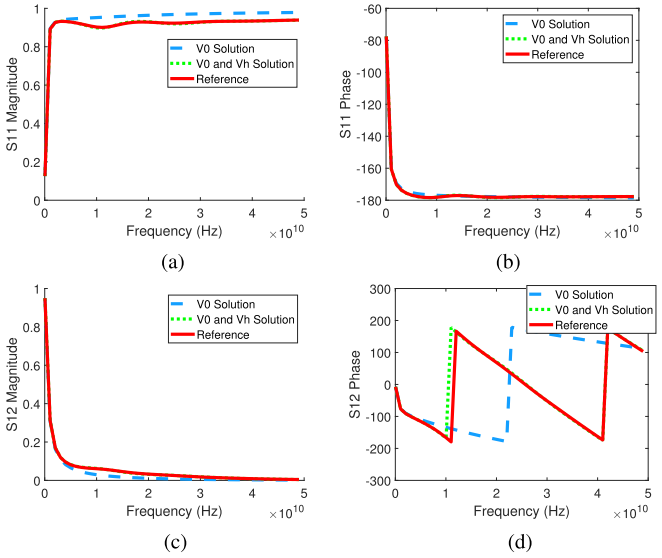

Fig. 7. S-parameters of the test-chip interconnect of 2000-μm length. (a) $|S_{11}|$. (b) S_{11} phase (degrees). (c) $|S_{12}|$. (d) S_{12} phase (degrees). (Reference is from measurements.)

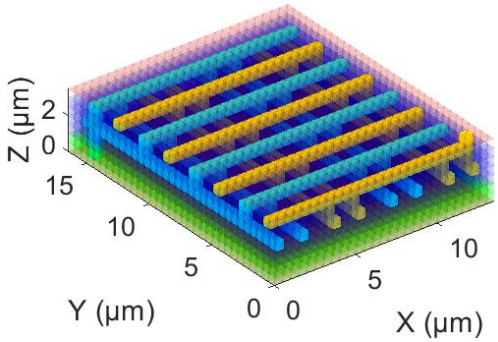

Fig. 8. Structure of an on-chip power grid.

In this example, we also elongate the structure to a length of 2000 μm. The S-parameters extracted from the proposed method are shown in Fig. 7. The blue line shows the result generated by using $\mathbf{V}_0$ only and, hence, the RC component of the layout solution. The green line depicts the result with both $\mathbf{V}_0$ and $\mathbf{V}_h$ components, where 27 $\mathbf{V}_h$ modes are used. As can be seen, only the green line matches the reference result. $\mathbf{V}_h$ becomes important in this structure since its electrical size is larger than the 100-μm-long one.

C. On-Chip Power Grid

In this example, we simulate an on-chip power grid shown in Fig. 8. The power wire is colored in yellow, while the ground wire is in blue. The regions other than conductors are dielectrics. The current source is a Gaussian derivative with $\tau = 10^{-12}$ s, and it is injected from the ground wire to the power wire, which is shown by the red line in Fig. 8.

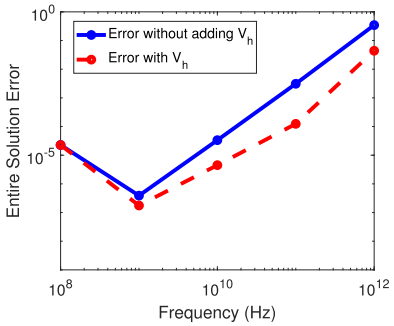

Fig. 9. Entire solution error before and after adding the $\mathbf{V}_h$ part of the solution for different frequencies for the power grid structure.

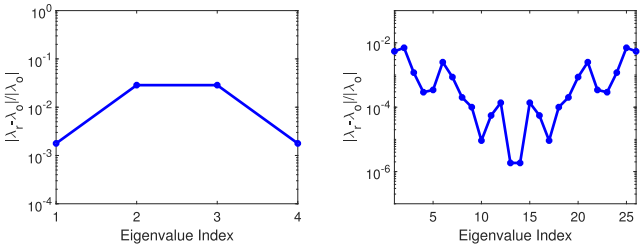

Fig. 10. Comparison of the eigenvalues from the proposed fast solution and the original eigenvalue solution with (a) five steps of sampling with SG = 100 and (b) 300 steps of sampling with SG = 5 for the power grid example.

In this example, the $\mathbf{V}_h$ part is also needed to obtain good accuracy at high frequencies. To find $\tilde{\mathbf{V}}_h$, the parameters used are $\epsilon_1 = 10^{-5}$, $\epsilon_2 = 10^{-2}$, and SG $= 100$. The time step used in the explicit time marching is $\Delta t = 10^{-15}$ s. There are four $\mathbf{V}_h$ modes found with five steps of sampling. Their eigenvalues are $-5.3506 \times 10^{10} \pm 2.0334 \times 10^{13} j$ and $-1.2362 \times 10^{11} \pm 5.2297 \times 10^{13} j$. Without adding the four modes, the error of the entire solution is 34.48% at 1000 GHz; adding them, the error is greatly reduced to 4.4%. The accuracy before and after adding the four $\mathbf{V}_h$ modes is shown in Fig. 9. Again, when we increase the time window for time marching, we find more $\mathbf{V}_h$ modes, and also they are more accurate. In Fig. 10(a) and (b), we plot the error of the complex eigenvalues of the $\mathbf{V}_h$ modes extracted using five steps of sampling with SG $= 100$ and 300 steps of sampling with SG $= 5$, respectively. As can be seen, although the accuracy of both is good, the latter case is more accurate, and having more $\mathbf{V}_h$ modes is identified. For the latter case, 299 $\mathbf{V}_h$ modes are identified, using which the entire solution error is reduced to 1.7131×10^{-6} at 1000 GHz. We also compare the S-parameters extracted from this method (with both $\mathbf{V}_0$ and $\mathbf{V}_h$ modes) and those from the finite difference method in Fig. 11. As can be seen, they agree very well with each other.

In Table III, we list the first 20 eigenvalues found from the proposed fast algorithm in comparison with those of the original eigenvalue solution. As can be seen, they match each other very well, which validates the proposed method for finding high-order modes.

D. Scan D Flip-Flop Layout

Next, to examine the capability of the proposed work, we take a GDSII file from a 45-nm Scan D flip-flop design [40] and analyze its layout performance. The top view of the

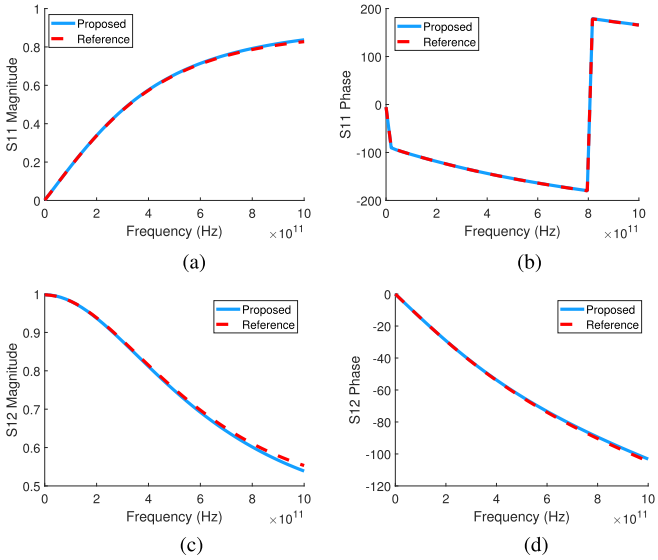

Fig. 11. S-parameters of an on-chip power grid. (a) $|S_{11}|$. (b) S_{11} phase (degrees). (c) $|S_{12}|$. (d) S_{12} phase (degrees).

TABLE III

FIRST 20 EIGENVALUES FROM THE PROPOSED FAST EIGENVALUE SOLUTION COMPARED WITH THOSE FROM THE ORIGINAL EIGENVALUE SOLUTION FOR THE POWER GRID EXAMPLE

Eigenvalue from brute-force solution (rad/s)	Eigenvalue from fast solution (rad/s)
$-2.0932\times10^{10}\pm1.4133\times10^{13}$j	$-2.0915\times10^{11}\pm1.4133\times10^{13}$j
$-2.5515\times10^{10}\pm2.0933\times10^{13}$j	$-2.2350\times10^{10}\pm2.0932\times10^{13}$j
$-2.2928\times10^{10}\pm2.3214\times10^{13}$j	$-2.3428\times10^{10}\pm2.3210\times10^{13}$j
$-2.2120\times10^{10}\pm2.6723\times10^{13}$j	$-2.1924\times10^{10}\pm2.6723\times10^{13}$j
$-2.1983\times10^{10}\pm2.9874\times10^{13}$j	$-2.7626\times10^{10}\pm2.9874\times10^{13}$j
$-2.2730\times10^{10}\pm3.5079\times10^{13}$j	$-2.3174\times10^{10}\pm3.5086\times10^{13}$j
$-2.5862\times10^{10}\pm3.9890\times10^{13}$j	$-6.5502\times10^{10}\pm3.9903\times10^{13}$j
$-2.4912\times10^{10}\pm4.0165\times10^{13}$j	$-1.0058\times10^{11}\pm4.0227\times10^{13}$j
$-2.3851\times10^{10}\pm4.4811\times10^{13}$j	$-3.5384\times10^{10}\pm4.4819\times10^{13}$j
$-2.3552\times10^{10}\pm4.7854\times10^{13}$j	$-1.8570\times10^{10}\pm4.7841\times10^{13}$j

structure in layers 9–11 is shown in Fig. 12, with each layer plotted in different colors. The length and width of this structure are 13 and 3.33 μm. The blue and green regions are occupied by conductors, whose conductivity is 5.7×10^7 S/m. The current is injected from the V_{SS} conductor to the V_{DD} conductor, the waveform of which is a Gaussian derivative with $\tau = 10^{-11}$ s and $t_0 = 3\tau$. In this example, there are around 3,616,773 unknowns. To simulate this example, the time step of a traditional FDTD must be as small as 10^{-16} s to ensure stability. The proposed method is able to use an arbitrarily large time step since its time dependence is analytically derived in the inverse model for the *RC* component. The proposed method uses a time step of 10^{-12} s solely determined by accuracy. It only takes 34.02 s, whereas the FDTD costs 6.9×10^5 s to finish the simulation of the whole structure in the same time window. In Fig. 13, we compare the port voltages in the time domain simulated from the proposed method and the FDTD. As can be seen, they agree very well with each other. In Fig. 14, we also compare the impedance Z-parameters extracted from the proposed method with those from the finite difference method in the frequency domain, which also shows excellent agreement.

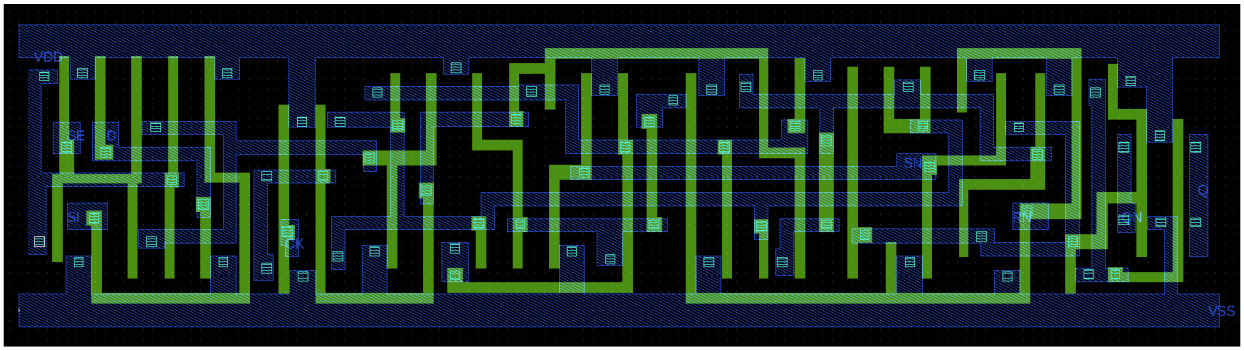

Fig. 12. Top view of the Scan D flip-flop layout in layers 9–11.

TABLE IV
Z-PARAMETERS EXTRACTED AT $f = 10$ GHz FROM THE PORTS SHOWN IN FIG. 15

0.0143–j2.56	0.00615–j1.54	0.00443–j1.40	-0.00139–j2.56	-0.000905–j2.15	-0.000652–j1.70	-0.00113–j2.56
0.00616–j1.54	0.00664–j318.768	0.00235–j81.86	0.00025–j1.54	0.000333–j1.30	0.000276–j1.03	-0.000918–j1.54
0.00443–j1.40	0.00235–j81.86	0.00699–j261.79	0.00141–j1.40	0.00126–j1.20	0.000981–j0.949	-0.00109–j1.40
-0.00139–j2.56	0.00025–j1.54	0.00141–j1.40	0.137–j2.56	0.0824–j2.15	0.0554–j1.70	-0.00691–j2.56
-0.000905–j2.15	0.000334–j1.30	0.00126–j1.20	0.0824–j2.15	0.0644–j195.21	0.0421–j22.43	-0.00547–j2.15
-0.000654–j1.70	0.000276–j1.03	0.000982–j0.949	0.0554–j1.70	0.0421–j22.43	0.0324–j477.88	-0.00412–j1.70
-0.00113–j2.56	-0.000918–j1.54	-0.00109–j1.40	-0.00691–j2.56	-0.00548–j2.15	-0.00412–j1.70	0.0131–j2.56

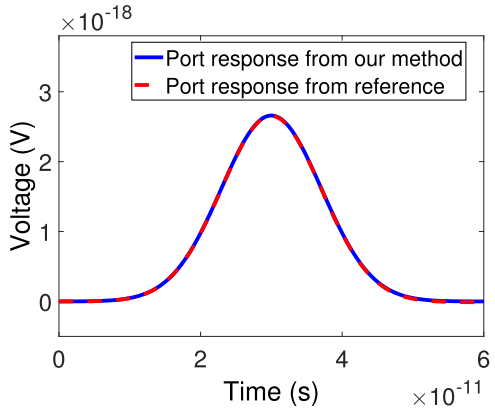

Fig. 13. Port response of the Scan D flip-flop simulated from this method (blue line) and the FDTD (red line).

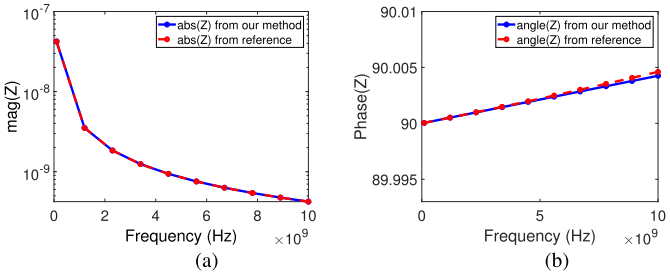

Fig. 14. Comparison of the Z-parameters of the Scan D flip-flop between this method and the finite difference method. (a) Magnitude. (b) Phase (degrees).

E. Intel 4004

The last example is an Intel 4004 processor (a 4-bit central processing unit), the layout of which is shown in Fig. 15. It has seven layers and over 86,220 objects, and the discretization of which results in 115,455,658 unknowns, which is over 115 million. The GDSII file of the processor is directly loaded into the software developed based on the proposed algorithm, and the layout analysis is fully automated. It only takes the proposed method 729 s to finish the extraction and analysis of the entire layout for one circuit stimulus, which demonstrates the efficiency and high capacity of this work. This is the result of the $\mathbf{V}_0$ part solution since this digital IC is electrically small. There are seven ports of interest as marked by the blue dots in Fig. 15. The impedance Z-parameters extracted at $f = 10$ GHz are shown in Table IV, where the value on the ith row and jth column denotes $\mathbf{Z}_{ij}$. The FDTD failed to simulate this example in feasible run time because of the requirement of a small-time step of 10^{-17} s for stability.

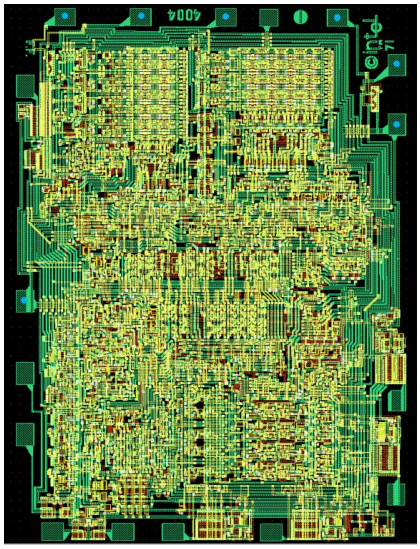

Fig. 15. Layout of Intel 4004 processor where the seven ports are marked by the blue dots.

VII. CONCLUSION

In this article, a closed-form model of the inverse of full-wave Maxwell's system of equations is found for an arbitrary physical layout in both frequency and time domains.

The advantages of the proposed inverse model of IC layouts are multifaceted. First, it is accurate from zero to high frequencies. Second, the layout response is explicitly decomposed into R, C, L, and full-wave components, without computation or approximation, each of which can be obtained independently, and then superposed to obtain the final layout response. This not only is much more efficient than a brute-force simulation but also provides circuit designers with key insights for layout automation. In addition, neither time marching nor point-by-point frequency sweep needs to be performed for the RC component as its time and frequency dependencies are analytically known from the inverse model. Moreover, the full-wave component is also efficiently represented by $\mathbf{V}_h$ modes whose number is small. Hence, both its time- and frequency-domain representations can be readily obtained. The proposed work has been applied to large-scale layout modeling and simulation. Superior performance in efficiency, accuracy, and capacity has been demonstrated. In addition to ICs, this article also provides package and board designers with a rapid, accurate, and circuit-intuitive tool for layout automation. Its broadband inverse model is also applicable to the electromagnetic analysis of other physical problems.

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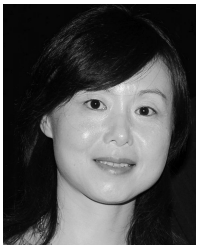

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Dr. Jiao was among the 21 women faculty selected across the country as the 2014–2015 Fellow of the Executive Leadership in Academic Technology and Engineering (ELATE) at Drexel University, a national leadership program for women in the academic STEM fields. She received the 2013 S. A. Schelkunoff Prize Paper Award from the IEEE Antennas and Propagation Society, which recognizes the Best Paper published in the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION during the previous year. She has been named a University Faculty Scholar by Purdue University since 2013. She was among the 85 engineers selected throughout the nation for the National Academy of Engineering's 2011 US Frontiers of Engineering Symposium. She was a recipient of the 2010 Ruth and Joel Spira Outstanding Teaching Award, the 2008 National Science Foundation (NSF) CAREER Award, the 2006 Jack and Cathie Kozik Faculty Start Up Award (which recognizes an outstanding new faculty member of the School of Electrical and Computer Engineering, Purdue University), the 2006 Office of Naval Research (ONR) Award under the Young Investigator Program, the 2004 Best Paper Award presented at the Intel Corporation's Annual Corporate-Wide Technology Conference (Design and Test Technology Conference) for her work on generic broadband model of high-speed circuits, the 2003 Intel Corporation's Logic Technology Development (LTD) Divisional Achievement Award, the Intel Corporation's Technology CAD Divisional Achievement Award, the 2002 Intel Corporation's Components Research the Intel Hero Award (Intel-wide, she was the tenth recipient), the Intel Corporation's LTD Team Quality Award, and the 2000 Raj Mittra Outstanding Research Award presented by the University of Illinois at Urbana–Champaign. She has served as a reviewer for many IEEE journals and conferences. She is also an Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY and the IEEE JOURNAL ON MULTISCALE AND MULTIPHYSICS COMPUTATIONAL TECHNIQUES.